

Document Title

512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	August 5 , 2002	
0.1	2' nd Draft Changed Icc, Icc1 value & 55ns product tDW value	November 11 , 2002	
0.2	3' rd Draft t_{LZ1} , t_{LZ2} value is changed from 5ns to 10ns t_{WP} value is changed from 55ns to 50ns (70ns product) t_{WP} value is changed from 45ns to 40ns (55ns product) VDR & IDR measurement condition change Changed I_{SB1} test conditions	March 13 , 2003	
0.3	4' th Draft Add Pb-free part number	February 13 , 2004	

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The attached datasheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

FEATURES

- Process Technology : 0.18 μ m Full CMOS
- Organization : 512K x 8 bit
- Power Supply Voltage : 2.7V ~ 3.3V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 36-FPBGA 6.0x7.0

GENERAL DESCRIPTION

The EM640FU8E families are fabricated by EMLSI' s advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1} , Typ)	Operating (I_{CC1} .Max)	
EM640FU8E	Industrial (-40 ~ 85°C)	2.7V~3.3V	55 ¹⁾ / 70ns	1 μ A	2 mA	36FPBGA

1. The parameter is measured with 30pF test load.

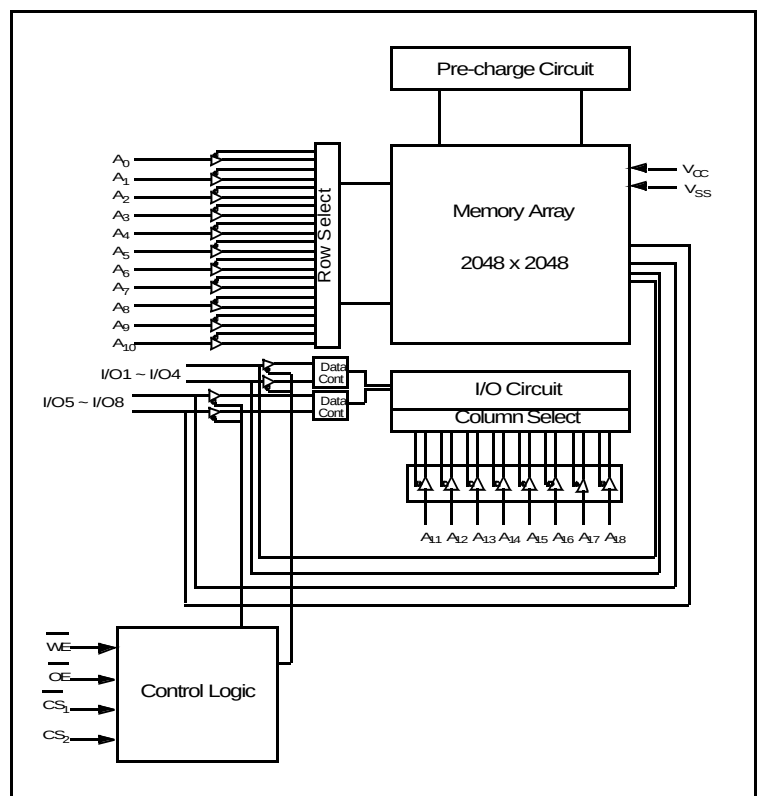
PIN DESCRIPTION

	1	2	3	4	5	6
A	A ₀	A ₁	CS ₂	A ₃	A ₆	A ₈
B	I/O ₅	A ₂	$\overline{WE}$	A ₄	A ₇	I/O ₁
C	I/O ₆		DNU	A ₅		I/O ₂
D	V _{SS}					V _{CC}
E	V _{CC}					V _{SS}
F	I/O ₇		A ₁₈	A ₁₇		I/O ₃
G	I/O ₈	$\overline{OE}$	$\overline{CS}_1$	A ₁₆	A ₁₅	I/O ₄
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

36-FPBGA : Top view (ball down)

Name	Function	Name	Function
$\overline{CS}_1, CS_2$	Chip select inputs	$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input	Vcc	Power Supply
A ₀ ~A ₁₈	Address Inputs	Vss	Ground
I/O ₁ ~I/O ₈	Data Inputs/outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.2 to $V_{CC}+0.3$ (Max. 4.0V)	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	°C

* Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	-	$V_{CC} + 0.2^{2)}$	V
Input low voltage	V_{IL}	-0.2 ³⁾	-	0.6	V

1. $T_A = -40$ to 85°C , otherwise specified
2. Overshoot: $V_{CC} + 2.0$ V in case of pulse width ≤ 20 ns
3. Undershoot: -2.0 V in case of pulse width ≤ 20 ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ ($f = 1\text{MHz}$, $T_A = 25^\circ\text{C}$)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	C_{IO}	$V_{IO} = 0\text{V}$	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-1	-	1	μA
Output leakage current	I _{LO}	$\overline{\text{CS}}_1 = \text{V}_{\text{IH}}$, CS ₂ =V _{IL} or $\overline{\text{OE}} = \text{V}_{\text{IH}}$ or $\overline{\text{WE}} = \text{V}_{\text{IL}}$, V _{IO} =V _{SS} to V _{CC}		-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, CS ₂ = $\overline{\text{WE}} = \text{V}_{\text{IH}}$, V _{IN} =V _{IH} or V _{IL}		-	-	2	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{\text{CS}}_1 \leq 0.2\text{V}$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V		-	-	2	mA
		I _{CC2}	Cycle time = Min, I _{IO} =0mA, 100% duty, $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	55ns	-	-	20
	70ns		-	-	15		
Output low voltage	V _{OL}	I _{OL} = 2.1mA		-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA		2.2	-	-	V
Standby Current (TTL)	I _{SB}	$\overline{\text{CS}}_1 = \text{V}_{\text{IH}}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}		-	-	0.3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{\text{CS}}_1 \geq \text{V}_{\text{CC}} - 0.2\text{V}$, CS ₂ ≥V _{CC} -0.2V ($\overline{\text{CS}}_1$ controlled) or 0V≤CS ₂ ≤0.2V (CS ₂ controlled), Other inputs=0~V _{CC} (Typ. condition : V _{CC} =3.0V @ 25°C) (Max. condition : V _{CC} =3.3V @ 85°C)	LL LF	-	1	5	μA

AC OPERATING CONDITIONS
Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.2V

Input Rise and Fall Time : 5ns

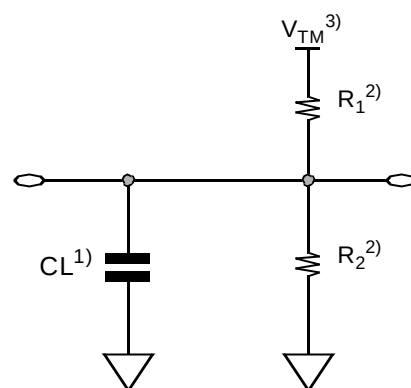
Input and Output reference Voltage : 1.5V

Output Load (See right) : CL = 100pF + 1 TTL

 $CL^{(1)} = 30pF + 1\text{ TTL}$

1. Including scope and Jig capacitance

 2. $R_1 = 3070\Omega$, $R_2 = 3150\Omega$

 3. $V_{TM} = 2.8V$

READ CYCLE ($V_{CC} = 2.7$ to $3.3V$, Gnd = 0V, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

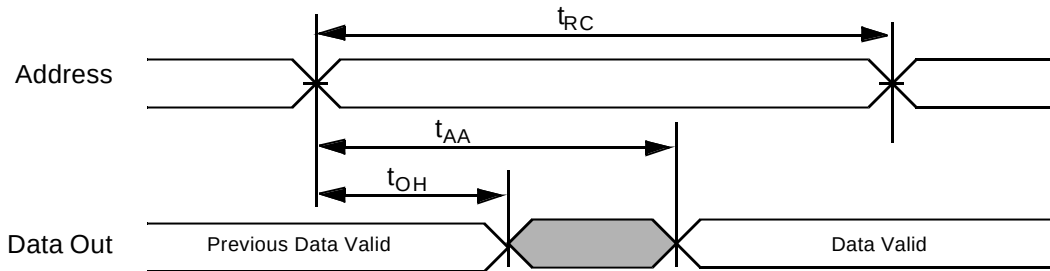
Parameter	Symbol	55ns		70ns		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	55	-	70	-	ns
Address access time	t_{AA}	-	55	-	70	ns
Chip select to output	t_{CO1}, t_{CO2}	-	55	-	70	ns
Output enable to valid output	t_{OE}	-	30	-	35	ns
Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	10	-	ns
Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	20	0	25	ns
Output disable to high-Z output	t_{OHZ}	0	20	0	25	ns
Output hold from address change	t_{OH}	10	-	10	-	ns

WRITE CYCLE ($V_{CC} = 2.7$ to $3.3V$, Gnd = 0V, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

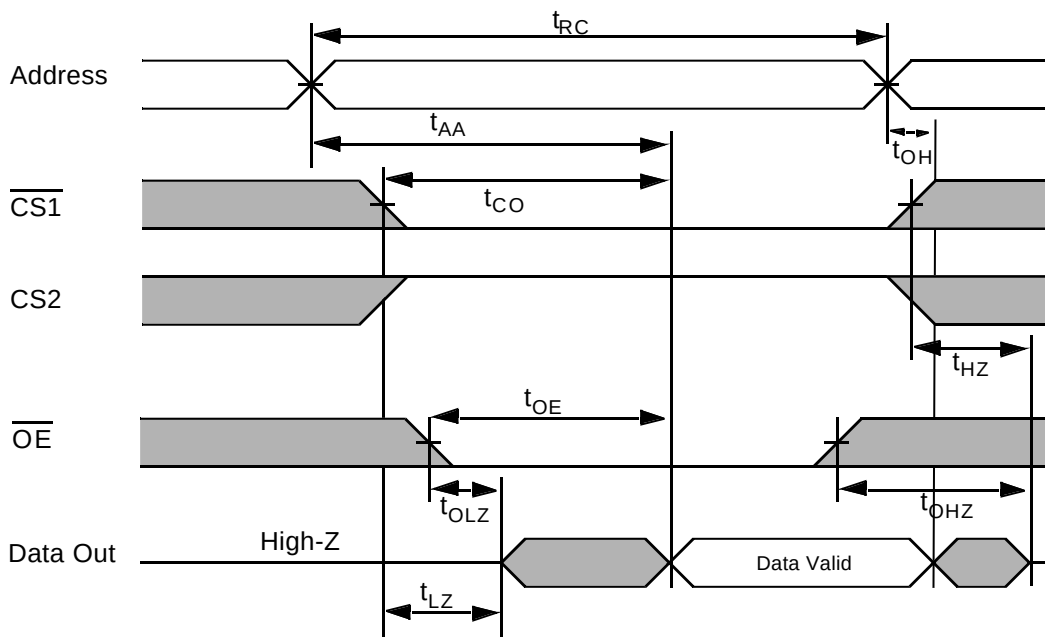
Parameter	Symbol	55ns		70ns		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	55	-	70	-	ns
Chip select to end of write	t_{CW1}, t_{CW2}	45	-	60	-	ns
Address setup time	t_{AS}	0	-	0	-	ns
Address valid to end of write	t_{AW}	45	-	60	-	ns
Write pulse width	t_{WP}	40	-	50	-	ns
Write recovery time	t_{WR}	0	-	0	-	ns
Write to output high-Z	t_{WHZ}	0	20	0	25	ns
Data to write time overlap	t_{DW}	30		30		ns
Data hold from write time	t_{DH}	0	-	0	-	ns
End write to output low-Z	t_{OW}	5	-	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1). (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



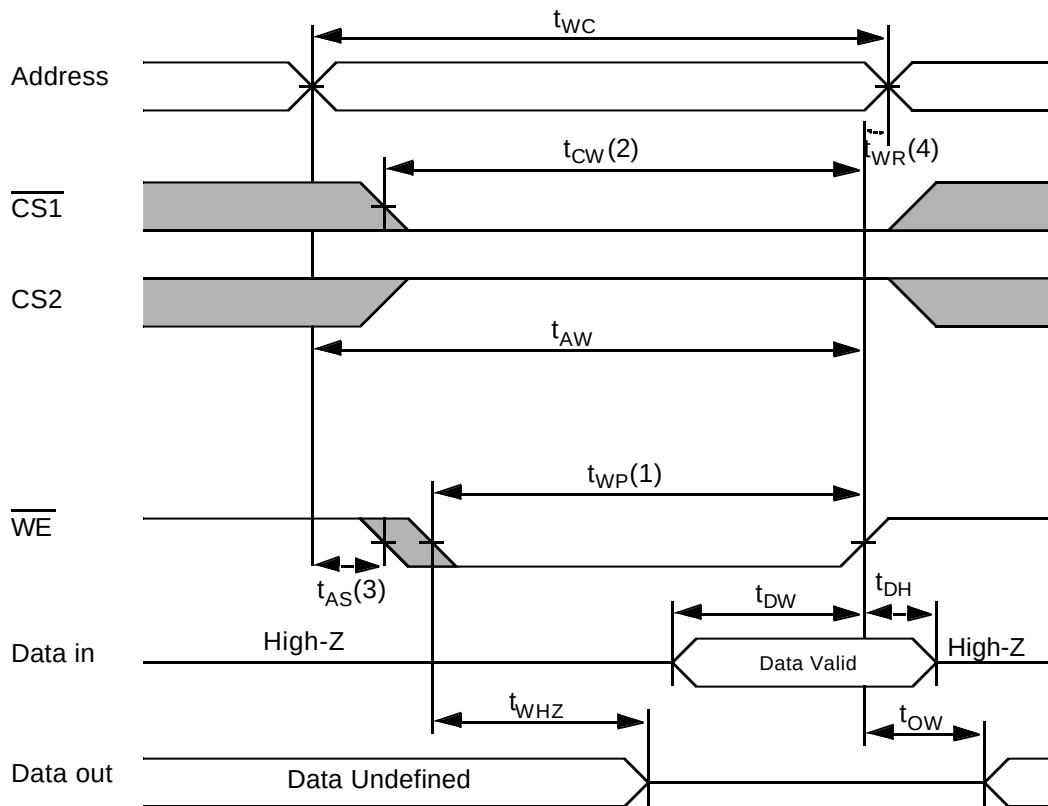
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE} = V_{IH}$)



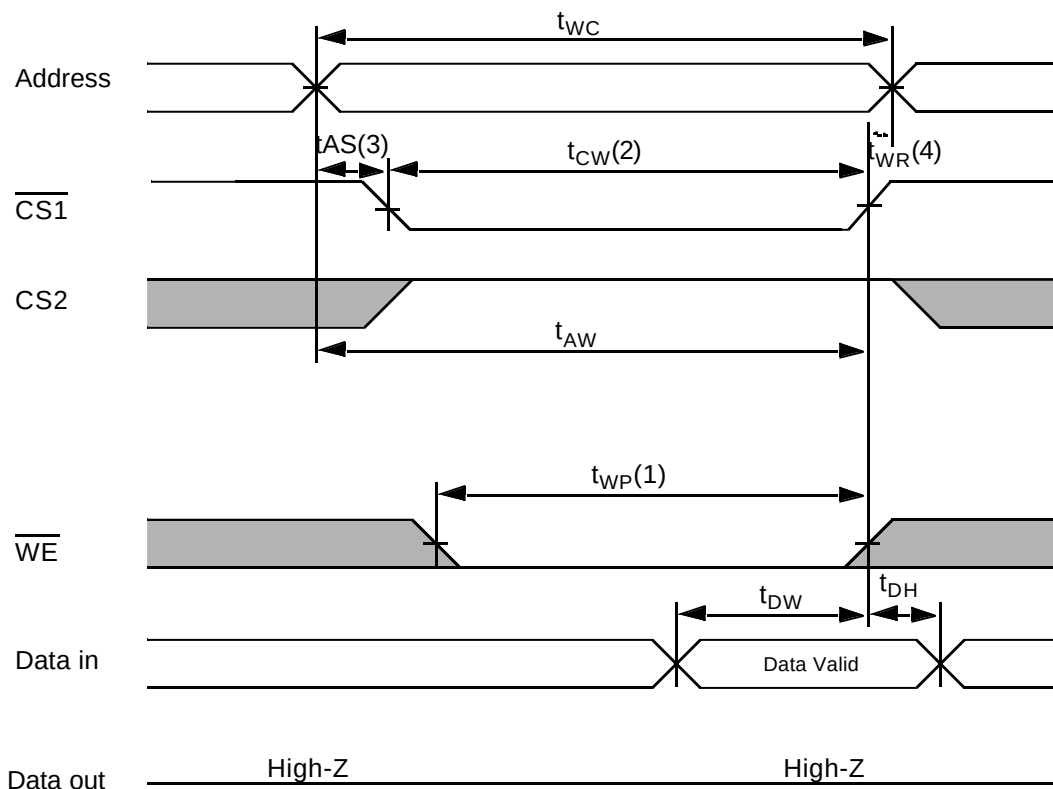
NOTES (READ CYCLE)

- t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

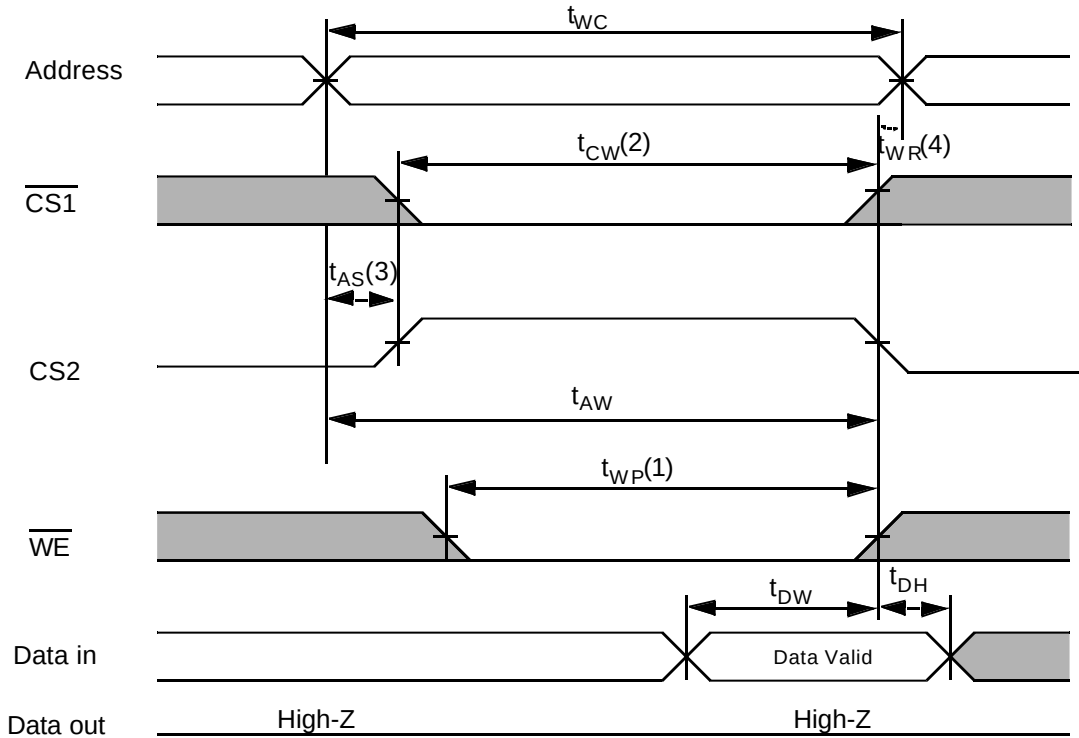
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ CONTROLLED)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, a high CS₂ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ goes high and $\overline{WE}$ goes low. A write ends at the earliest transition when $\overline{CS_1}$ goes high, CS₂ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high.

DATA RETENTION CHARACTERISTICS

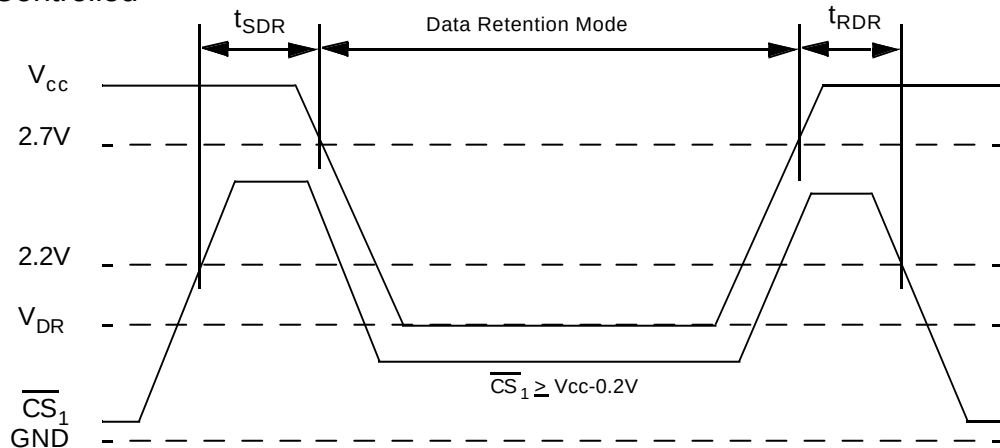
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	I_{SB1} Test Condition (Chip Disabled) ¹⁾	1.5	-	3.3	V
Data Retention Current	I_{DR}	$V_{CC}=1.5V$, I_{SB1} Test Condition (Chip Disabled) ¹⁾	-	0.5	-	μA
Chip Deselect to Data Retention Time	t_{SDR}	See data retention wave form	0	-	-	ns
Operation Recovery Time	t_{RDR}		t_{RC}	-	-	

NOTES

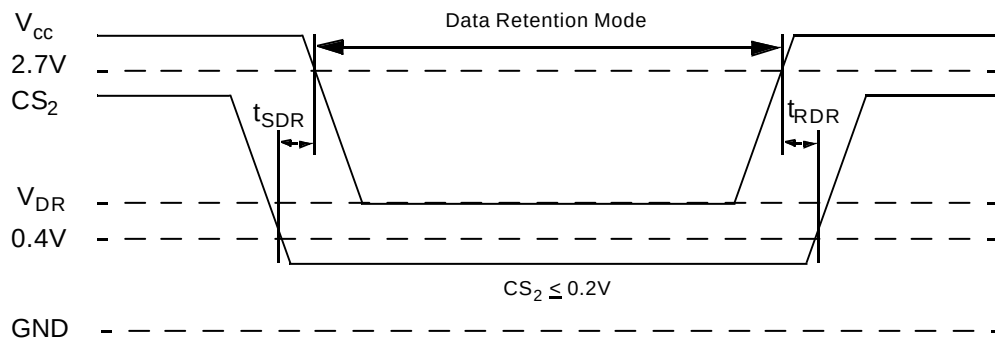
1. See the I_{SB1} measurement condition of datasheet page 4.

DATA RETENTION WAVE FORM

$\overline{CS}_1$ Controlled



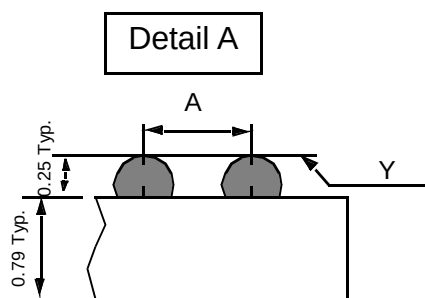
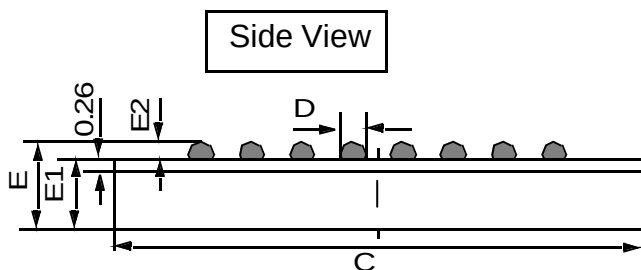
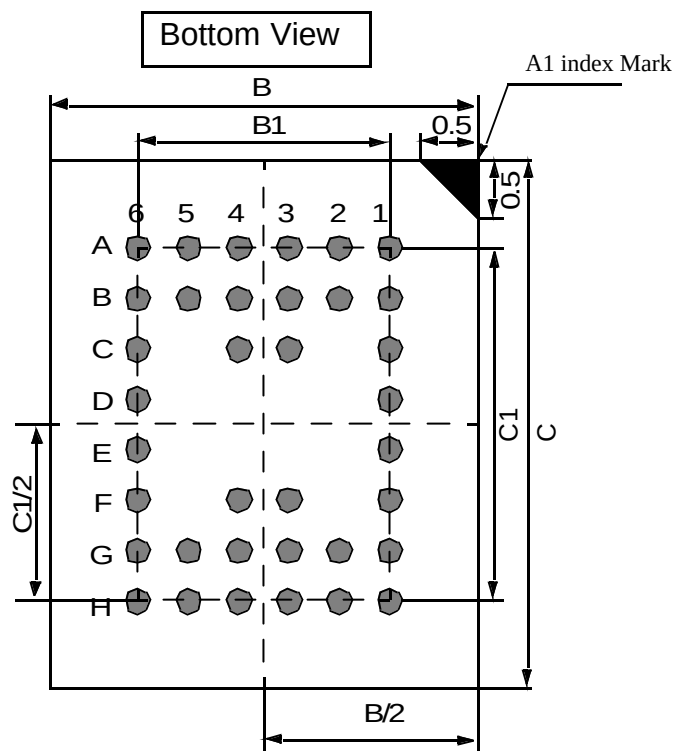
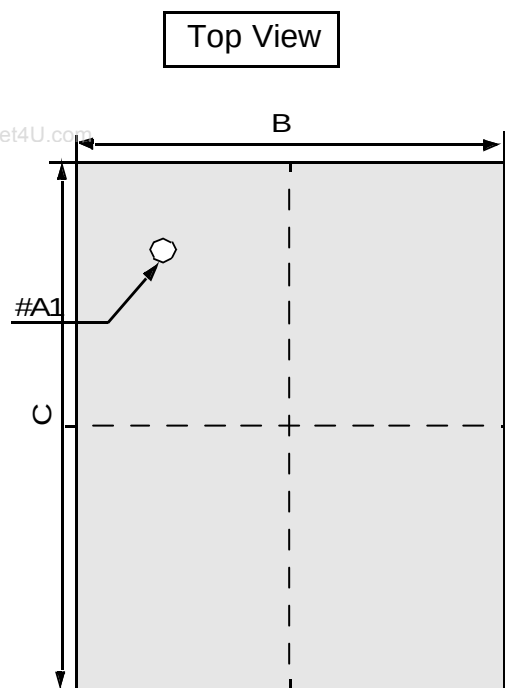
CS_2 Controlled



Unit: millimeters

PACKAGE DIMENSION

36 Ball Fine Pitch BGA (0.75mm ball pitch)

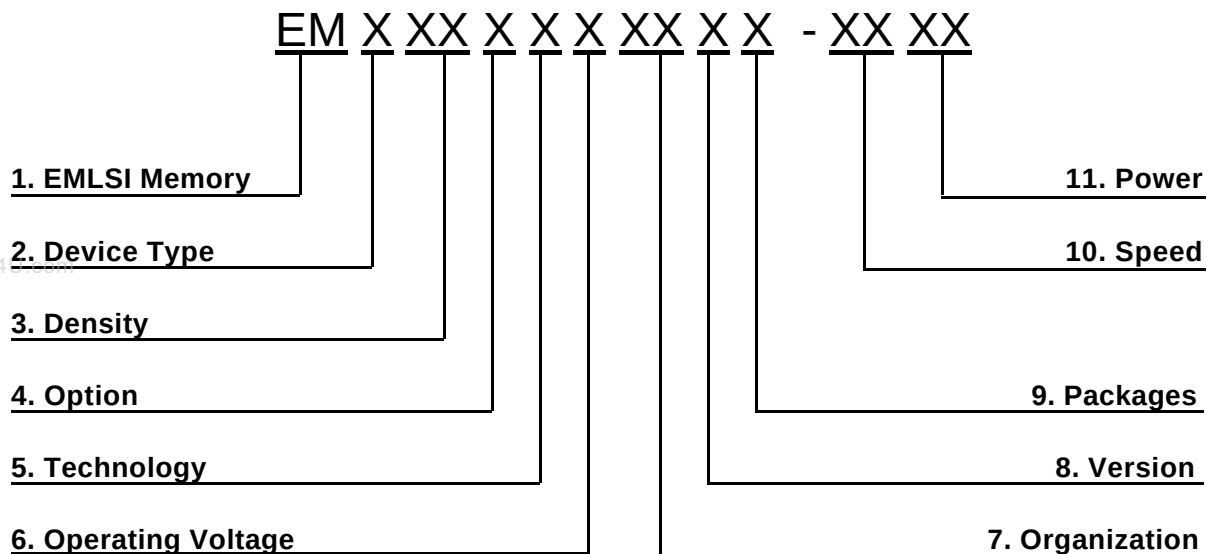


	Min	Typ	Max
A	-	0.75	-
B	5.93	6.00	6.03
B1	-	3.75	-
C	6.93	7.00	7.03
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.04	1.10
E1	-	0.79	-
E2	-	0.25	-
Y	-	-	0.08

NOTES.

1. Bump counts : 36(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)

MEMORY FUNCTION GUIDE



1. Memory Component

2. Device Type

- 6 ----- Low Power SRAM
- 7 ----- STRAM

3. Density

- 1 ----- 1M
- 2 ----- 2M
- 4 ----- 4M
- 8 ----- 8M
- 16 ----- 16M
- 32 ----- 32M
- 64 ----- 64M

4. Option

- 0 ----- Dual CS
- 1 ----- Single CS

5. Technology

- Blank ----- CMOS
- F ----- Full CMOS

6. Operating Voltage

- Blank ----- 5V
- V ----- 3.3V
- U ----- 3.0V
- S ----- 2.5V
- R ----- 2.0V
- P ----- 1.8V

7. Organization

- 8 ----- x8 bit
- 16 ----- x16 bit
- 32 ----- x32 bit

8. Version

- Blank ----- Mother Die
- A ----- First revision
- B ----- Second revision
- C ----- Third revision
- D ----- Fourth revision

9. Package

- Blank ----- Package
- W ----- Wafer

10. Speed

- 45 ----- 45ns
- 55 ----- 55ns
- 70 ----- 70ns
- 85 ----- 85ns
- 10 ----- 100ns
- 12 ----- 120ns

11. Power

- LL ----- Low Low Power
- L ----- Low Power
- S ----- Standard Power
- LF ----- Low Low Power (Pb-free)