

Section 15 Electrical Characteristics

15.1 Absolute Maximum Ratings

Table 15-1 lists the absolute maximum ratings.

Table 15-1 Absolute Maximum Ratings

—Preliminary—

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage (except port 7)	V_{IN}	−0.3 to $V_{CC} + 0.3$	V
Input voltage (port 7)	V_{IN}	−0.3 to $AV_{CC} + 0.3$	V
Reference voltage	V_{REF}	−0.3 to $AV_{CC} + 0.3$	V
Analog power supply voltage	AV_{CC}	−0.3 to +7.0	V
Analog input voltage	V_{AN}	−0.3 to $AV_{CC} + 0.3$	V
Operating temperature	T_{opr}	Regular specifications: −20 to +75	°C
		Wide-range specifications: −40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

15.2 Electrical Characteristics

15.2.1 DC Characteristics

Table 15-2 lists the DC characteristics. Table 15-3 lists the permissible output currents.

Table 15-2 DC Characteristics

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Schmitt trigger input voltages	Port A,	V_T^-	1.0	—	—	V	
	P8 ₀ to P8 ₂ ,	V_T^+	—	—	$V_{CC} \times 0.7$	V	
	PB ₀ to PB ₃	$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, NMI, MD ₁ , MD ₀	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		2.0	—	$AV_{CC} + 0.3$	V	
	Ports 6, 9, P8 ₃ , PB ₄ to PB ₇ , D ₇ to D ₀		2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{\text{RES}}$, $\overline{\text{STBY}}$, MD ₁ , MD ₀	V_{IL}	-0.3	—	0.5	V	
	NMI, EXTAL, ports 6, 7, 9, P8 ₃ , PB ₄ to PB ₇ , D ₇ to D ₀		-0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			3.5	—	—	V	$I_{OH} = -1 \text{ mA}$

Note: * If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open.
 Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^1$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	All output pins (except RESO)	V_{OL}	—	—	0.4	V $I_{OL} = 1.6 \text{ mA}$
	Ports B, A ₁₉ to A ₀		—	—	1.0	V $I_{OL} = 10 \text{ mA}$
	RESO		—	—	0.4	V $I_{OL} = 2.6 \text{ mA}$
Input leakage current	$\overline{\text{STBY}}$, NMI, RES, MD ₁ , MD ₀	$ I_{IN} $	—	—	1.0	μA $V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	Port 7		—	—	1.0	μA $V_{IN} = 0.5 \text{ to } AV_{CC} - 0.5 \text{ V}$
Three-state leakage current (off state)	Ports 6, 8 to B, A ₁₉ to A ₀ , D ₇ to D ₀	$ I_{TS1} $	—	—	1.0	μA $V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	RESO		—	—	10.0	μA
Input capacitance	NMI	C_{IN}	—	—	50	pF $V_{IN} = 0 \text{ V}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$
	All input pins except NMI		—	—	15	
Current dissipation*2	Normal operation	I_{CC}	—	45	60	mA $f = 16 \text{ MHz}$
	Sleep mode		—	32	45	mA $f = 16 \text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA $T_a \leq 50^\circ\text{C}$
			—	—	20.0	μA $50^\circ\text{C} < T_a$

- Notes: 1. If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5 \text{ V}$ and $V_{ILmax} = 0.5 \text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5 \text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3 \text{ V}$.

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	$V_{REF} = 5.0 \text{ V}$
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

- Notes: 1. If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
 2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5 \text{ V}$ and $V_{ILmax} = 0.5 \text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
 3. The values are for $V_{RAM} < V_{CC} < 4.5 \text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3 \text{ V}$.

Conditions: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A,	V_{T-}	$V_{CC} \times 0.2$	—	—	V	
	PB ₀ to PB ₂ ,	V_{T+}	—	—	$V_{CC} \times 0.7$	V	
	PB ₀ to PB ₃	$V_{T+} - V_{T-}$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	RES, STBY, NMI, MD ₁ , MD ₀	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 6, 9, PB ₃ , PB ₄ to PB ₇ , D ₇ to D ₀		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	

Note: * If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Input low voltage	\overline{RES} , \overline{STBY} , MD_1 , MD_0	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 6, 7, 9, PB_3 , PB_4 to PB_7 , D_7 to D_0		-0.3	—	$V_{CC} \times 0.2$	V	$V_{CC} < 4.0\text{ V}$
					0.8	V	$V_{CC} = 4.0\text{ to }5.5\text{ V}$
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu\text{A}$
			$V_{CC} - 1.0$	—	—	V	$I_{OH} = -1\text{ mA}$
Output low voltage	All output pins (except \overline{RESO})	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
	Ports B, A_{19} to A_0		—	—	1.0	V	$V_{CC} \leq 4\text{ V}$, $I_{OL} = 5\text{ mA}$, $4\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $I_{OL} = 10\text{ mA}$
	\overline{RESO}		—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	\overline{STBY} , NMI, \overline{RES} , MD_1 , MD_0	$ I_{IN} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	Port 7		—	—	1.0	μA	$V_{IN} = 0.5\text{ to }AV_{CC} - 0.5\text{ V}$
Three-state leakage current (off state)	Ports 6, 8 to B, A_{19} to A_0 , D_7 to D_0	$ I_{TS1} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	\overline{RESO}		—	—	10.0	μA	

Note: * If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*1$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	NMI	C_{IN}	—	—	50	pF	$V_{IN} = 0\text{ V}$ $f = 1\text{ MHz}$ $T_a = 25^\circ\text{C}$
	All input pins except NMI		—	—	15		
Current dissipation*2	Normal operation	I_{CC}^*4	—	12 (3.0 V)	33.8 (5.5 V)	mA	$f = 8\text{ MHz}$
	Sleep mode		—	8 (3.0 V)	25.0 (5.5 V)	mA	$f = 8\text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	$AV_{CC} = 3.0\text{ V}$
			—	1.2	—	mA	$AV_{CC} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	$V_{REF} = 3.0\text{ V}$
			—	0.3	—	mA	$V_{REF} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

- Notes: 1. If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5\text{ V}$ and $V_{ILmax} = 0.5\text{ V}$ with all output pins unloaded.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7\text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3\text{ V}$.
4. I_{CC} depends on V_{CC} and f as follows:
 $I_{CCmax} = 3.0\text{ (mA)} + 0.7\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [normal mode]
 $I_{CCmax} = 3.0\text{ (mA)} + 0.5\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [sleep mode]

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, PB_0 to PB_2 , PB_0 to PB_3	V_{T^-}	$V_{CC} \times 0.2$	—	—	V
		V_{T^+}	—	—	$V_{CC} \times 0.7$	V
		$V_{T^+} - V_{T^-}$	$V_{CC} \times 0.07$	—	—	V
Input high voltage	\overline{RES} , \overline{STBY} , NMI, MD_1 , MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V
	Ports 6, 9, PB_3 , PB_4 to PB_7 , D_7 to D_0		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V
Input low voltage	\overline{RES} , \overline{STBY} , MD_1 , MD_0	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V
	NMI, EXTAL, ports 6, 7, 9, PB_3 , PB_4 to PB_7 , D_7 to D_0		-0.3	—	$V_{CC} \times 0.2$	V $V_{CC} < 4.0\text{ V}$
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V $I_{OH} = -200\ \mu\text{A}$
			$V_{CC} - 1.0$	—	—	V $I_{OH} = -1\text{ mA}$

Note: * If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Output low voltage	All output pins (except RESO)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
	Ports B, A ₁₉ to A ₀	—	—	1.0	—	V	$V_{CC} \leq 4\text{ V}$ $I_{OL} = 5\text{ mA}$, $4\text{ V} < V_{CC} \leq 5.5\text{ V}$ $I_{OL} = 10\text{ mA}$
	RESO	—	—	0.4	—	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	STBY, NMI, RES, MD ₁ , MD ₀	$ I_{IN} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	Port 7	—	—	1.0	—	μA	$V_{IN} = 0.5\text{ to }AV_{CC} - 0.5\text{ V}$
Three-state leakage current (off state)	Ports 6, 8 to B, A ₁₉ to A ₀ , D ₇ to D ₀	$ I_{TS1} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	RESO	—	—	10.0	—	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$

Note: * If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 15-2 DC Characteristics (cont)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^{*1}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications),
 $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	NMI	C_{IN}	—	—	50	pF	$V_{IN} = 0\text{ V}$ $f = 1\text{ MHz}$ $T_a = 25^{\circ}\text{C}$
	All input pins except NMI		—	—	15		
Current dissipation*2	Normal operation	I_{CC}^{*4}	—	15 (3.0 V)	41.5 (5.5 V)	mA	$f = 10\text{ MHz}$
	Sleep mode		—	10 (3.0 V)	30.5 (5.5 V)	mA	$f = 10\text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA	$T_a \leq 50^{\circ}\text{C}$
			—	—	20.0	μA	$50^{\circ}\text{C} < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	$AV_{CC} = 3.0\text{ V}$
			—	1.2	—	mA	$AV_{CC} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	$V_{REF} = 3.0\text{ V}$
			—	0.3	—	mA	$V_{REF} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

- Notes: 1. If the A/D converter is not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5\text{ V}$ and $V_{ILmax} = 0.5\text{ V}$ with all output pins unloaded.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0\text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3\text{ V}$.
4. I_{CC} depends on V_{CC} and f as follows:
 $I_{CCmax} = 3.0\text{ (mA)} + 0.7\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [normal mode]
 $I_{CCmax} = 3.0\text{ (mA)} + 0.5\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [sleep mode]

Table 15-3 Permissible Output Currents

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports B, A ₁₉ to A ₀	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins including ports B, A ₁₉ to A ₀	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

- Notes: 1. To protect chip reliability, do not exceed the output current values in table 15-3.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 15-1 and 15-2.

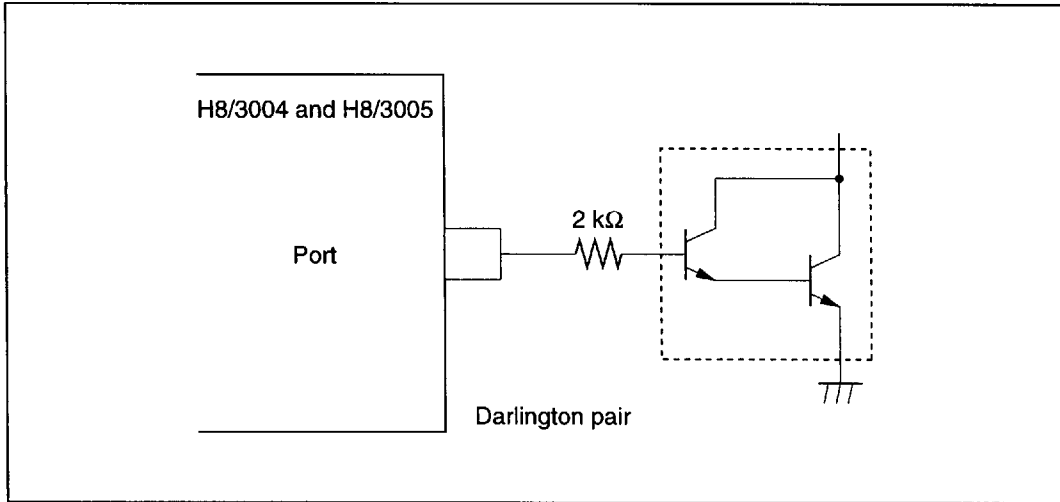


Figure 15-1 Darlington Pair Drive Circuit (Example)

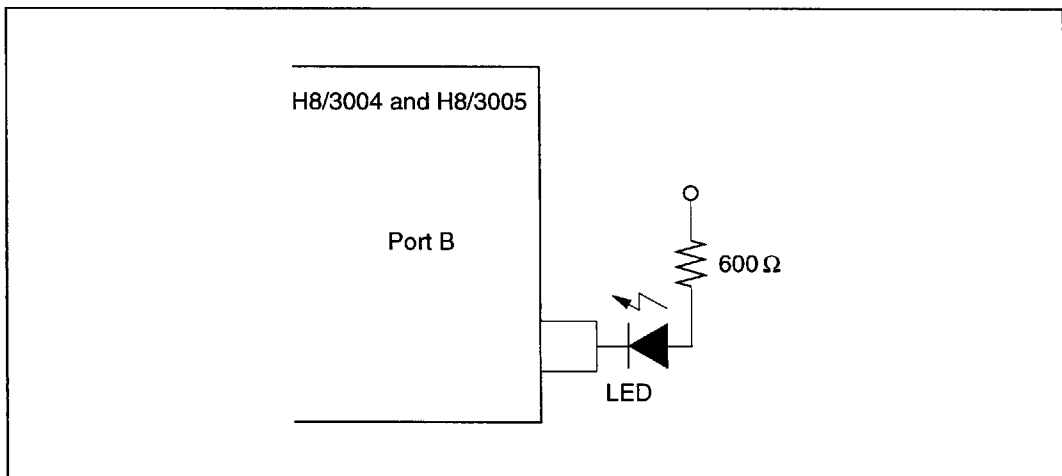


Figure 15-2 LED Drive Circuit (Example)

15.2.2 AC Characteristics

Bus timing parameters are listed in table 15-4. Control signal timing parameters are listed in table 15-5. Timing parameters of the on-chip supporting modules are listed in table 15-6.

Table 15-4 Bus Timing

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions
		8 MHz	Max	10 MHz	Max	16 MHz	Max		
Clock cycle time	t_{CYC}	125	500	100	500	62.5	500	ns	Figure 15-4, Figure 15-5
Clock low pulse width	t_{CL}	40	—	30	—	20	—		
Clock high pulse width	t_{CH}	40	—	30	—	20	—		
Clock rise time	t_{CR}	—	20	—	15	—	10		
Clock fall time	t_{CF}	—	20	—	15	—	10		
Address delay time	t_{AD}	—	60	—	50	—	30		
Address hold time	t_{AH}	25	—	20	—	10	—		
Address strobe delay time	t_{ASD}	—	60	—	40	—	30		
Write strobe delay time	t_{WSD}	—	60	—	50	—	30		
Strobe delay time	t_{SD}	—	60	—	50	—	30		
Write data strobe pulse width 1	t_{WSW1}^*	85	—	60	—	35	—		
Write data strobe pulse width 2	t_{WSW2}^*	150	—	110	—	65	—		
Address setup time 1	t_{AS1}	20	—	15	—	10	—		
Address setup time 2	t_{AS2}	80	—	65	—	40	—		
Read data setup time	t_{RDS}	50	—	35	—	20	—		
Read data hold time	t_{RDH}	0	—	0	—	0	—		

Table 15-4 Bus Timing (cont)

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions
		8 MHz	Max	10 MHz	Max	16 MHz	Max		
Write data delay time	t_{WDD}	—	75	—	75	—	60	ns	Figure 15-4, Figure 15-5
Write data setup time 1	t_{WDS1}	60	—	40	—	15	—		
Write data setup time 2	t_{WDS2}	5	—	-10	—	-5	—		
Write data hold time	t_{WDH}	25	—	20	—	20	—		
Read data access time 1	t_{ACC1*}	—	110	—	100	—	55		
Read data access time 2	t_{ACC2*}	—	230	—	200	—	115		
Read data access time 3	t_{ACC3*}	—	55	—	50	—	25		
Read data access time 4	t_{ACC4*}	—	160	—	150	—	85		
Precharge time	t_{PCH*}	85	—	60	—	40	—		
Wait setup time	t_{WTS}	40	—	40	—	25	—	ns	Figure 15-6
Wait hold time	t_{WTH}	10	—	10	—	5	—		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 78 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 83 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 38 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 70 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 90 \text{ (ns)}\end{aligned}$$

At 10 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 50 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 50 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 50 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 50 \text{ (ns)}\end{aligned}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 39 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 41 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 38 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 23 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 40 \text{ (ns)}\end{aligned}$$

Table 15-5 Control Signal Timing

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions
		8 MHz	Max	10 MHz	Max	16 MHz	Max		
RES setup time	t_{RESS}	200	—	200	—	200	—	ns	Figure 15-7
RES pulse width	t_{RESW}	10	—	10	—	10	—	t_{CYC}	
RESO output delay time	t_{RESD}	—	100	—	100	—	100	ns	Figure 15-8
RESO output pulse width	t_{RESOW}	132	—	132	—	132	—	t_{CYC}	
NMI setup time (NMI, \overline{IRQ}_4 to \overline{IRQ}_0)	t_{NMIS}	200	—	200	—	150	—	ns	Figure 15-9
NMI hold time (NMI, \overline{IRQ}_4 to \overline{IRQ}_0)	t_{NMIH}	10	—	10	—	10	—		
Interrupt pulse width (NMI, \overline{IRQ}_4 to \overline{IRQ}_0 when exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t_{OSC1}	20	—	20	—	20	—	ms	Figure 15-10
Clock oscillator settling time in software standby (crystal)	t_{OSC2}	8	—	8	—	8	—	ms	Figure 14-1

Table 15-6 Timing of On-Chip Supporting Modules

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions	
		8 MHz	Max	10 MHz	Max	16 MHz	Max			
ITU	Timer output delay time	t_{TOD}	—	100	—	100	—	100	ns	Figure 15-12
	Timer input setup time	t_{TICS}	50	—	50	—	50	—		
	Timer clock input setup time	t_{TCKS}	50	—	50	—	50	—	t_{cyc}	Figure 15-13
	Timer clock pulse width	t_{TCKWH}	1.5	—	1.5	—	1.5	—		
	Timer clock pulse width	t_{TCKWL}	2.5	—	2.5	—	2.5	—		
SCI	Input clock cycle	Asynchronous	t_{SCYC}	4	—	4	—	4	—	Figure 15-14
		Synchronous	t_{SCYC}	6	—	6	—	6		
	Input clock rise time	t_{SCKr}	—	1.5	—	1.5	—	1.5	t_{scyc}	
	Input clock fall time	t_{SCKf}	—	1.5	—	1.5	—	1.5		
	Input clock pulse width	t_{SCKw}	0.4	0.6	0.4	0.6	0.4	0.6		

Table 15-6 Timing of On-Chip Supporting Modules (cont)

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C		Unit	Test Conditions	
		8 MHz	10 MHz	10 MHz	16 MHz	16 MHz				
SCI	Transmit data delay time	t_{TXD}	—	100	—	100	—	100	ns	Figure 15-15
	Receive data setup time (synchronous)	t_{RXS}	100	—	100	—	100	—		
	Receive data hold time (synchronous clock input)	t_{RXH}	100	—	100	—	100	—		
	Receive data hold time (synchronous clock output)	t_{RXH}	0	—	0	—	0	—		
Ports	Output data delay time	t_{PWD}	—	100	—	100	—	100	ns	Figure 15-11
	Input data setup time (synchronous)	t_{PRS}	50	—	50	—	50	—		
	Input data hold time (synchronous)	t_{PRH}	50	—	50	—	50	—		

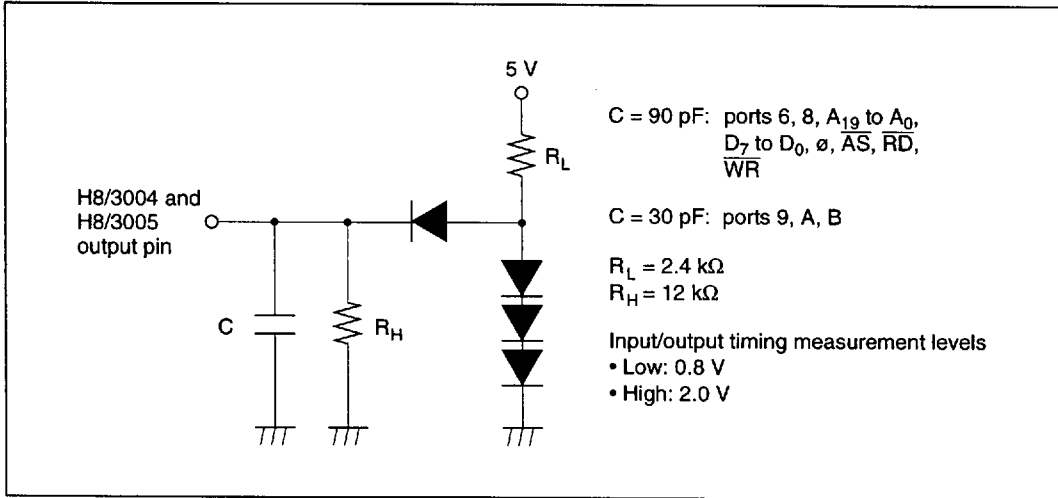


Figure 15-3 Output Load Circuit

15.2.3 A/D Conversion Characteristics

Table 15-7 lists the A/D conversion characteristics.

Table 15-7 A/D Converter Characteristics

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{REF} = 3.0\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }10\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 2\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Condition A			Condition B			Condition C			Unit
	8 MHz			10 MHz			16 MHz			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	13.4	—	—	8.4	μs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10^1	—	—	10^1	—	—	10^4	k Ω
	—	—	5^2	—	—	5^3	—	—	5^5	
Nonlinearity error	—	—	± 6.0	—	—	± 6.0	—	—	± 3.0	LSB
Offset error	—	—	± 4.0	—	—	± 4.0	—	—	± 2.0	LSB
Full-scale error	—	—	± 4.0	—	—	± 4.0	—	—	± 2.0	LSB
Quantization error	—	—	± 0.5	—	—	± 0.5	—	—	± 0.5	LSB
Absolute accuracy	—	—	± 8.0	—	—	± 8.0	—	—	± 4.0	LSB

- Notes: 1. The value is for $4.0 \leq AV_{CC} \leq 5.5$.
2. The value is for $2.7 \leq AV_{CC} < 4.0$.
3. The value is for $3.0 \leq AV_{CC} < 4.0$.
4. The value is for $\phi \leq 12\text{ MHz}$.
5. The value is for $\phi > 12\text{ MHz}$.

15.3 Operational Timing

This section shows timing diagrams.

15.3.1 Bus Timing

Bus timing is shown as follows:

- Basic bus cycle: two-state access

Figure 15-4 shows the timing of the external two-state access cycle.

- Basic bus cycle: three-state access

Figure 15-5 shows the timing of the external three-state access cycle.

- Basic bus cycle: three-state access with one wait state

Figure 15-6 shows the timing of the external three-state access cycle with one wait state inserted.

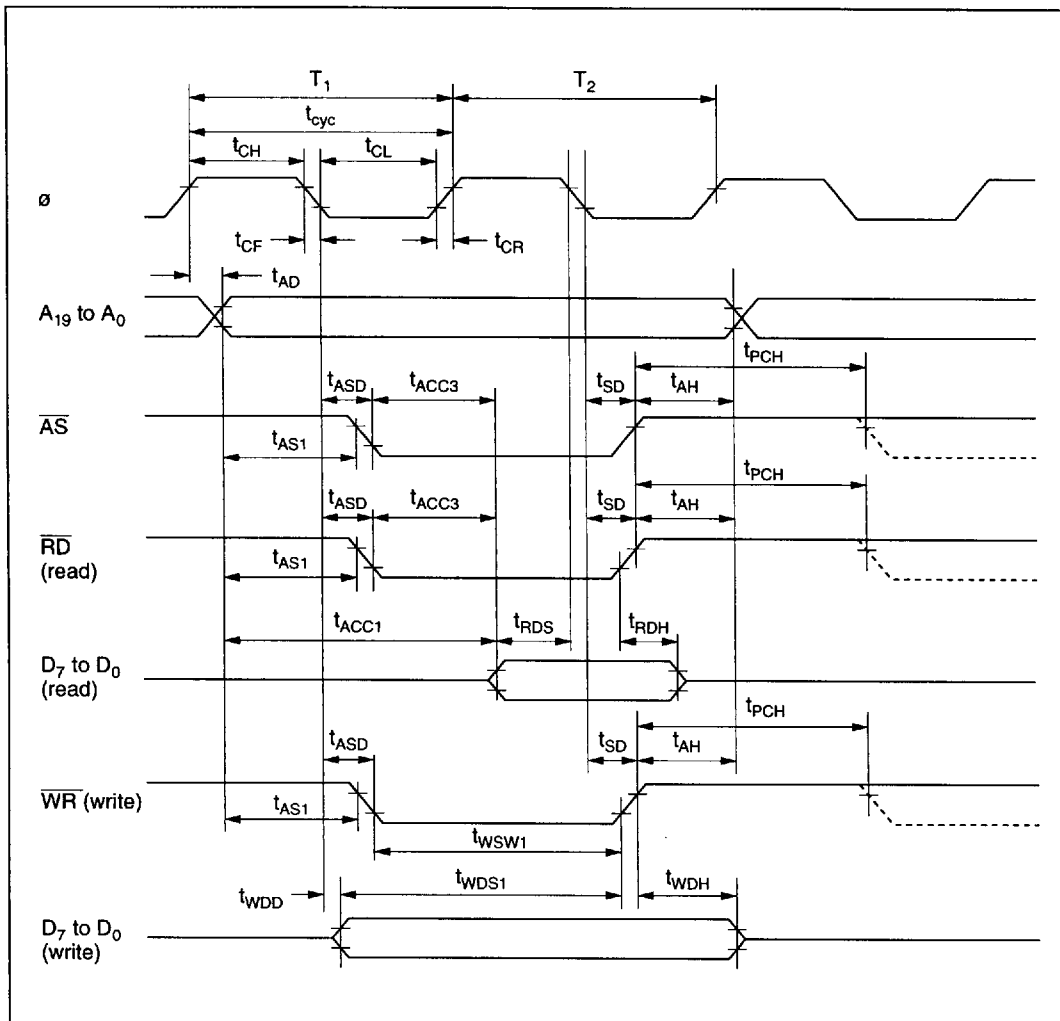


Figure 15-4 Basic Bus Cycle: Two-State Access

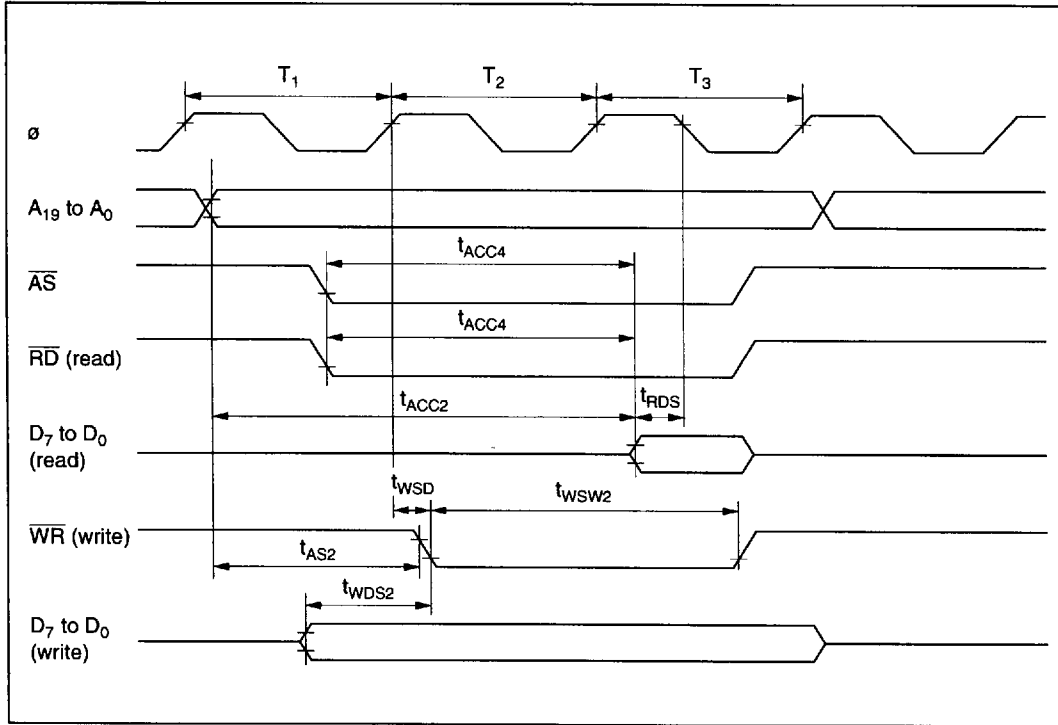


Figure 15-5 Basic Bus Cycle: Three-State Access

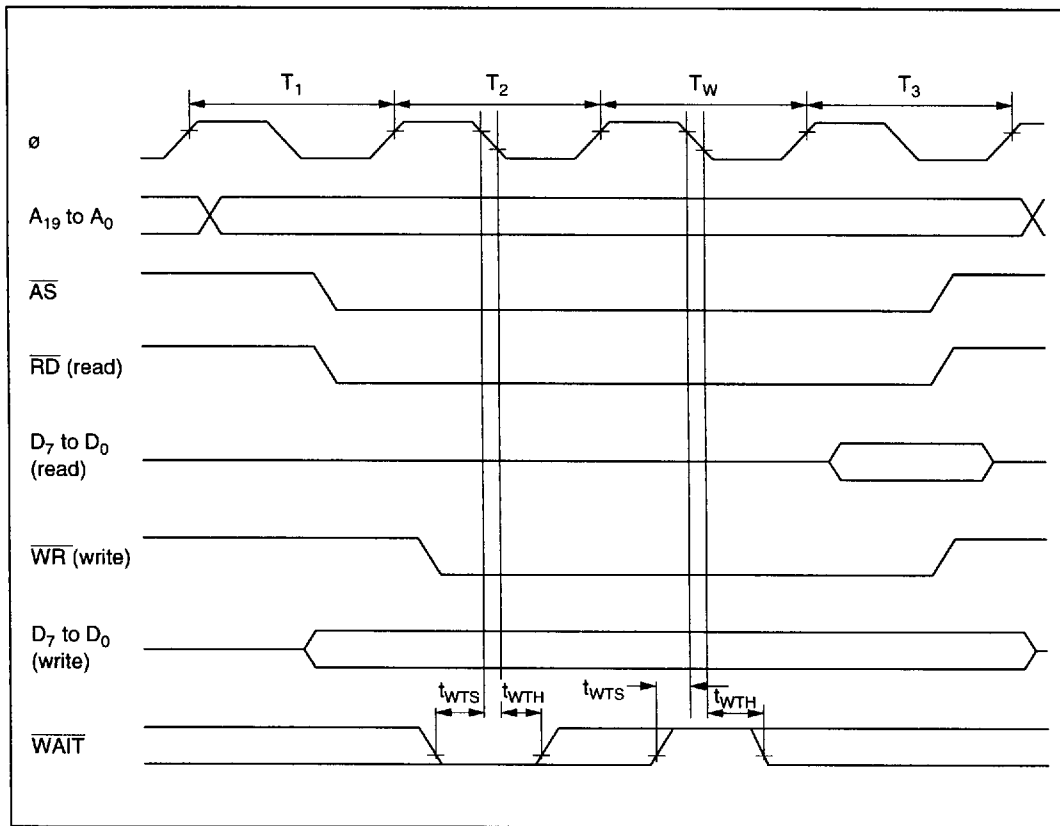


Figure 15-6 Basic Bus Cycle: Three-State Access with One Wait State

15.3.2 Control Signal Timing

Control signal timing is shown as follows:

- Reset input timing

Figure 15-7 shows the reset input timing.

- Reset output timing

Figure 15-8 shows the reset output timing.

- Interrupt input timing

Figure 15-9 shows the input timing for NMI and \overline{IRQ}_4 to \overline{IRQ}_0 .

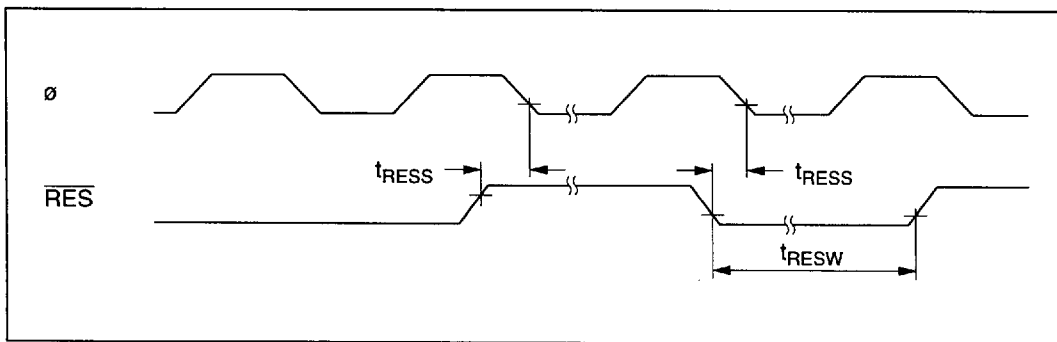


Figure 15-7 Reset Input Timing

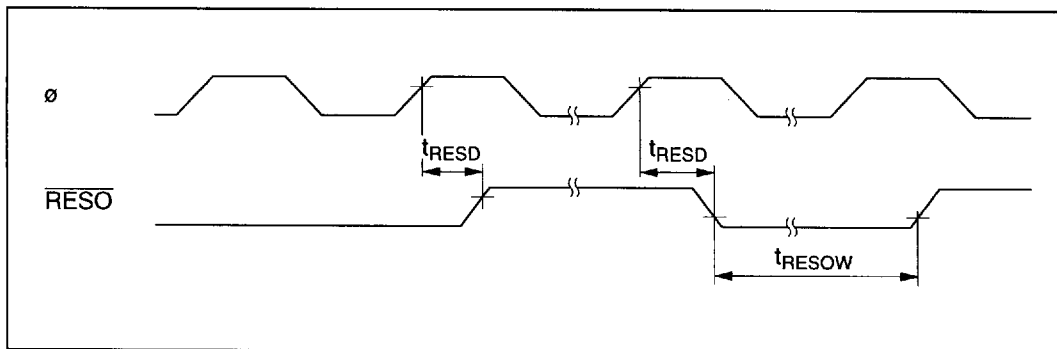


Figure 15-8 Reset Output Timing

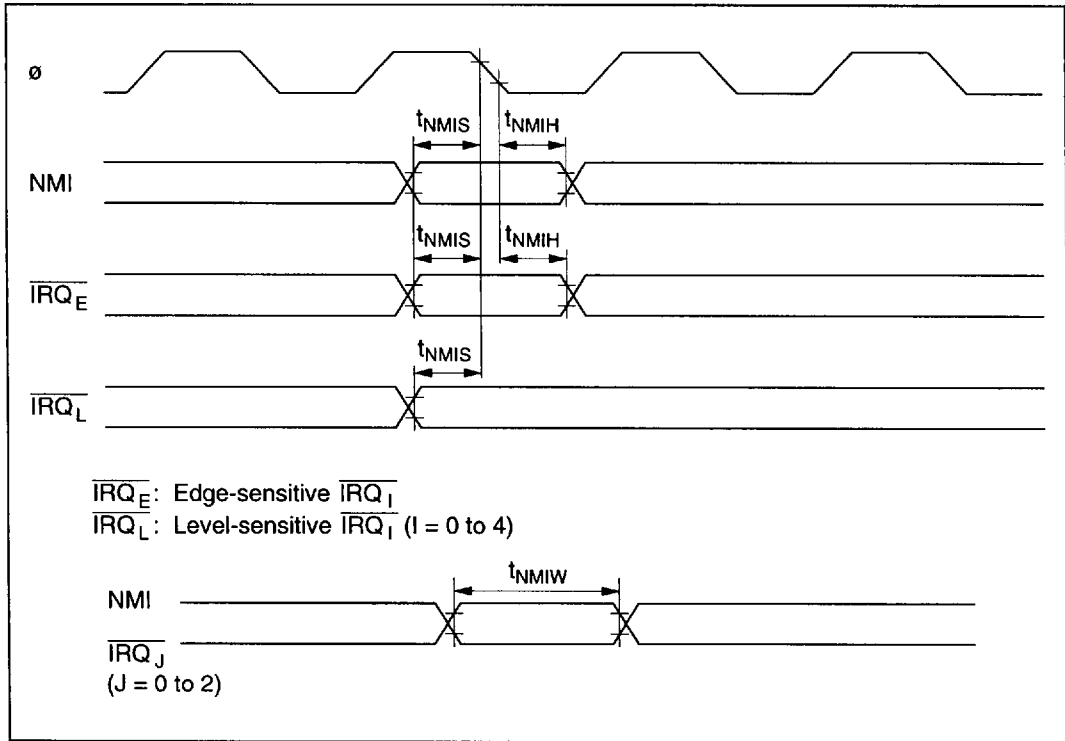


Figure 15-9 Interrupt Input Timing

15.3.3 Clock Timing

Clock timing is shown as follows:

- Oscillator settling timing

Figure 15-10 shows the oscillator settling timing.

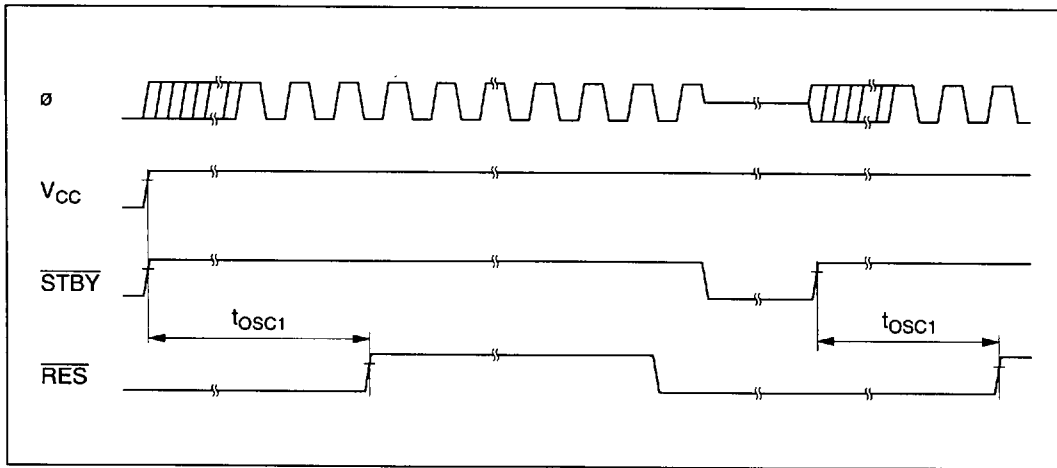


Figure 15-10 Oscillator Settling Timing

15.3.4 I/O Port Timing

I/O port timing is shown as follows.

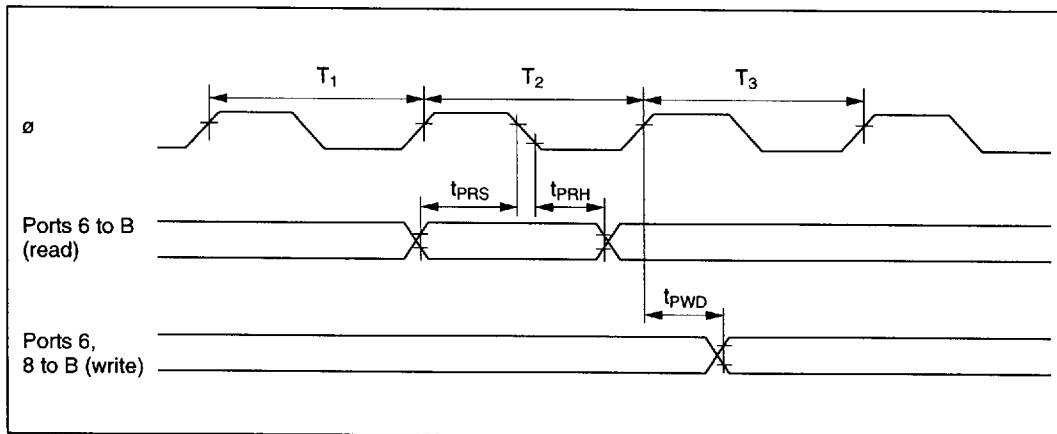


Figure 15-11 I/O Port Input/Output Timing

15.3.5 ITU Timing

ITU timing is shown as follows:

- ITU input/output timing

Figure 15-12 shows the ITU input/output timing.

- ITU external clock input timing

Figure 15-13 shows the ITU external clock input timing.

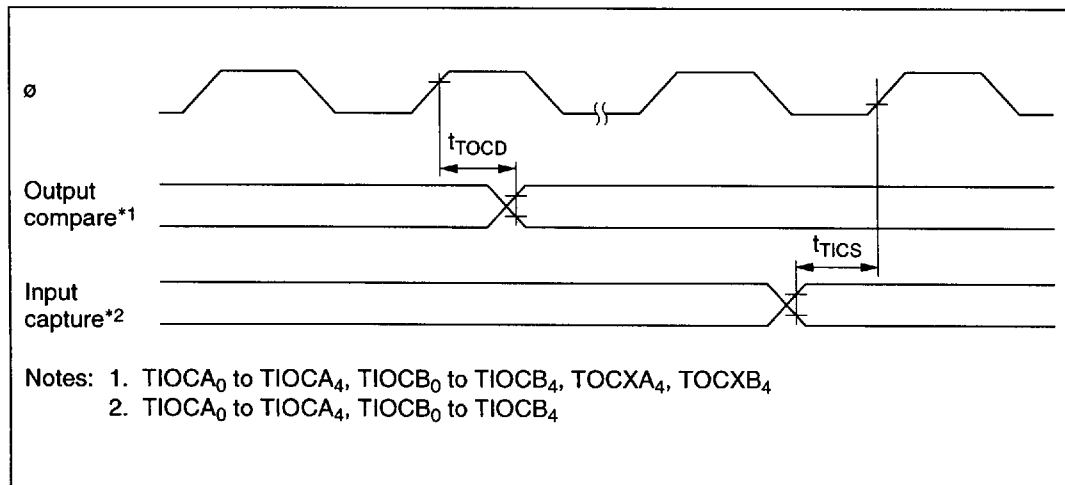


Figure 15-12 ITU Input/Output Timing

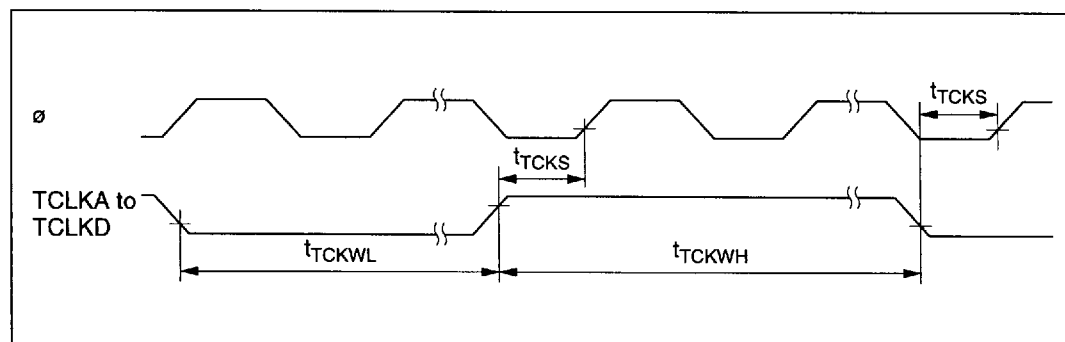


Figure 15-13 ITU Clock Input Timing

15.3.6 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing

Figure 15-14 shows the SCI input clock timing.

- SCI input/output timing (synchronous mode)

Figure 15-15 shows the SCI input/output timing in synchronous mode.

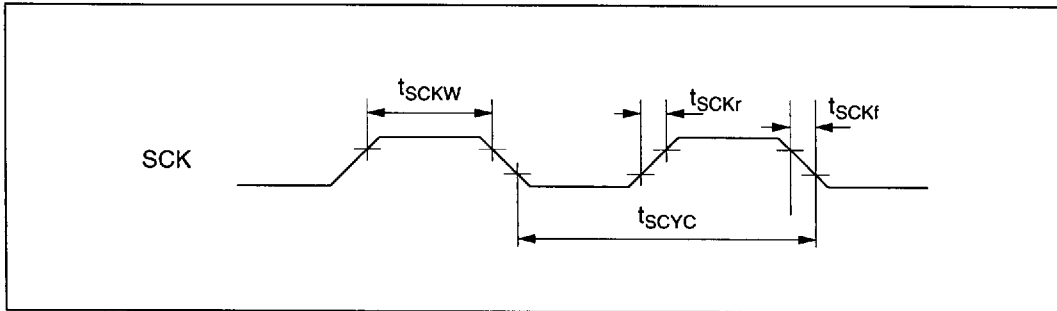


Figure 15-14 SCK Input Clock Timing

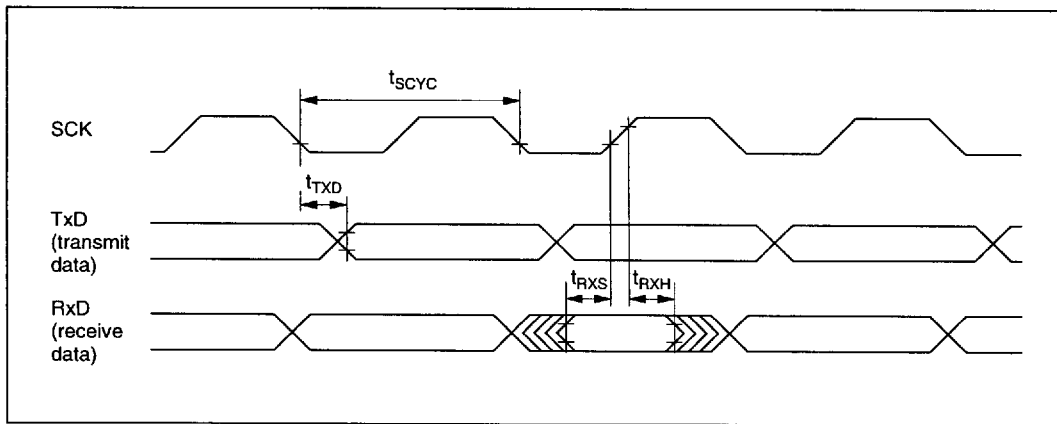


Figure 15-15 SCI Input/Output Timing in Synchronous Mode