

Section 21 Electrical Characteristics

—Preliminary—

21.1 Absolute Maximum Ratings

Table 21-1 lists the absolute maximum ratings.

Table 21-1 Absolute Maximum Ratings

—Preliminary—

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Programming voltage	HD6473048 V_{PP}	−0.3 to +13.5	V
	HD64F3048	−0.3 to +13.0	V
Input voltage (except for MD ₂ and port 7)	V_{in}	−0.3 to $V_{CC} + 0.3$	V
Input voltage (MD ₂)	HD6473048, HD6433048, HD6433047, HD6433045, HD6433044	V_{in}	−0.3 to $V_{CC} + 0.3$
	HD64F3048		−0.3 to +13.0
Input voltage (port 7)	V_{in}	−0.3 to $AV_{CC} + 0.3$	V
Reference voltage	V_{REF}	−0.3 to $AV_{CC} + 0.3$	V
Analog power supply voltage	AV_{CC}	−0.3 to +7.0	V
Analog input voltage	V_{AN}	−0.3 to $AV_{CC} + 0.3$	V
Operating temperature	T_{opr}	Regular specifications: −20 to +75	°C
		Wide-range specifications: −40 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.
Particularly, insure that peak overshoot at the V_{PP} and MD₂ pins does not exceed 13 V.

21.2 Electrical Characteristics of Masked ROM and PROM Versions

21.2.1 DC Characteristics

Table 21-2 lists the DC characteristics. Table 21-3 lists the permissible output currents.

Table 21-2 DC Characteristics

—Preliminary—

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V}$ to AV_{CC} ,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A,	V_{T^-}	1.0	—	—	V	
	P8 ₀ to P8 ₂ ,	V_{T^+}	—	—	$V_{CC} \times 0.7$	V	
	PB ₀ to PB ₃	$V_{T^+} - V_{T^-}$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD ₂ to MD ₀	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		2.0	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD ₂ to MD ₀	V_{IL}	-0.3	—	0.5	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		-0.3	—	0.8	V	
Output high voltage	All output pins (except $\overline{RES0}$)	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\text{ }\mu\text{A}$
			3.5	—	—	V	$I_{OH} = -1\text{ mA}$
Output low voltage	All output pins (except $\overline{RES0}$)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
	Ports 1, 2, 5, and B		—	—	1.0	V	$I_{OL} = 10\text{ mA}$
	$\overline{RES0}$		—	—	0.4	V	$I_{OL} = 2.6\text{ mA}$

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-2 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^{*1}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{\text{STBY}}$, NMI, $\overline{\text{RES}}$, MD ₂ to MD ₀	—	—	1.0	μA	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	Port 7	—	—	1.0	μA	$V_{IN} = 0.5 \text{ to } AV_{CC} - 0.5 \text{ V}$
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	—	—	1.0	μA	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	$\overline{\text{RESO}}$	—	—	10.0	μA	
Input pull-up current	Ports 2, 4, and 5	— I_P	50	—	300	μA $V_{IN} = 0 \text{ V}$
Input capacitance	NMI	C_{IN}	—	—	50	pF $V_{IN} = 0 \text{ V}$
	All input pins except NMI	—	—	—	15	pF $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$
Current dissipation*2	Normal operation	I_{CC}	—	50	65	mA $f = 16 \text{ MHz}$
			—	55	75	mA $f = 18 \text{ MHz}$
	Sleep mode		—	35	50	mA $f = 16 \text{ MHz}$
			—	40	55	mA $f = 18 \text{ MHz}$
	Module standby mode*4		—	20	25	mA $f = 16 \text{ MHz}$
			—	25	27	mA $f = 18 \text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA $T_a \leq 50^\circ\text{C}$
			—	—	20.0	μA $50^\circ\text{C} < T_a$

- Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5 \text{ V}$ and $V_{ILmax} = 0.5 \text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5 \text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3 \text{ V}$.
4. Module standby current values apply in sleep mode with all modules halted.

Table 21-2 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D and D/A conversion		—	1.2	2.0	mA	
	Idle		—	0.01	5.0	μA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	$V_{REF} = 5.0\text{ V}$
	During A/D and D/A conversion		—	1.3	3.0	mA	
	Idle		—	0.01	5.0	μA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-2 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, P8 ₀ to P8 ₂ , PB ₀ to PB ₃	V_{T^-}	$V_{CC} \times 0.2$	—	—	V	
		V_{T^+}	—	—	$V_{CC} \times 0.7$	V	
		$V_{T^+} - V_{T^-}$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	RES, STBY, NMI, MD ₂ to MD ₀	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	RES, STBY, MD ₂ to MD ₀	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		-0.3	—	$V_{CC} \times 0.2$	V	$V_{CC} < 4.0 \text{ V}$
					0.8	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$
Output high voltage	All output pins (except RESO)	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			$V_{CC} - 1.0$	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low voltage	All output pins (except RESO)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
	Ports 1, 2, 5, and B		—	—	1.0	V	$V_{CC} \leq 4 \text{ V}$ $I_{OL} = 5 \text{ mA}$, $4 \text{ V} < V_{CC} \leq 5.5 \text{ V}$ $I_{OL} = 10 \text{ mA}$
	RESO		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
Input leakage current	STBY, NMI, RES, MD ₂ to MD ₀	$ I_{IN} $	—	—	1.0	μA	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$
	Port 7		—	—	1.0	μA	$V_{IN} = 0.5 \text{ to } AV_{CC} - 0.5 \text{ V}$

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-2 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^{*1}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications),
 $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$ I_{TS1} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	$\overline{\text{RESO}}$		—	—	10.0	μA	
Input pull-up current	Ports 2, 4, and 5	$-I_p$	10	—	300	μA	$V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{IN} = 0\text{ V}$
Input capacitance	NMI	C_{IN}	—	—	50	pF	$V_{IN} = 0\text{ V}$ $f = 1\text{ MHz}$ $T_a = 25^{\circ}\text{C}$
	All input pins except NMI		—	—	15		
Current dissipation ^{*2}	Normal operation	I_{CC}^{*4}	—	12 (3.0 V)	35 (5.5 V)	mA	$f = 8\text{ MHz}$
			—	20 (3.3 V)	55 (5.5 V)	mA	$f = 13\text{ MHz}$ ($V_{CC} = 3.15\text{ V to }5.5\text{ V}$)
			—	8 (3.0 V)	25 (5.5 V)	mA	$f = 8\text{ MHz}$
			—	12 (3.3 V)	40 (5.5 V)	mA	$f = 13\text{ MHz}$ ($V_{CC} = 3.15\text{ V to }5.5\text{ V}$)
	Module standby mode ^{*5}		—	5 (3.0 V)	14 (5.5 V)	mA	$f = 8\text{ MHz}$
			—	7 (3.3 V)	20 (5.5 V)	mA	13 MHz ($V_{CC} = 3.15\text{ V to }5.5\text{ V}$)
	Standby mode ^{*3}		—	0.01	5.0	μA	$T_a \leq 50^{\circ}\text{C}$
			—	—	20.0	μA	$50^{\circ}\text{C} < T_a$

- Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5\text{ V}$ and $V_{ILmax} = 0.5\text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7\text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3\text{ V}$.
4. I_{CC} depends on V_{CC} and f as follows:
 $I_{CCmax} = 3.0\text{ (mA)} + 0.75\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [normal mode]
 $I_{CCmax} = 3.0\text{ (mA)} + 0.55\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [sleep mode]
 $I_{CCmax} = 3.0\text{ (mA)} + 0.25\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [module standby mode]
5. Module standby current values apply in sleep mode with all modules halted.

Table 21-2 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI _{CC}	—	0.4	1.0	mA	AV _{CC} = 3.0 V
			—	1.2	—	mA	AV _{CC} = 5.0 V
	During A/D and D/A conversion		—	0.4	1.0	mA	AV _{CC} = 3.0 V
			—	1.2	—	mA	AV _{CC} = 5.0 V
	Idle		—	0.01	5.0	μA	DASTE = 0
Reference current	During A/D conversion	AI _{CC}	—	0.2	0.4	mA	V _{REF} = 3.0 V
			—	0.3	—	mA	V _{REF} = 5.0 V
	During A/D and D/A conversion		—	0.8	2.0	mA	V _{REF} = 3.0 V
			—	1.3	—	mA	V _{REF} = 5.0 V
	Idle		—	0.01	5.0	μA	DASTE = 0
RAM standby voltage		V _{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-3 Permissible Output Currents

—Preliminary—

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications),
 $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 5, and B	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins in ports 1, 2, 5, and B	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

- Notes: 1. To protect chip reliability, do not exceed the output current values in table 21-3.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21-1 and 21-2.

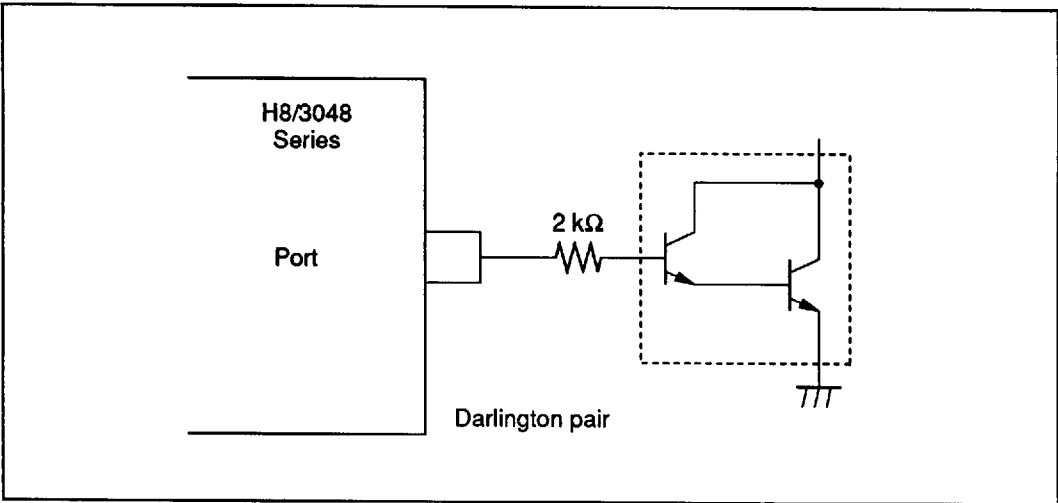


Figure 21-1 Darlington Pair Drive Circuit (Example)

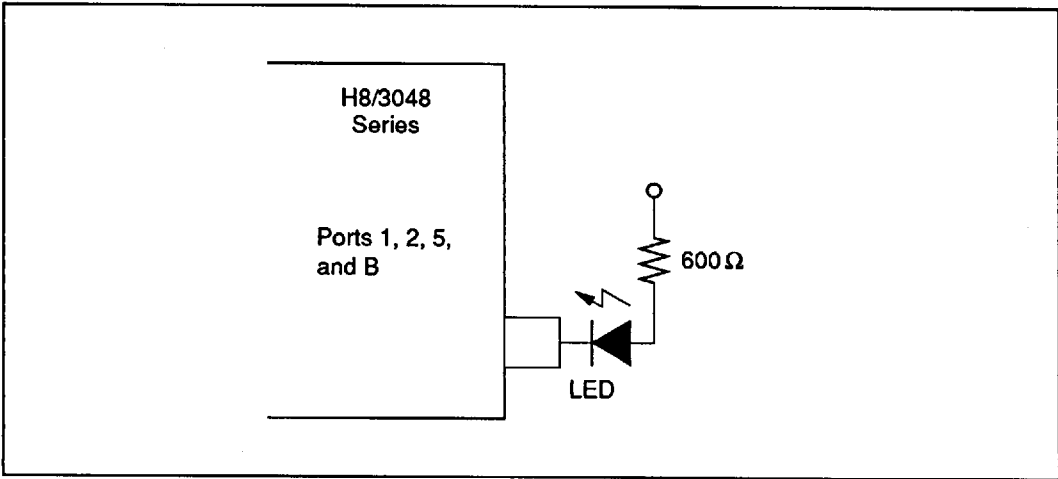


Figure 21-2 LED Drive Circuit (Example)

21.2.2 AC Characteristics

Bus timing parameters are listed in table 21-4. Refresh controller bus timing parameters are listed in table 21-5. Control signal timing parameters are listed in table 21-6. Timing parameters of the on-chip supporting modules are listed in table 21-7.

Table 21-4 Bus Timing (1)

—Preliminary—

Condition A: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 8 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 3.15 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 3.15 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 13 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 18 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions
		8 MHz		13 MHz		16 MHz		18 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock cycle time	t _{CYC}	125	1000	76.9	1000	62.5	1000	55.5	1000	ns	Figure 21-7 Figure 21-8
Clock pulse low width	t _{CL}	40	—	20	—	20	—	17	—		
Clock pulse high width	t _{CH}	40	—	20	—	20	—	17	—		
Clock rise time	t _{CR}	—	20	—	15	—	10	—	10		
Clock fall time	t _{CF}	—	20	—	15	—	10	—	10		
Address delay time	t _{AD}	—	60	—	50	—	30	—	25		
Address hold time	t _{AH}	25	—	20	—	10	—	10	—		
Address strobe delay time	t _{ASD}	—	60	—	50	—	30	—	25		
Write strobe delay time	t _{WSD}	—	60	—	50	—	30	—	25		
Strobe delay time	t _{SD}	—	60	—	50	—	30	—	25		
Write data strobe pulse width 1	t _{WSW1*}	85	—	40	—	35	—	32	—		
Write data strobe pulse width 2	t _{WSW2*}	150	—	90	—	65	—	62	—		
Address setup time 1	t _{AS1}	20	—	15	—	10	—	10	—		
Address setup time 2	t _{AS2}	80	—	45	—	40	—	38	—		
Read data setup time	t _{RDS}	50	—	30	—	20	—	15	—		
Read data hold time	t _{RDH}	0	—	0	—	0	—	0	—		

Table 21-4 Bus Timing (cont)

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Write data delay time	t _{WDD}	—	75	—	75	—	60	—	55	ns	Figure 21-7, Figure 21-8
Write data setup time 1	t _{WDS1}	60	—	20	—	15	—	10	—		
Write data setup time 2	t _{WDS2}	5	—	–10	—	–5	—	–10	—		
Write data hold time	t _{WDH}	25	—	15	—	20	—	20	—		
Read data access time 1	t _{ACC1*}	—	120	—	60	—	60	—	50		
Read data access time 2	t _{ACC2*}	—	240	—	140	—	120	—	105		
Read data access time 3	t _{ACC3*}	—	70	—	30	—	30	—	20		
Read data access time 4	t _{ACC4*}	—	180	—	100	—	95	—	80		
Precharge time	t _{PCH*}	85	—	55	—	45	—	40	—		
Wait setup time	t _{WTS}	40	—	40	—	25	—	25	—	ns	Figure 21-9
Wait hold time	t _{WTH}	10	—	10	—	5	—	5	—		
Bus request setup ime	t _{BRQS}	40	—	40	—	40	—	40	—	ns	Figure 21-21
Bus acknowledge delay time 1	t _{BACD1}	—	60	—	50	—	30	—	30		
Bus acknowledge delay time 2	t _{BACD2}	—	60	—	50	—	30	—	30		
Bus-floating time	t _{BZD}	—	70	—	70	—	40	—	40		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{ACC1} &= 1.5 \times t_{CYC} - 68 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{CYC} - 40 \text{ (ns)} \\ t_{ACC2} &= 2.5 \times t_{CYC} - 73 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{CYC} - 38 \text{ (ns)} \\ t_{ACC3} &= 1.0 \times t_{CYC} - 55 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{CYC} - 40 \text{ (ns)} \\ t_{ACC4} &= 2.0 \times t_{CYC} - 70 \text{ (ns)} \end{aligned}$$

At 13 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{ACC1} &= 1.5 \times t_{CYC} - 56 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{CYC} - 37 \text{ (ns)} \\ t_{ACC2} &= 2.5 \times t_{CYC} - 53 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{CYC} - 26 \text{ (ns)} \\ t_{ACC3} &= 1.0 \times t_{CYC} - 47 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{CYC} - 32 \text{ (ns)} \\ t_{ACC4} &= 2.0 \times t_{CYC} - 54 \text{ (ns)} \end{aligned}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{ACC1} &= 1.5 \times t_{CYC} - 34 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{CYC} - 28 \text{ (ns)} \\ t_{ACC2} &= 2.5 \times t_{CYC} - 37 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{CYC} - 29 \text{ (ns)} \\ t_{ACC3} &= 1.0 \times t_{CYC} - 33 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{CYC} - 28 \text{ (ns)} \\ t_{ACC4} &= 2.0 \times t_{CYC} - 30 \text{ (ns)} \end{aligned}$$

At 18 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{ACC1} &= 1.5 \times t_{CYC} - 34 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{CYC} - 24 \text{ (ns)} \\ t_{ACC2} &= 2.5 \times t_{CYC} - 34 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{CYC} - 22 \text{ (ns)} \\ t_{ACC3} &= 1.0 \times t_{CYC} - 36 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{CYC} - 21 \text{ (ns)} \\ t_{ACC4} &= 2.0 \times t_{CYC} - 31 \text{ (ns)} \end{aligned}$$

Table 21-5 Refresh Controller Bus Timing

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS delay time 1	t _{RAD1}	—	60	—	50	—	30	—	30	ns	Figure 21-10 to Figure 21-16
RAS delay time 2	t _{RAD2}	—	60	—	50	—	30	—	30		
RAS delay time 3	t _{RAD3}	—	60	—	50	—	30	—	30		
Row address hold time*	t _{RAH}	25	—	20	—	15	—	15	—		
RAS precharge time*	t _{RP}	85	—	55	—	45	—	40	—		
CAS to RAS precharge time*	t _{CRP}	85	—	55	—	45	—	40	—		
CAS pulse width	t _{CAS}	100	—	55	—	40	—	35	—		
RAS access time*	t _{RAC}	—	160	—	80	—	85	—	70		
Address access time	t _{AA}	—	105	—	45	—	55	—	45		
CAS access time*	t _{CAC}	—	50	—	30	—	30	—	25		
Write data setup time 3	t _{WDS3}	50	—	20	—	15	—	10	—		
CAS setup time*	t _{CSR}	20	—	10	—	15	—	10	—		
Read strobe delay time	t _{RSD}	—	60	—	50	—	30	—	30		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{CYC} - 38 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{CYC} - 75 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{CYC} - 90 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{CYC} - 43 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 40 \text{ (ns)}$$

At 13 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{CYC} - 19 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{CYC} - 47 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{CYC} - 74 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{CYC} - 29 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 22 \text{ (ns)}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{CYC} - 17 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{CYC} - 33 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{CYC} - 40 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{CYC} - 17 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 18 \text{ (ns)}$$

At 18 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{CYC} - 13 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{CYC} - 31 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{CYC} - 41 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{CYC} - 18 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 16 \text{ (ns)}$$

Table 21-6 Control Signal Timing

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions
		8 MHz	13 MHz	16 MHz	18 MHz						
RES setup time	t _{RESS}	200	—	200	—	200	—	200	—	ns	Figure 21-18
RES pulse width	t _{RESW}	10	—	10	—	10	—	10	—	t _{cyc}	
Mode programming setup time	t _{MDS}	200	—	200	—	200	—	200	—	ns	
RESO output delay time	t _{RESO}	—	100	—	100	—	100	—	100	ns	Figure 21-19
RESO output pulse width	t _{RESOW}	132	—	132	—	132	—	132	—	t _{cyc}	
NMI setup time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t _{NMIS}	200	—	200	—	150	—	150	—	ns	Figure 21-20
NMI hold time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t _{NMIH}	10	—	10	—	10	—	10	—		
Interrupt pulse width (NMI, $\overline{IRQ_2}$ to $\overline{IRQ_0}$ when exiting software standby mode)	t _{NMIW}	200	—	200	—	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t _{OSC1}	20	—	20	—	20	—	20	—	ms	Figure 21-22
Clock oscillator settling time in software standby (crystal)	t _{OSC2}	7	—	7	—	7	—	7	—	ms	Figure 20-1

Table 21-7 Timing of On-Chip Supporting Modules
—Preliminary—

Condition A: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 8 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 3.15 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 3.15 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 13 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 18 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions	
			8 MHz		13 MHz		16 MHz		18 MHz				
			Min	Max	Min	Max	Min	Max	Min	Max			
DMAC	$\overline{\text{DREQ}}$ setup time	t_{DRQS}	40	—	40	—	30	—	30	—	ns	Figure 21-30	
	$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—	10	—	10	—	10	—			
	$\overline{\text{TEND}}$ delay time 1	t_{TED1}	—	100	—	100	—	50	—	50			Figure 21-28, Figure 21-29
	$\overline{\text{TEND}}$ delay time 2	t_{TED2}	—	100	—	100	—	50	—	50			
ITU	Timer output delay time	t_{TOCD}	—	100	—	100	—	100	—	100	ns	Figure 21-24	
	Timer input setup time	t_{TICS}	50	—	50	—	50	—	50	—			
	Timer clock input setup time	t_{TCKS}	50	—	50	—	50	—	50	—		Figure 21-25	
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	1.5	—	1.5	—		t_{CYC}
		Both edges	t_{TCKWL}	2.5	—	2.5	—	2.5	—	2.5	—		
SCI	Input clock cycle	Asynchronous	t_{SCYC}	4	—	4	—	4	—	4	—	t_{CYC}	Figure 21-26
		Synchronous	t_{SCYC}	6	—	6	—	6	—	6	—		
	Input clock rise time	t_{SCKR}	—	1.5	—	1.5	—	1.5	—	1.5			
	Input clock fall time	t_{SCKF}	—	1.5	—	1.5	—	1.5	—	1.5			
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{SCYC}		

Table 21-7 Timing of On-Chip Supporting Modules (cont)

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

		Symbol	Condition A		Condition B		Condition C				Unit	Test Conditions
			8 MHz		13 MHz		16 MHz		18 MHz			
SCI	Transmit data delay time	t _{TXD}	—	100	—	100	—	100	—	100	ns	Figure 21-27
	Receive data setup time (synchronous)	t _{RXS}	100	—	100	—	100	—	100	—		
	Receive data hold time (synchronous)	Clock input t _{RXH}	100	—	100	—	100	—	100	—		
		Clock output	0	—	0	—	0	—	0	—		
Ports and TPC	Output data delay time	t _{PWD}	—	100	—	100	—	100	—	100	ns	Figure 21-23
	Input data setup time	t _{PRS}	50	—	50	—	50	—	50	—		
	Input data hold time	t _{PRH}	50	—	50	—	50	—	50	—		

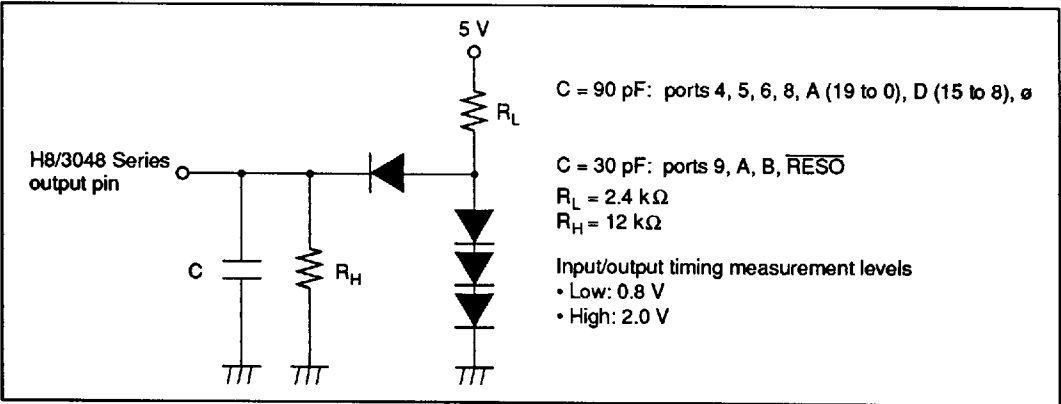


Figure 21-3 Output Load Circuit

21.2.3 A/D Conversion Characteristics

Table 21-8 lists the A/D conversion characteristics.

Table 21-8 A/D Converter Characteristics —Preliminary—

- Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)
- Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)
- Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item	Condition A			Condition B			Condition C						Unit
	8 MHz			13 MHz			16 MHz			18 MHz			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	10.4	—	—	8.4	—	—	7.5	μs
Analog input capacitance	—	—	20	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10 ^{*1}	—	—	10 ^{*1}	—	—	10 ^{*3}	—	—	10 ^{*3}	kΩ
	—	—	5 ^{*2}	—	—	5 ^{*2}	—	—	5 ^{*4}	—	—	5 ^{*4}	
Nonlinearity error	—	—	±6.0	—	—	±6.0	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	—	—	±4.0	—	—	±4.0	LSB

- Notes: 1. The value is for $4.0 \leq AV_{CC} \leq 5.5$.
2. The value is for $2.7 \leq AV_{CC} \leq 4.0$.
3. The value is for $\phi \leq 12\text{ MHz}$.
4. The value is for $\phi > 12\text{ MHz}$.

21.2.4 D/A Conversion Characteristics

Table 21-9 lists the D/A conversion characteristics.

Table 21-9 D/A Converter Characteristics —Preliminary—

- Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular
specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)
- Condition B: $V_{CC} = 3.15\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.15\text{ V to }5.5\text{ V}$, $V_{REF} = 3.15\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }13\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular
specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)
- Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }18\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular
specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item	Condition A			Condition B			Condition C						Unit	Test Conditions
	8 MHz			13 MHz			16 MHz			18 MHz				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	—	—	10	—	—	10	μs	20-pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	—	±1.0	±1.5	—	±1.0	±1.5	LSB	2-MΩ resistive load
	—	—	±2.0	—	—	±2.0	—	—	±1.0	—	—	±1.0	LSB	4-MΩ resistive load

21.3 Electrical Characteristics of Flash Memory Version

21.3.1 DC Characteristics

Table 21-10 lists the DC characteristics. Table 21-11 lists the permissible output currents.

Table 21-10 DC Characteristics

—Preliminary—

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V}$ to AV_{CC} ,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A,	V_{T^-}	1.0	—	—	V	
	P8 ₀ to P8 ₂ ,	V_{T^+}	—	—	$V_{CC} \times 0.7$	V	
	PB ₀ to PB ₃	$V_{T^+} - V_{T^-}$	0.4	—	—	V	
Input high voltage	RES, STBY, NMI, MD ₂ to MD ₀	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		2.0	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	RES, STBY, MD ₂ to MD ₀	V_{IL}	-0.3	—	0.5	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		-0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			3.5	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low voltage	All output pins (except RES0)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
	Ports 1, 2, 5, and B		—	—	1.0	V	$I_{OL} = 10 \text{ mA}$
	RES0		—	—	0.4	V	$I_{OL} = 2.6 \text{ mA}$

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V}$ to AV_{CC} ,
 $V_{SS} = AV_{SS} = 0 \text{ V}^{*1}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD ₁ , MD ₀	$ I_{IN} $	—	—	1.0	μA	$V_{IN} = 0.5$ to $V_{CC} - 0.5 \text{ V}$
	MD ₂		—	—	10.0	μA	$V_{IN} = 0.5$ to $V_{CC} + 0.5 \text{ V}$
	MD ₂		—	—	50.0	μA	$V_{IN} = V_{CC} + 0.5$ to 12.6 V
	Port 7		—	—	1.0	μA	$V_{IN} = 0.5$ to $AV_{CC} - 0.5 \text{ V}$
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$ I_{TS1} $	—	—	1.0	μA	$V_{IN} = 0.5$ to $V_{CC} - 0.5 \text{ V}$
	$\overline{RESO}$		—	—	10.0	μA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	50	—	300	μA	$V_{IN} = 0 \text{ V}$
Input capacitance	NMI	C_{IN}	—	—	50	pF	$V_{IN} = 0 \text{ V}$
	All input pins except NMI		—	—	15	pF	$f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$
Current dissipation*2	Normal operation	I_{CC}	—	50	65	mA	$f = 16 \text{ MHz}$
	Sleep mode		—	35	50	mA	$f = 16 \text{ MHz}$
	Module standby mode*4		—	20	25	mA	$f = 16 \text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
			—	—	20.0	μA	$50^\circ\text{C} < T_a$

- Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5 \text{ V}$ and $V_{ILmax} = 0.5 \text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5 \text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3 \text{ V}$.
4. Module standby current values apply in sleep mode with all modules halted.

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V}$ to AV_{CC} ,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D and D/A conversion		—	1.2	2.0	mA	
	Idle		—	0.01	5.0	μA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	$V_{REF} = 5.0\text{ V}$
	During A/D and D/A conversion		—	1.3	3.0	mA	
	Idle		—	0.01	5.0	μA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^*$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, P8 ₀ to P8 ₂ , PB ₀ to PB ₃	V_{T^-}	$V_{CC} \times 0.2$	—	—	V	
		V_{T^+}	—	—	$V_{CC} \times 0.7$	V	
		$V_{T^+} - V_{T^-}$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	RES, STBY, NMI, MD ₂ to MD ₀	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	RES, STBY, MD ₂ to MD ₀	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, P8 ₃ , P8 ₄ , PB ₄ to PB ₇		-0.3	—	$V_{CC} \times 0.2$	V	$V_{CC} < 4.0 \text{ V}$
					0.8	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200 \mu\text{A}$
			$V_{CC} - 1.0$	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low voltage	All output pins (except RES0)	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
	Ports 1, 2, 5, and B		—	—	1.0	V	$V_{CC} \leq 4 \text{ V}$ $I_{OL} = 5 \text{ mA}$, $4 \text{ V} < V_{CC} \leq 5.5 \text{ V}$ $I_{OL} = 10 \text{ mA}$
	RES0		—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD ₁ , MD ₀	$ I_{IN} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	MD ₂		—	—	10.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} + 0.5\text{ V}$
	MD ₂		—	—	50.0	μA	$V_{IN} = V_{CC} + 0.5\text{ to }12.6\text{ V}$
	Port 7		—	—	1.0	μA	$V_{IN} = 0.5\text{ to }AV_{CC} - 0.5\text{ V}$
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$ I_{TS1} $	—	—	1.0	μA	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	$\overline{RESO}$		—	—	10.0	μA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	10	—	300	μA	$V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{IN} = 0\text{ V}$
Input capacitance	NMI	C_{IN}	—	—	50	pF	$V_{IN} = 0\text{ V}$
	All input pins except NMI		—	—	15		$f = 1\text{ MHz}$ $T_a = 25^\circ\text{C}$

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}^1$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular specifications),
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}^{*4}	—	12 (3.0 V)	35 (5.5 V)	mA	$f = 8 \text{ MHz}$
	Sleep mode		—	8 (3.0 V)	25 (5.5 V)	mA	$f = 8 \text{ MHz}$
	Module standby mode*5		—	5 (3.0 V)	14 (5.5 V)	mA	$f = 8 \text{ MHz}$
	Standby mode*3		—	0.01	5.0	μA	$T_a \leq 50^\circ\text{C}$
			—	—	20.0	μA	$50^\circ\text{C} < T_a$

- Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5 \text{ V}$ and $V_{ILmax} = 0.5 \text{ V}$ with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7 \text{ V}$, $V_{IHmin} = V_{CC} \times 0.9$, and $V_{ILmax} = 0.3 \text{ V}$.
4. I_{CC} depends on V_{CC} and f as follows:
 $I_{CCmax} = 3.0 \text{ (mA)} + 0.75 \text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [normal mode]
 $I_{CCmax} = 3.0 \text{ (mA)} + 0.55 \text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [sleep mode]
 $I_{CCmax} = 3.0 \text{ (mA)} + 0.25 \text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [module standby mode]
5. Module standby current values apply in sleep mode with all modules halted.

Table 21-10 DC Characteristics (cont)

—Preliminary—

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$. $V_{SS} = AV_{SS} = 0\text{ V}^*$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	0.4	1.0	mA	$AV_{CC} = 3.0\text{ V}$
			—	1.2	—	mA	$AV_{CC} = 5.0\text{ V}$
	During A/D and D/A conversion		—	0.4	1.0	mA	$AV_{CC} = 3.0\text{ V}$
			—	1.2	—	mA	$AV_{CC} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	$V_{REF} = 3.0\text{ V}$
			—	0.3	—	mA	$V_{REF} = 5.0\text{ V}$
	During A/D and D/A conversion		—	0.8	2.0	mA	$V_{REF} = 3.0\text{ V}$
			—	1.3	—	mA	$V_{REF} = 5.0\text{ V}$
	Idle		—	0.01	5.0	μA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC} , AV_{SS} , and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC} , and connect AV_{SS} to V_{SS} .

Table 21-11 Permissible Output Currents**—Preliminary—**

Conditions: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications),
 $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 5, and B	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins in ports 1, 2, 5, and B	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 21-11.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21-4 and 21-5.

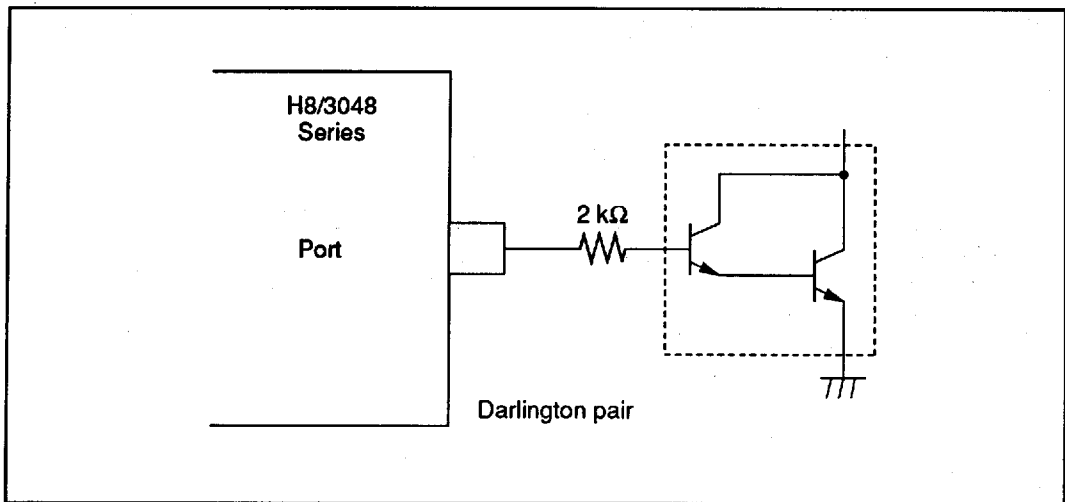


Figure 21-4 Darlington Pair Drive Circuit (Example)

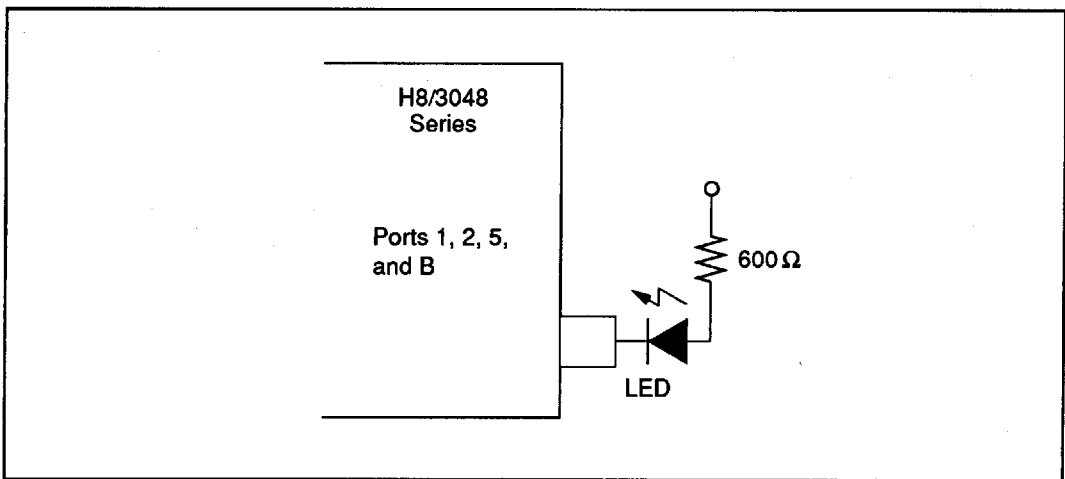


Figure 21-5 LED Drive Circuit (Example)

21.3.2 AC Characteristics

Bus timing parameters are listed in table 21-12. Refresh controller bus timing parameters are listed in table 21-13. Control signal timing parameters are listed in table 21-14. Timing parameters of the on-chip supporting modules are listed in table 21-15.

Table 21-12 Bus Timing (1)

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition C		Unit	Test Conditions
		8 MHz		16 MHz			
		Min	Max	Min	Max		
Clock cycle time	t _{CYC}	125	1000	62.5	1000	ns	Figure 21-7
Clock pulse low width	t _{CL}	40	—	20	—		Figure 21-8
Clock pulse high width	t _{CH}	40	—	20	—		
Clock rise time	t _{CR}	—	20	—	10		
Clock fall time	t _{CF}	—	20	—	10		
Address delay time	t _{AD}	—	60	—	30		
Address hold time	t _{AH}	25	—	10	—		
Address strobe delay time	t _{ASD}	—	60	—	30		
Write strobe delay time	t _{WSD}	—	60	—	30		
Strobe delay time	t _{SD}	—	60	—	30		
Write data strobe pulse width 1	t _{WSW1*}	85	—	35	—		
Write data strobe pulse width 2	t _{WSW2*}	150	—	65	—		
Address setup time 1	t _{AS1}	20	—	10	—		
Address setup time 2	t _{AS2}	80	—	40	—		
Read data setup time	t _{RDS}	50	—	20	—		
Read data hold time	t _{RDH}	0	—	0	—		

Table 21-12 Bus Timing (cont)**—Preliminary—**

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition C		Unit	Test Conditions
		8 MHz		16 MHz			
		Min	Max	Min	Max		
Write data delay time	t _{WDD}	—	75	—	60	ns	Figure 21-7
Write data setup time 1	t _{WDS1}	60	—	15	—		Figure 21-8
Write data setup time 2	t _{WDS2}	5	—	–5	—		
Write data hold time	t _{WDH}	25	—	20	—		
Read data access time 1	t _{ACC1*}	—	120	—	60		
Read data access time 2	t _{ACC2*}	—	240	—	120		
Read data access time 3	t _{ACC3*}	—	70	—	30		
Read data access time 4	t _{ACC4*}	—	180	—	95		
Precharge time	t _{PCH*}	85	—	45	—		
Wait setup time	t _{WTS}	40	—	25	—	ns	Figure 21-9
Wait hold time	t _{WTH}	10	—	5	—		
Bus request setup time	t _{BRQS}	40	—	40	—	ns	Figure 21-21
Bus acknowledge delay time 1	t _{BACD1}	—	60	—	30		
Bus acknowledge delay time 2	t _{BACD2}	—	60	—	30		
Bus-floating time	t _{BZD}	—	70	—	40		

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{array}{ll}
 t_{ACC1} = 1.5 \times t_{CYC} - 68 \text{ (ns)} & t_{WSW1} = 1.0 \times t_{CYC} - 40 \text{ (ns)} \\
 t_{ACC2} = 2.5 \times t_{CYC} - 73 \text{ (ns)} & t_{WSW2} = 1.5 \times t_{CYC} - 38 \text{ (ns)} \\
 t_{ACC3} = 1.0 \times t_{CYC} - 55 \text{ (ns)} & t_{PCH} = 1.0 \times t_{CYC} - 40 \text{ (ns)} \\
 t_{ACC4} = 2.0 \times t_{CYC} - 70 \text{ (ns)} &
 \end{array}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{array}{ll}
 t_{ACC1} = 1.5 \times t_{CYC} - 34 \text{ (ns)} & t_{WSW1} = 1.0 \times t_{CYC} - 28 \text{ (ns)} \\
 t_{ACC2} = 2.5 \times t_{CYC} - 37 \text{ (ns)} & t_{WSW2} = 1.5 \times t_{CYC} - 29 \text{ (ns)} \\
 t_{ACC3} = 1.0 \times t_{CYC} - 33 \text{ (ns)} & t_{PCH} = 1.0 \times t_{CYC} - 28 \text{ (ns)} \\
 t_{ACC4} = 2.0 \times t_{CYC} - 30 \text{ (ns)} &
 \end{array}$$

Table 21-13 Refresh Controller Bus Timing

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition C		Unit	Test Conditions
		8 MHz		16 MHz			
		Min	Max	Min	Max		
RAS delay time 1	t_{RAD1}	—	60	—	30	ns	Figure 21-10 to Figure 21-16
RAS delay time 2	t_{RAD2}	—	60	—	30		
RAS delay time 3	t_{RAD3}	—	60	—	30		
Row address hold time*	t_{RAH}	25	—	15	—		
RAS precharge time*	t_{RP}	85	—	45	—	ns	Figure 21-10 to Figure 21-16
CAS to RAS precharge time*	t_{CRP}	85	—	45	—		
CAS pulse width	t_{CAS}	100	—	40	—		
RAS access time*	t_{RAC}	—	160	—	85		
Address access time	t_{AA}	—	105	—	55	ns	Figure 21-10 to Figure 21-16
CAS access time*	t_{CAC}	—	50	—	30		
Write data setup time 3	t_{WDS3}	50	—	15	—		
CAS setup time*	t_{CSR}	20	—	15	—		
Read strobe delay time	t_{RSD}	—	60	—	30	ns	Figure 21-10 to Figure 21-16

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{RAH} &= 0.5 \times t_{CYC} - 38 \text{ (ns)} & t_{CAC} &= 1.0 \times t_{CYC} - 75 \text{ (ns)} \\ t_{RAC} &= 2.0 \times t_{CYC} - 90 \text{ (ns)} & t_{CSR} &= 0.5 \times t_{CYC} - 43 \text{ (ns)} \\ t_{RP} &= t_{CRP} = 1.0 \times t_{CYC} - 40 \text{ (ns)} \end{aligned}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned} t_{RAH} &= 0.5 \times t_{CYC} - 17 \text{ (ns)} & t_{CAC} &= 1.0 \times t_{CYC} - 33 \text{ (ns)} \\ t_{RAC} &= 2.0 \times t_{CYC} - 40 \text{ (ns)} & t_{CSR} &= 0.5 \times t_{CYC} - 17 \text{ (ns)} \\ t_{RP} &= t_{CRP} = 1.0 \times t_{CYC} - 18 \text{ (ns)} \end{aligned}$$

Table 21-14 Control Signal Timing
—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Condition A		Condition C		Unit	Test Conditions
		Min	Max	Min	Max		
RES setup time	t _{RESS}	200	—	200	—	ns	Figure 21-18
RES pulse width	t _{RESW}	10	—	10	—	t _{CYC}	
Mode programming setup time	t _{MDS}	200	—	200	—	ns	
RESO output delay time	t _{RESO}	—	100	—	100	ns	Figure 21-19
RESO output pulse width	t _{RESOW}	132	—	132	—	t _{CYC}	
NMI setup time (NMI, IRQ ₅ to IRQ ₀)	t _{NMIS}	200	—	150	—	ns	Figure 21-20
NMI hold time (NMI, IRQ ₅ to IRQ ₀)	t _{NMIH}	10	—	10	—		
Interrupt pulse width (NMI, IRQ ₂ to IRQ ₀ when exiting software standby mode)	t _{NMIW}	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t _{OSC1}	20	—	20	—	ms	Figure 21-22
Clock oscillator settling time in software standby (crystal)	t _{OSC2}	7	—	7	—	ms	Figure 20-1

Table 21-15 Timing of On-Chip Supporting Modules**—Preliminary—**

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

		Symbol	Condition A		Condition C		Unit	Test Conditions	
			Min	Max	Min	Max			
DMAC	DREQ setup time	t _{DROS}	40	—	30	—	ns	Figure 21-30	
	DREQ hold time	t _{DRQH}	10	—	10	—			
	TEND delay time 1	t _{TED1}	—	100	—	50	Figure 21-28, Figure 21-29		
	TEND delay time 2	t _{TED2}	—	100	—	50			
ITU	Timer output delay time	t _{TOCD}	—	100	—	100	ns	Figure 21-24	
	Timer input setup time	t _{TICS}	50	—	50	—			
	Timer clock input setup time	t _{TCKS}	50	—	50	—	Figure 21-25		
	Timer clock pulse width	Single edge	t _{TCKWH}	1.5	—	1.5		t _{cyc}	
		Both edges	t _{TCKWL}	2.5	—	2.5			
SCI	Input clock cycle	Asynchronous	t _{SCYC}	4	—	4	—	t _{cyc}	Figure 21-26
		Synchronous	t _{SCYC}	6	—	6	—		
	Input clock rise time	t _{SCKR}	—	1.5	—	1.5			
	Input clock fall time	t _{SCKF}	—	1.5	—	1.5			
	Input clock pulse width	t _{SCKW}	0.4	0.6	0.4	0.6	t _{scyc}		

Table 21-15 Timing of On-Chip Supporting Modules (cont)

—Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item		Symbol	Condition A		Condition C		Unit	Test Conditions	
			8 MHz		16 MHz				
			Min	Max	Min	Max			
SCI	Transmit data delay time	t _{TXD}	—	100	—	100	ns	Figure 21-27	
	Receive data setup time (synchronous)	t _{RXS}	100	—	100	—			
	Receive data hold time (synchronous)	Clock input	t _{RXH}	100	—	100			—
		Clock output	t _{RXH}	0	—	0			—
Ports and TPC	Output data delay time	t _{PWD}	—	100	—	100	ns	Figure 21-23	
	Input data setup time	t _{PRS}	50	—	50	—			
	Input data hold time	t _{PRH}	50	—	50	—			

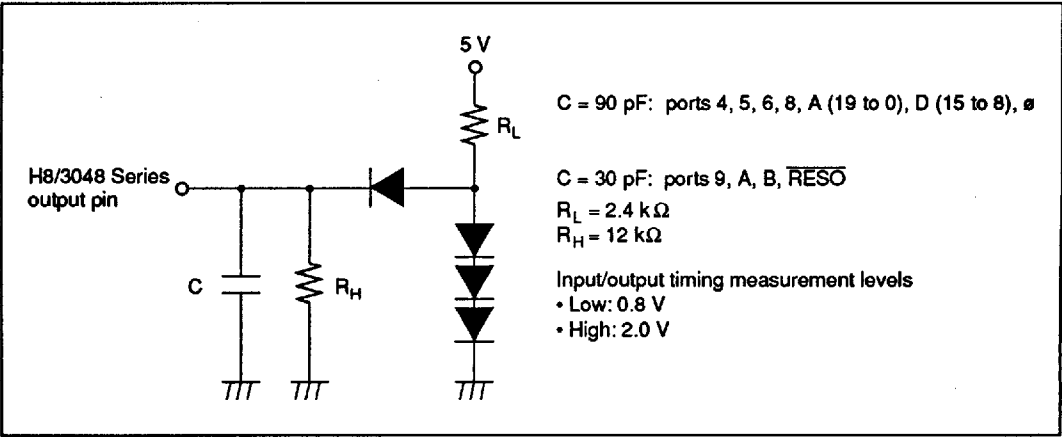


Figure 21-6 Output Load Circuit

21.3.3 A/D Conversion Characteristics

Table 21-16 lists the A/D conversion characteristics.

Table 21-16 A/D Converter Characteristics

—Preliminary—

Condition A: $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $AV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{REF} = 2.7 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 8 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{REF} = 4.5 \text{ V to } AV_{CC}$,
 $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 1 \text{ MHz to } 16 \text{ MHz}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ (regular
specifications), $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ (wide-range specifications)

Item	Condition A			Condition C			Unit
	8 MHz			16 MHz			
	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	8.4	μs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*1	—	—	10*3	kΩ
	—	—	5*2	—	—	5*4	
Nonlinearity error	—	—	±6.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	LSB

Notes: 1. The value is for $4.0 \leq AV_{CC} \leq 5.5$.
2. The value is for $2.7 \leq AV_{CC} < 4.0$.
3. The value is for $\phi \leq 12 \text{ MHz}$.
4. The value is for $\phi > 12 \text{ MHz}$.

21.3.4 D/A Conversion Characteristics

Table 21-17 lists the D/A conversion characteristics.

Table 21-17 D/A Converter Characteristics —Preliminary—

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular
specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^{\circ}\text{C to }+75^{\circ}\text{C}$ (regular
specifications), $T_a = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ (wide-range specifications)

Item	Condition A			Condition C			Unit	Test Conditions
	8 MHz			16 MHz				
	Min	Typ	Max	Min	Typ	Max		
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	μs	20-pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±1.0	±1.5	LSB	2-MΩ resistive load
	—	—	±2.0	—	—	±1.0	LSB	4-MΩ resistive load

21.3.5 Flash Memory Characteristics

Table 21-18 lists the flash memory characteristics.

Table 21-18 Flash Memory

Condition A: $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{REF} = 2.7\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $V_{PP} = 12\text{ V} \pm 0.6\text{ V}$, $\phi = 1\text{ MHz to }8\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Condition C: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{REF} = 4.5\text{ V to }AV_{CC}$,
 $V_{SS} = AV_{SS} = 0\text{ V}$, $V_{PP} = 12\text{ V} \pm 0.6\text{ V}$, $\phi = 1\text{ MHz to }16\text{ MHz}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ (regular specifications), $T_a = -40^\circ\text{C to }+85^\circ\text{C}$ (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming time*1	t_p	—	50	1000	μs	
Erase time*1	t_E	—	1	30	s	
Erase-program cycle	N_{WEC}	—	—	100	time	
Verify setup time 1*1	t_{VS1}	4	—	—	μs	
Verify setup time 2*1	t_{VS2}	2	—	—	μs	
Flash memory read setup time*2	t_{FRS}	50	—	—	μs	$V_{CC} \geq 4.5\text{ V}$
		100	—	—	μs	$V_{CC} < 4.5\text{ V}$

- Notes: 1. To specify each time, follow the appropriate algorithm.
2. Before reading the flash memory, wait at least for the read setup time after clearing the $V_{PP}E$ bit; lowering the voltage supplied to V_{PP} from 12 V to 0–5 V; turning on the power when the external clock is used; or returning from standby mode. When the V_{PP} voltage is cut off, t_{FRS} indicates the time from when the V_{PP} falls below $V_{CC} + 2\text{ V}$ to when the flash memory is read.

21.4 Operational Timing

This section shows timing diagrams.

21.4.1 Bus Timing

Bus timing is shown as follows:

- Basic bus cycle: two-state access

Figure 21-7 shows the timing of the external two-state access cycle.

- Basic bus cycle: three-state access

Figure 21-8 shows the timing of the external three-state access cycle.

- Basic bus cycle: three-state access with one wait state

Figure 21-9 shows the timing of the external three-state access cycle with one wait state inserted.

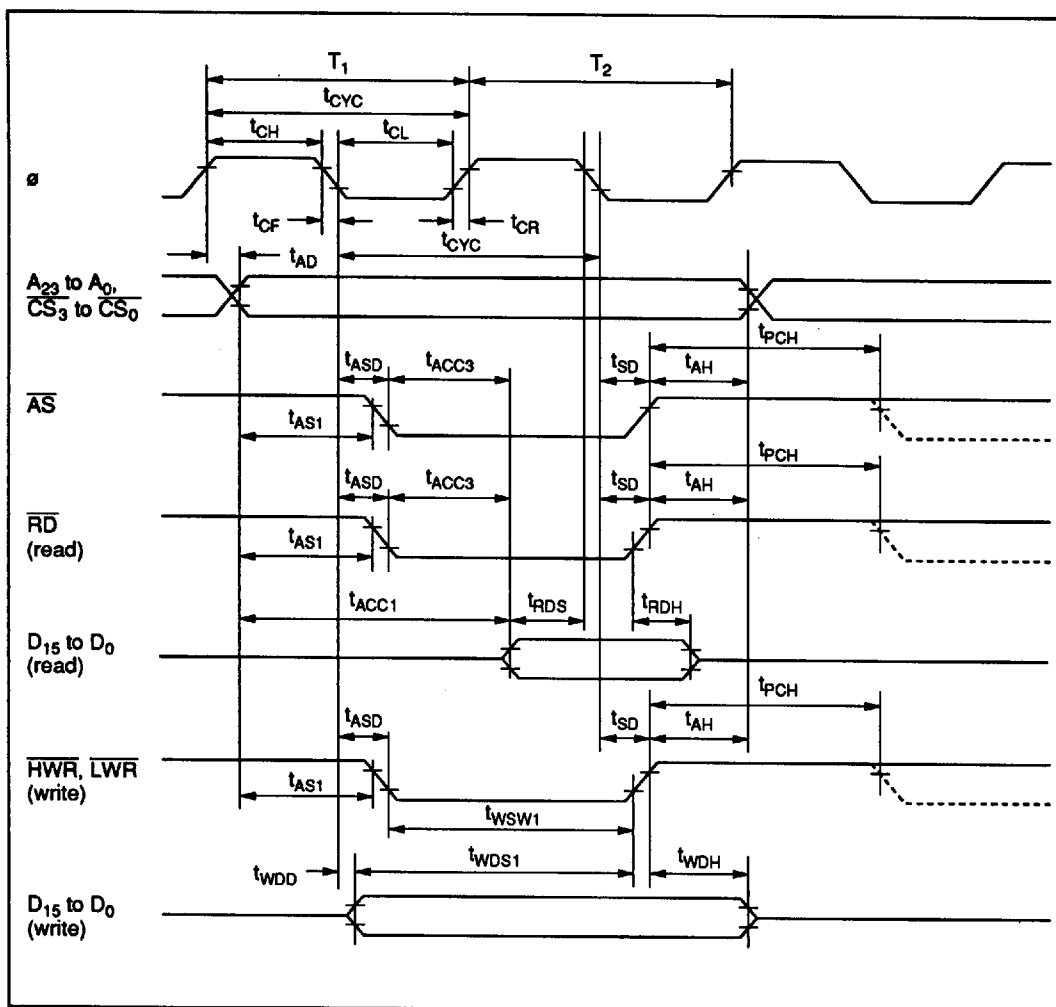


Figure 21-7 Basic Bus Cycle: Two-State Access

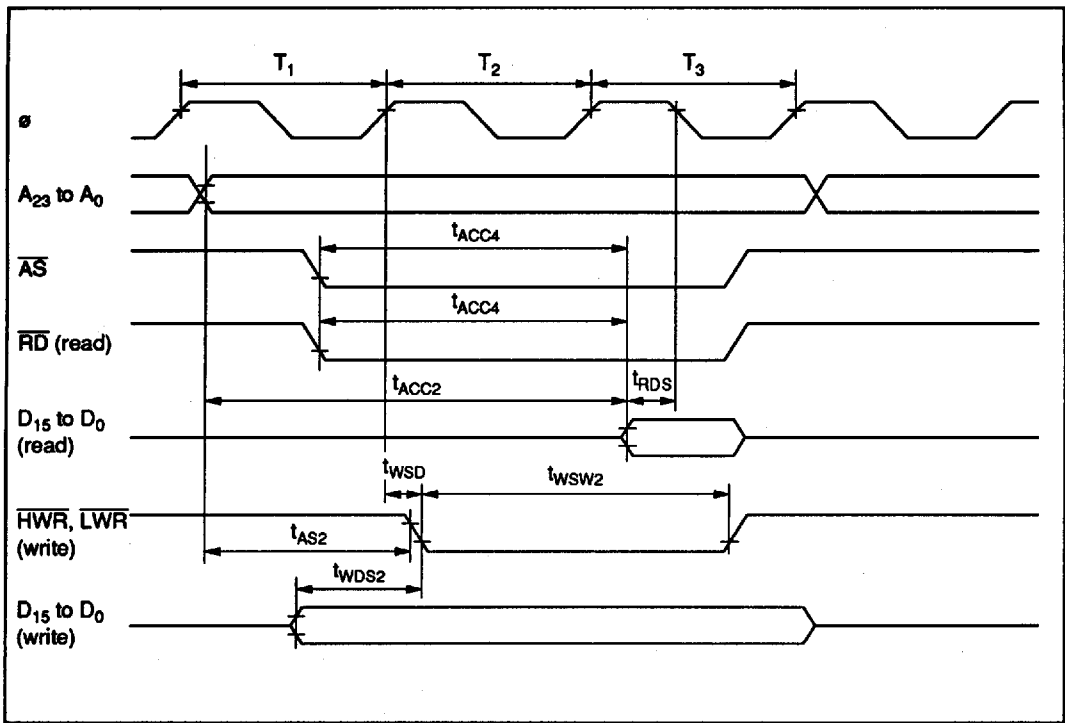


Figure 21-8 Basic Bus Cycle: Three-State Access

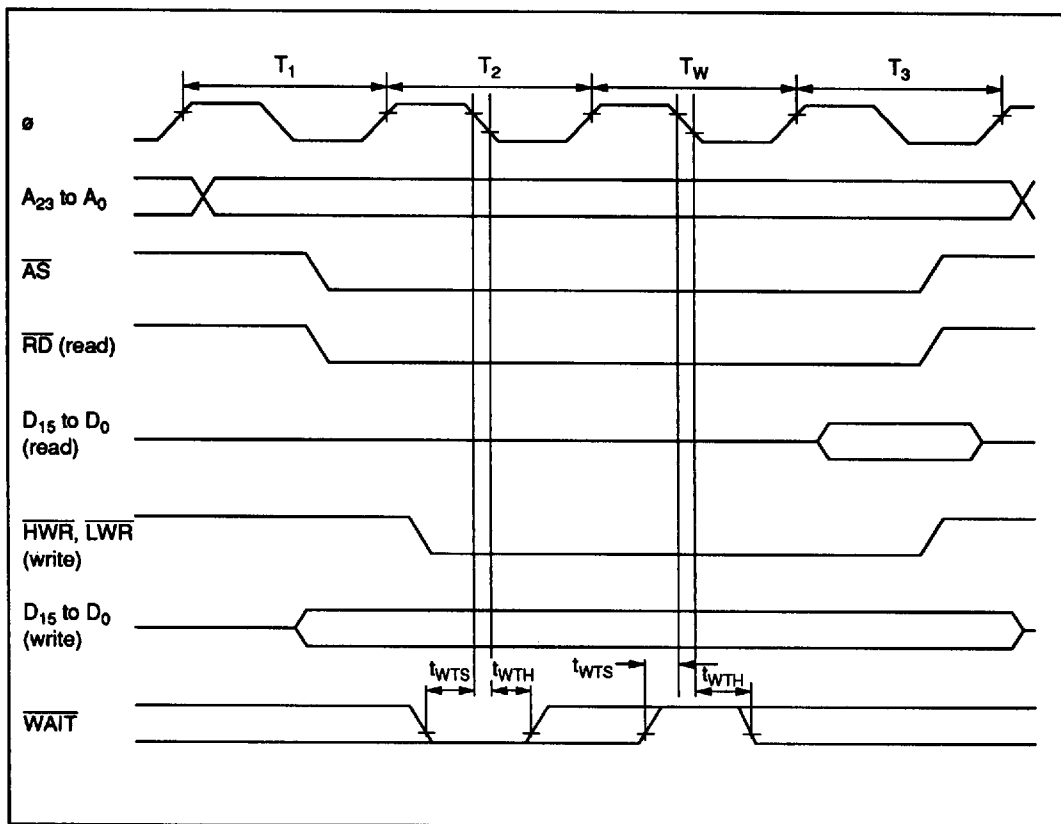


Figure 21-9 Basic Bus Cycle: Three-State Access with One Wait State

21.4.2 Refresh Controller Bus Timing

Refresh controller bus timing is shown as follows:

- DRAM bus timing

Figures 21-10 to 21-15 show the DRAM bus timing in each operating mode.

- PSRAM bus timing

Figures 21-16 and 21-17 show the pseudo-static RAM bus timing in each operating mode.

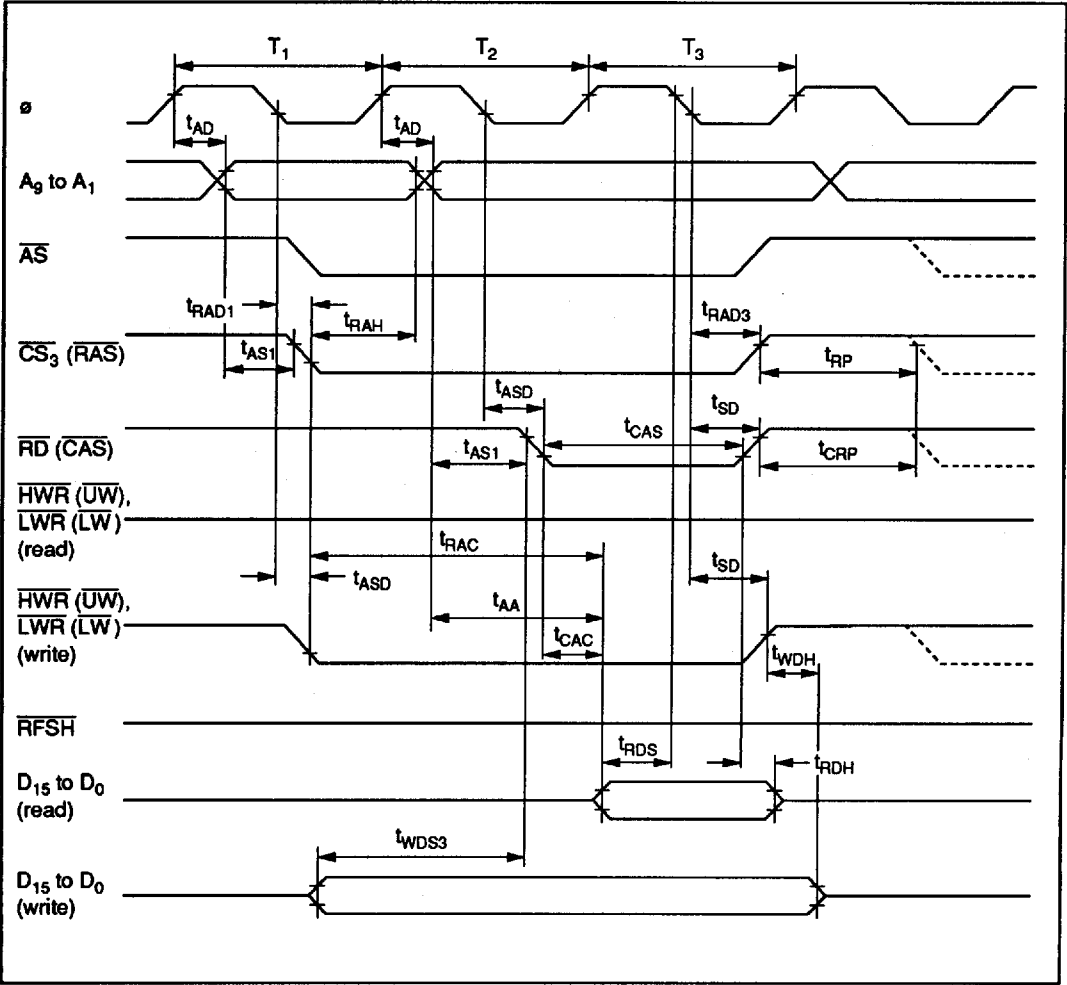


Figure 21-10 DRAM Bus Timing (Read/Write): Three-State Access
— 2WE Mode —

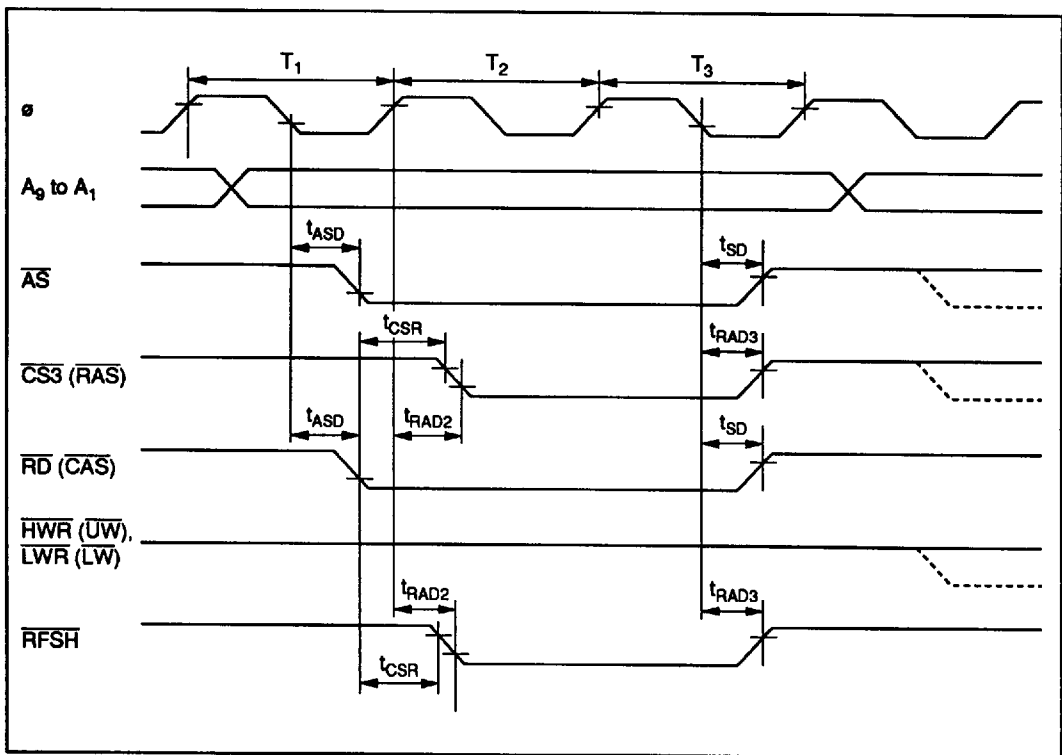


Figure 21-11 DRAM Bus Timing (Refresh Cycle): Three-State Access
— 2WE Mode —

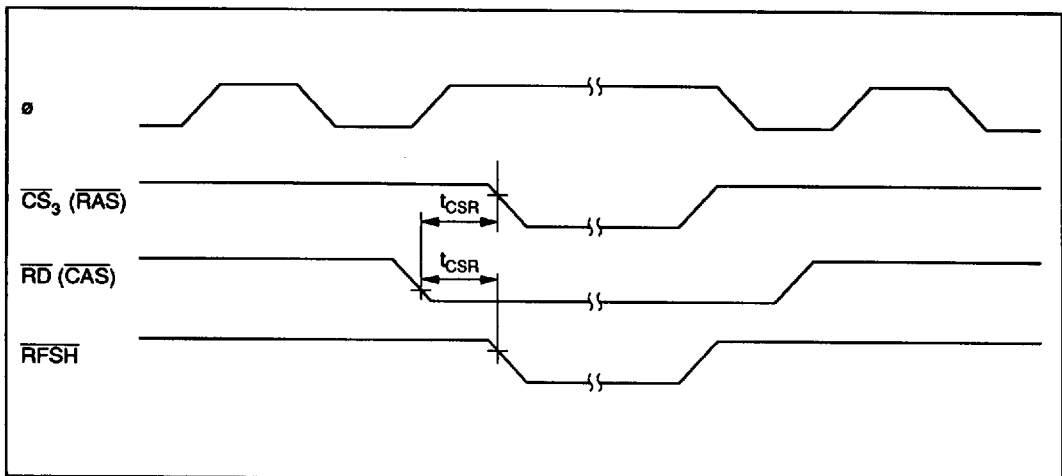


Figure 21-12 DRAM Bus Timing (Self-Refresh Mode)
— 2WE Mode —

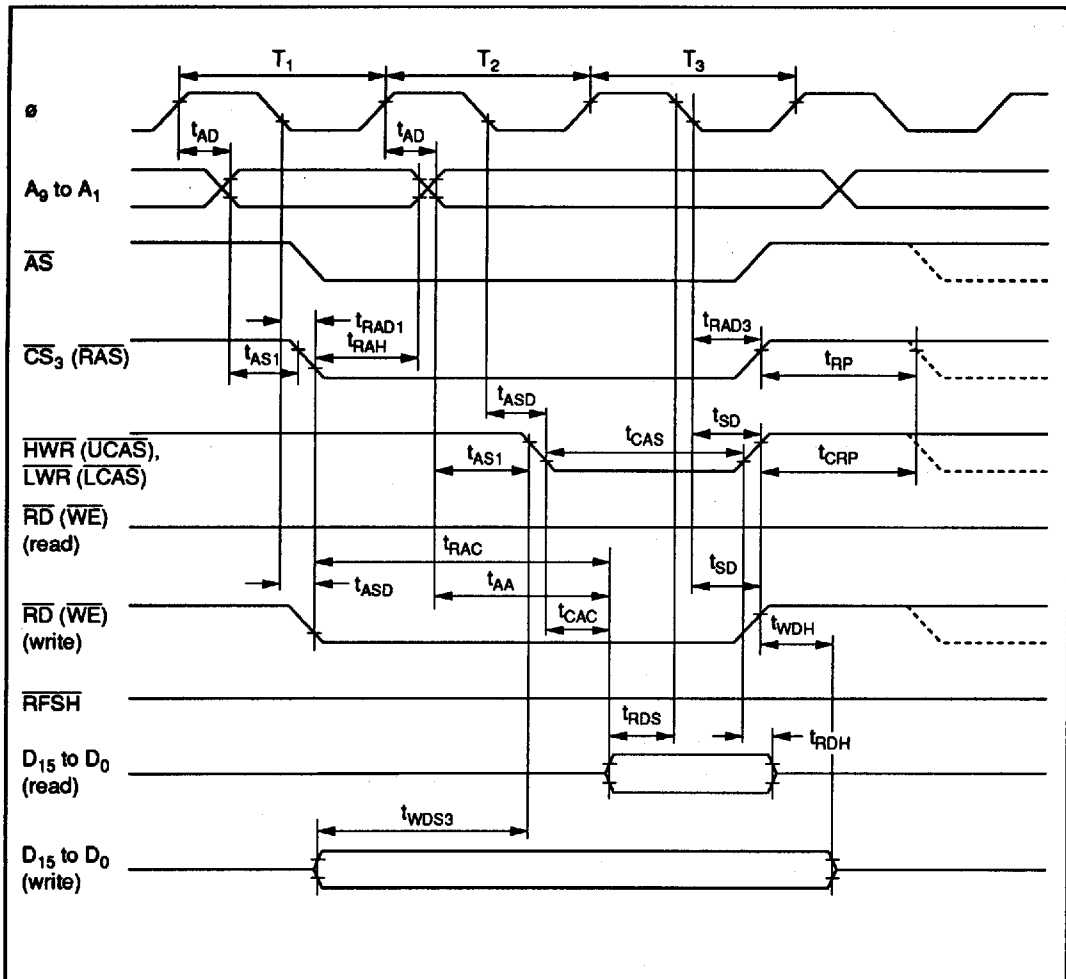


Figure 21-13 DRAM Bus Timing (Read/Write): Three-State Access
— 2CAS Mode —

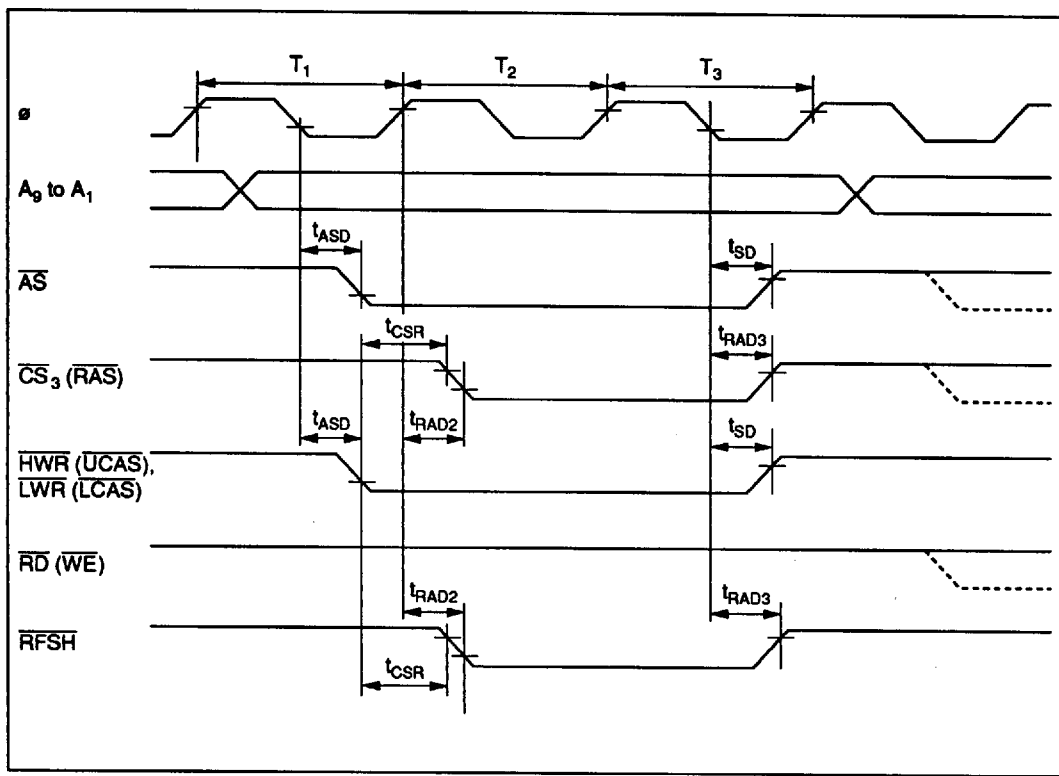


Figure 21-14 DRAM Bus Timing (Refresh Cycle): Three-State Access
— 2CAS Mode —

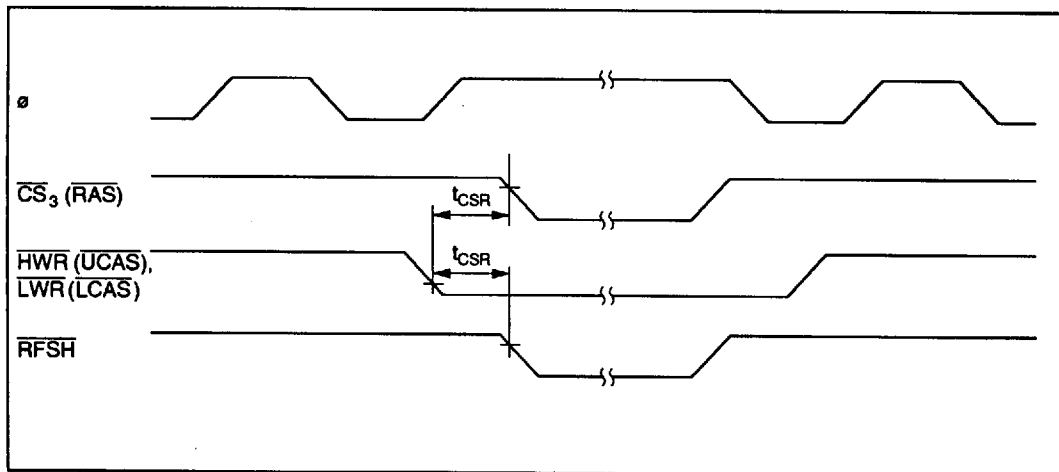


Figure 21-15 DRAM Bus Timing (Self-Refresh Mode)
— 2CAS Mode —

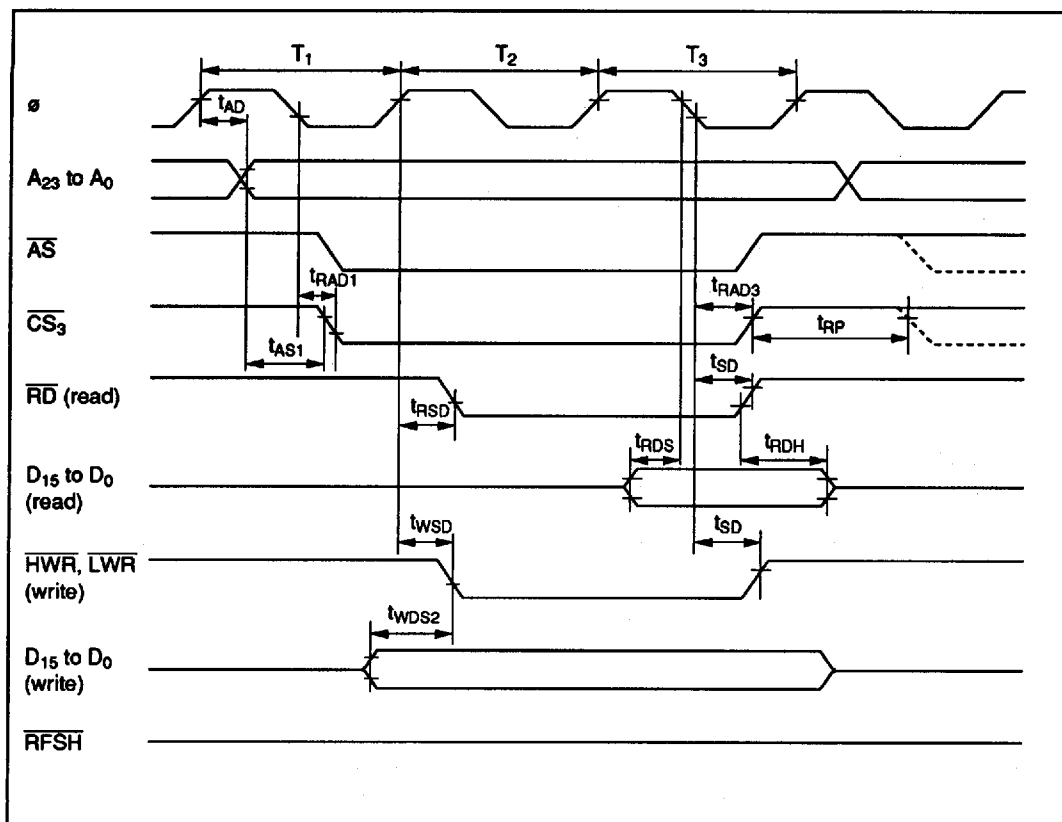


Figure 21-16 PSRAM Bus Timing (Read/Write): Three-State Access

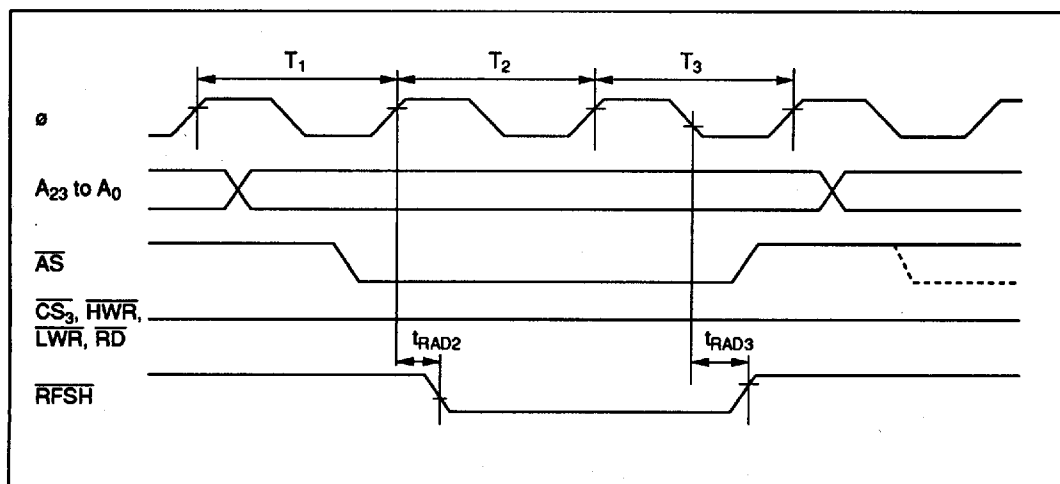


Figure 21-17 PSRAM Bus Timing (Refresh Cycle): Three-State Access

21.4.3 Control Signal Timing

Control signal timing is shown as follows:

- Reset input timing

Figure 21-18 shows the reset input timing.

- Reset output timing

Figure 21-19 shows the reset output timing.

- Interrupt input timing

Figure 21-20 shows the input timing for NMI and $\overline{\text{IRQ}}_5$ to $\overline{\text{IRQ}}_0$.

- Bus-release mode timing

Figure 21-21 shows the bus-release mode timing.

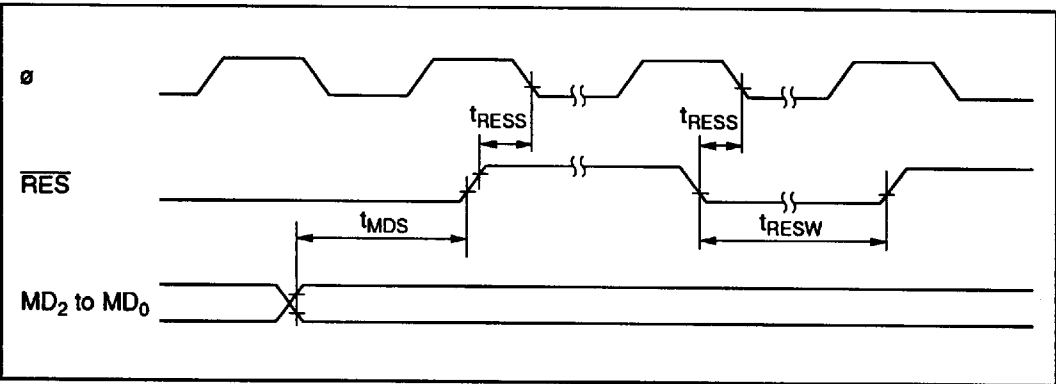


Figure 21-18 Reset Input Timing

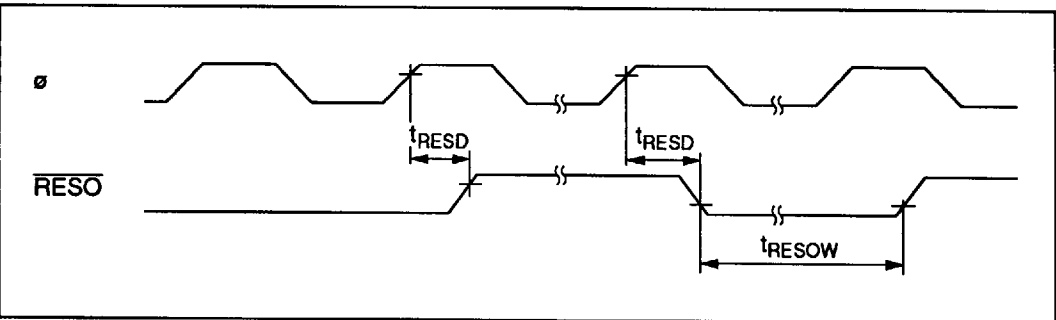


Figure 21-19 Reset Output Timing

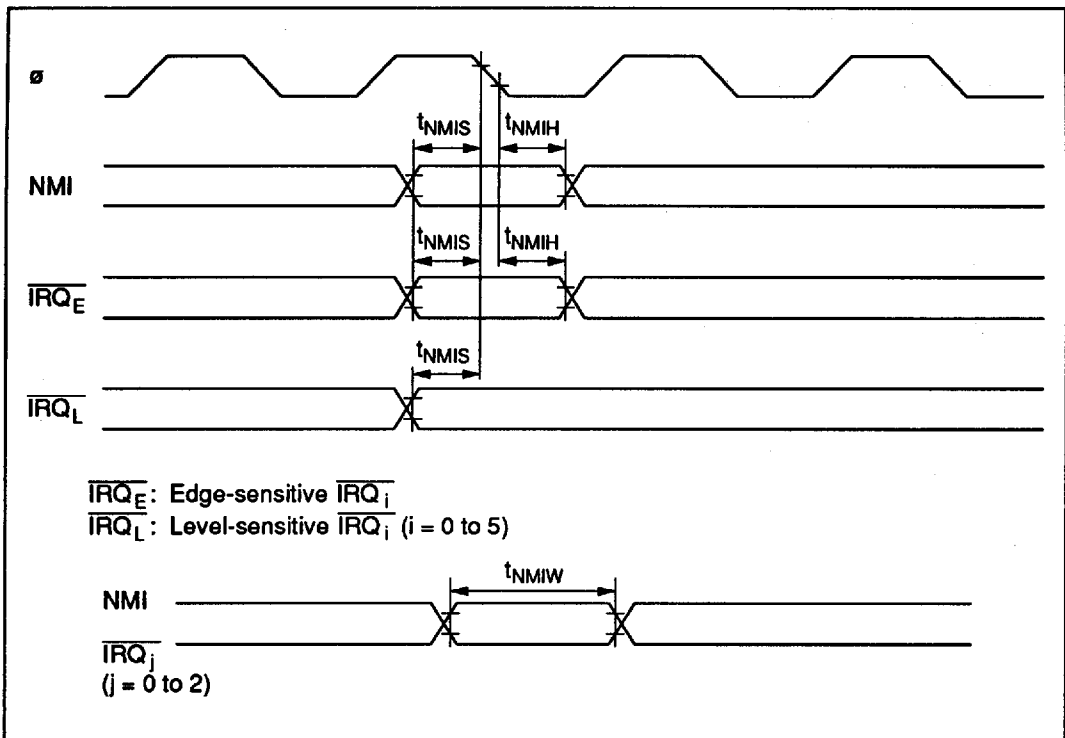


Figure 21-20 Interrupt Input Timing

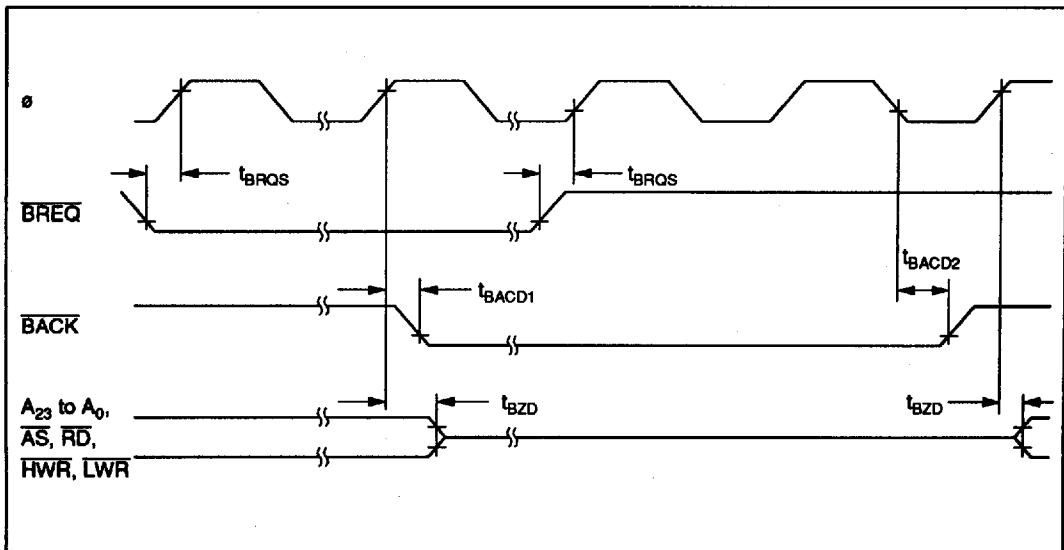


Figure 21-21 Bus-Release Mode Timing

21.4.4 Clock Timing

Clock timing is shown as follows:

- Oscillator settling timing

Figure 21-22 shows the oscillator settling timing.

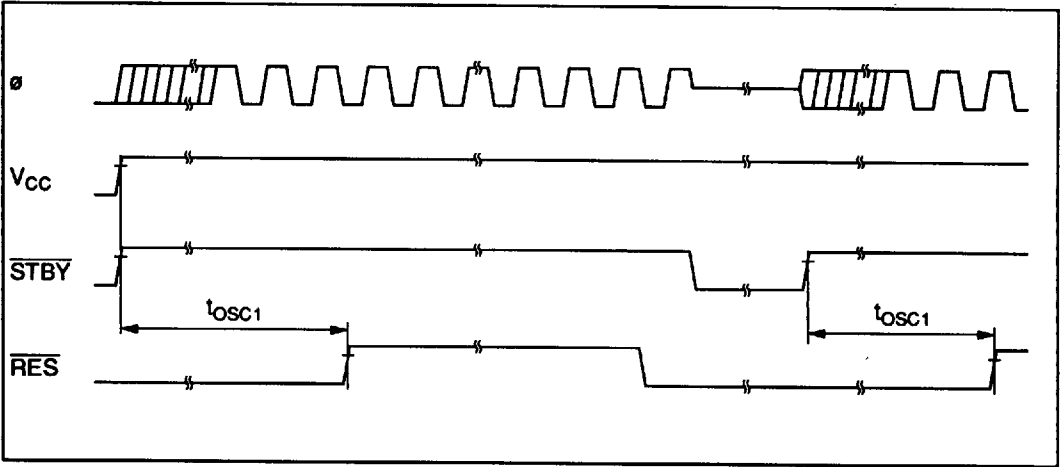


Figure 21-22 Oscillator Settling Timing

21.4.5 TPC and I/O Port Timing

Figure 21-23 shows the TPC and I/O port timing.

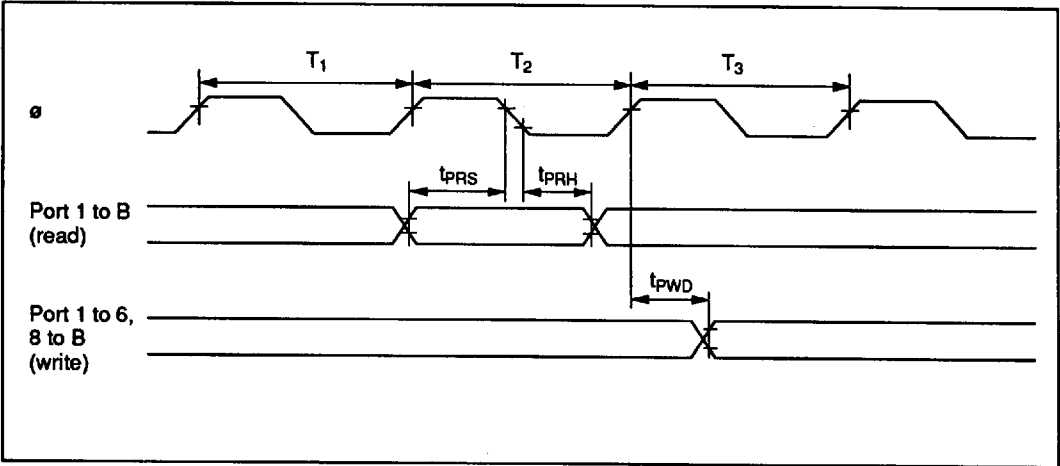


Figure 21-23 TPC and I/O Port Input/Output Timing

21.4.6 ITU Timing

ITU timing is shown as follows:

- ITU input/output timing

Figure 21-24 shows the ITU input/output timing.

- ITU external clock input timing

Figure 21-25 shows the ITU external clock input timing.

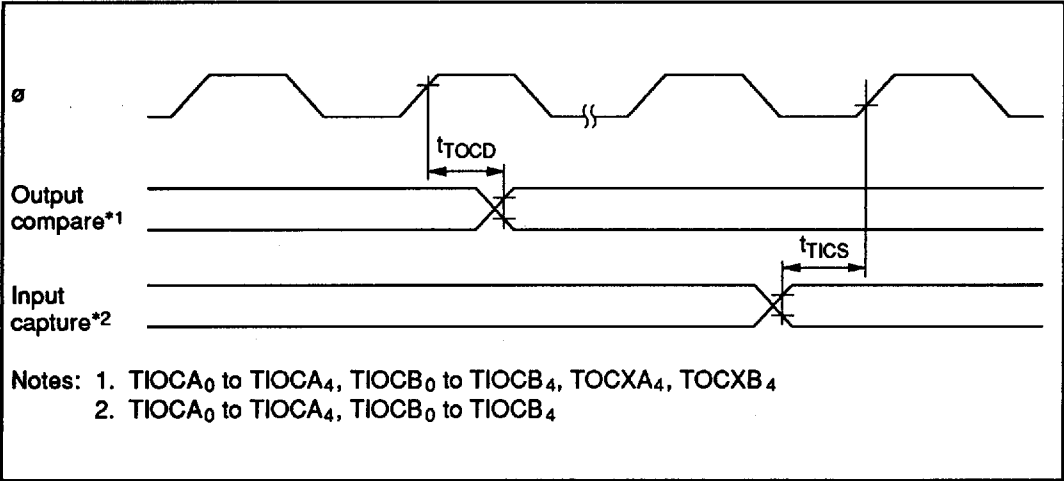


Figure 21-24 ITU Input/Output Timing

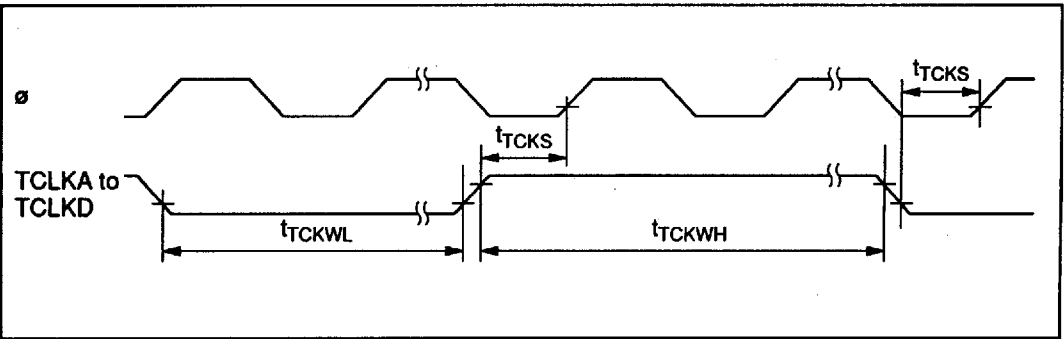


Figure 21-25 ITU Clock Input Timing

21.4.7 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing

Figure 21-26 shows the SCK input clock timing.

- SCI input/output timing (synchronous mode)

Figure 21-27 shows the SCI input/output timing in synchronous mode.

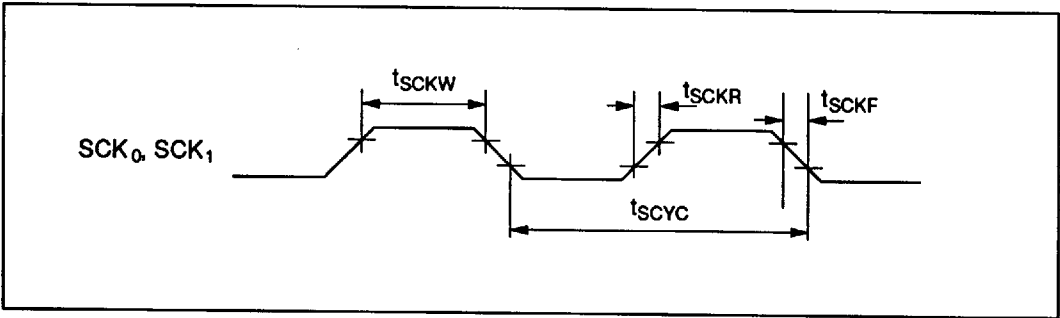


Figure 21-26 SCK Input Clock Timing

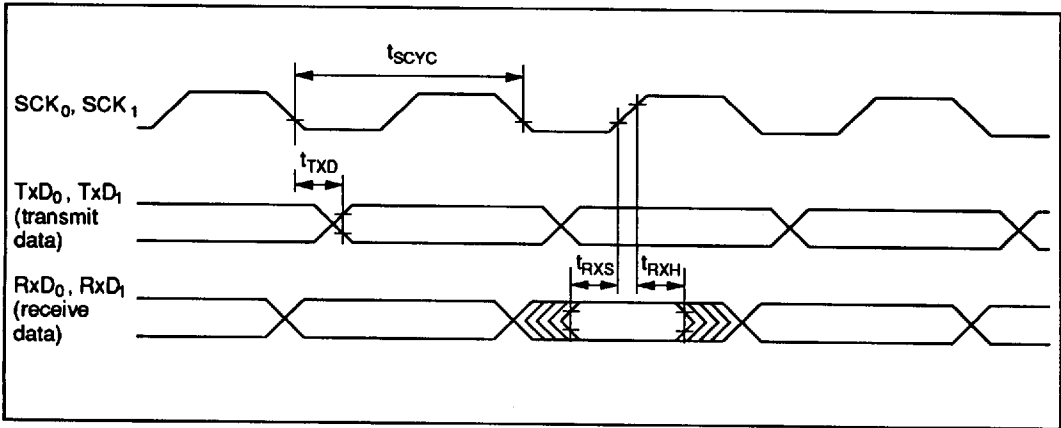


Figure 21-27 SCI Input/Output Timing in Synchronous Mode

21.4.8 DMAC Timing

DMAC timing is shown as follows.

- DMAC $\overline{\text{TEND}}$ output timing for 2 state access

Figure 21-28 shows the DMAC $\overline{\text{TEND}}$ output timing for 2 state access.

- DMAC $\overline{\text{TEND}}$ output timing for 3 state access

Figure 21-29 shows the DMAC $\overline{\text{TEND}}$ output timing for 3 state access.

- DMAC $\overline{\text{DREQ}}$ input timing

Figure 21-30 shows DMAC $\overline{\text{DREQ}}$ input timing.

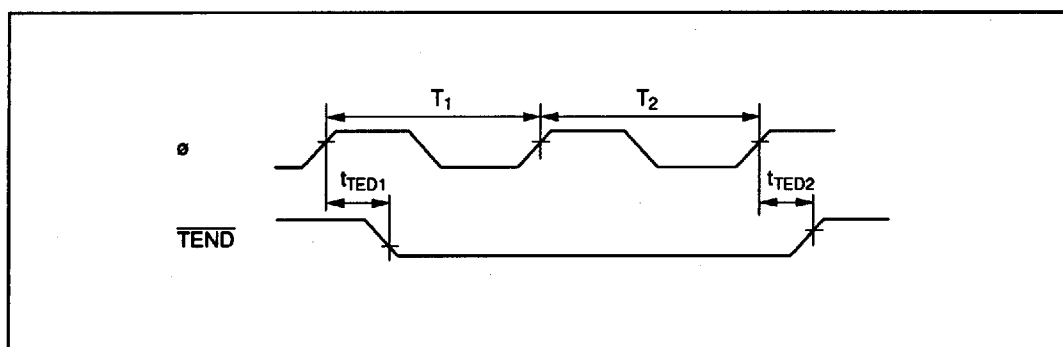


Figure 21-28 DMAC $\overline{\text{TEND}}$ Output Timing for 2 State Access

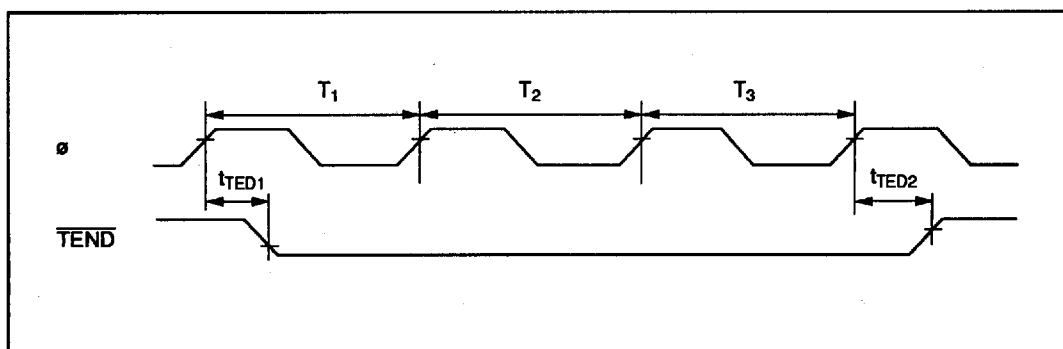


Figure 21-29 DMAC $\overline{\text{TEND}}$ Output Timing for 3 State Access

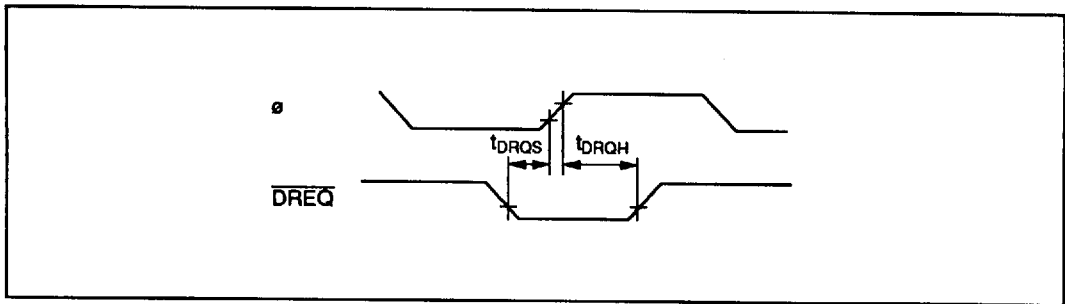


Figure 21-30 DMAC $\overline{\text{DREQ}}$ Input Timing