ZILOG

PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z01701

14,400 BPS Z-FAX MODEM FOR FACSIMILE APPLICATIONS

FEATURES

Part Number	DSP	AFE	Speed (MHz)
Z01701	16-Bit	Integrated	12.5

- ITU-T[1] Group 3 Facsimile Transmit and Receive
  V.17 14400, 12000, 9600, 7200 bps
  V.29 9600, 7200 bps
  V.27ter 4800, 2400 bps
  V.21 (Channel 2) 300 bps
  T.30, T.4
- Combined Data Pump and Analog Front-End (AFE)
- Serial Synchronous Data Port
  RS-232C/V.24 Type Handshake
- HDLC Framing at all Data Speeds
- Parallel 8-Bit Microprocessor Bus Interface
- Direct Memory Access Controller (DMA)
- Low-Power Consumption: 25 mA
- 44-Pin PLCC Package
- Single 5 VDC Power Supply
- 0°C to +70°C Temperature Range

Note:
(1) International Telecommunications Union (ITU), formerly CCITT.

GENERAL DESCRIPTION

The Z01701 Z-Fax Modem is a synchronous 14,400 bits per second (bps) half-duplex modem for use in facsimile applications. This device is specifically designed for use in ITU Group 3 facsimile applications where space, performance, and low-power consumption are key requirements.

Operating over the Public Switch Telephone Network (PSTN), the Z01701 meets the specified ITU Group 3 facsimile standard for V.17, V.29, V.27ter, V.21 Ch. 2, and is compatible with T.4 and T.30 facsimile protocols.

The Z01701 performs HDLC framing according to T.30 at all Group 3 speeds (14,400, 12,000, 9600, 7200, 4800, 2400 and 300 bps). This capability eliminates the need for an external Serial Input/Output (SIO) device in Data Terminal Equipment (DTE) for products incorporating error correction.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip. Automatic and selectable compromise equalizers are included to optimize performance.

The Z01701 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers. The host can select among three preset link line equalizers for both amplitude and delay equalization. The host can also select among four preset premises to central office cable equalizers for amplitude and delay equalization.

The Z01701 provides comprehensive selectable and programmable tone generation and detection.

Additionally, by means of software control, the host can select either the parallel or serial interface for synchronous data transfer. All digital I/O signals are TTL compatible. The parallel interface is compatible with standard 8-bit microprocessors, including the Z80 bus interface, allowing direct access to eight I/O registers and indirect access to the modem RAM.

GENERAL DESCRIPTION (Continued)

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control, and programmable coefficients. The serial interface is used only for data transfer and complies with V.24/RS-232C specifications. All control and status information is transferred by means of the parallel interface.

The Z01701 telephone line interface can be wired for either two-wire or four-wire (half-duplex only) operation. The transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer, thereby reducing the external circuits to a minimum.

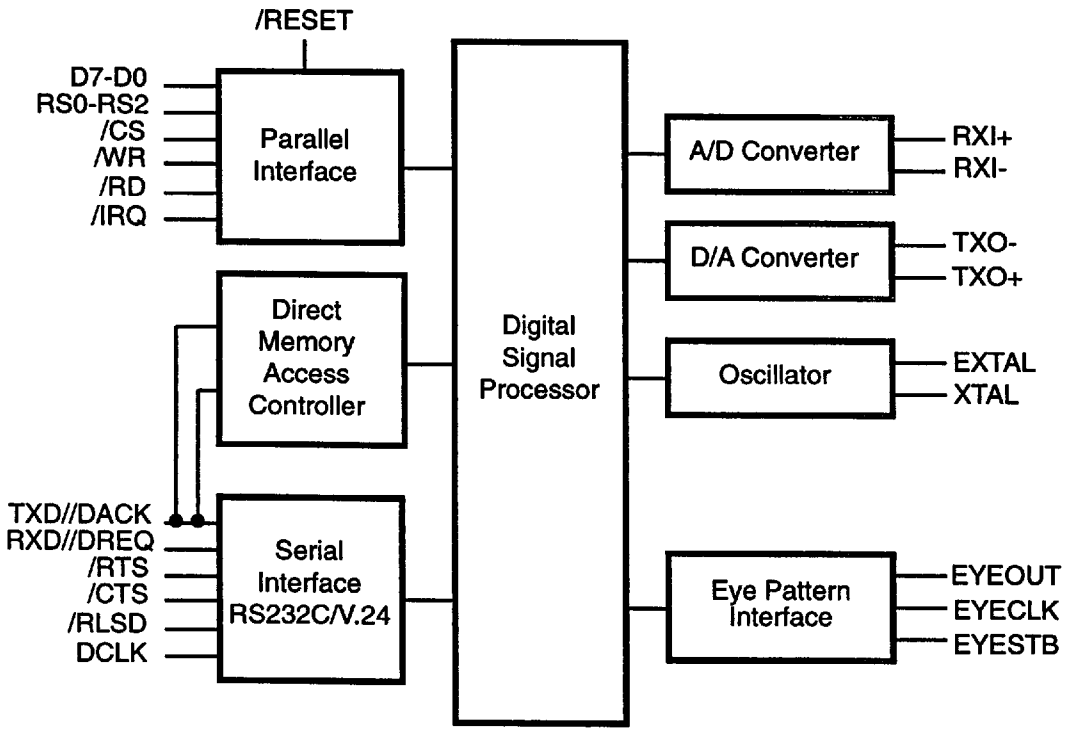
In addition, the Z01701 provides for further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the need for external filtering components.

The Z01701 device operates on a single 5 VDC power supply. During periods of no traffic, the host can place the modem into Sleep mode, reducing power consumption to less than 5 percent of full load power.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Note: /DACK and /DREQ is multiplexed with the TxD and RxD lines.

Figure 1. Z01701 Block Diagram

User Information

The Zilog Z01701 datapump chip can be selected for either parallel or serial synchronous data transfer under software control. Figure 1 shows a block diagram of the general modem chip interface. The hardware and software configurations can be customized for a particular facsimile application. The parallel interface allows direct access to 8 I/O registers, indirect access to the modem RAM, and is compatible with most 8-bit microprocessors, including the Z80. The serial interface is used only for data transfer and complies with V.24/RS232C. All controls and status information are transferred via the parallel interface. The RAM access capability allows to diagnostic data, additional status control, and programmable coefficients. The hardware and software interfaces are presented in the subsequent sections.

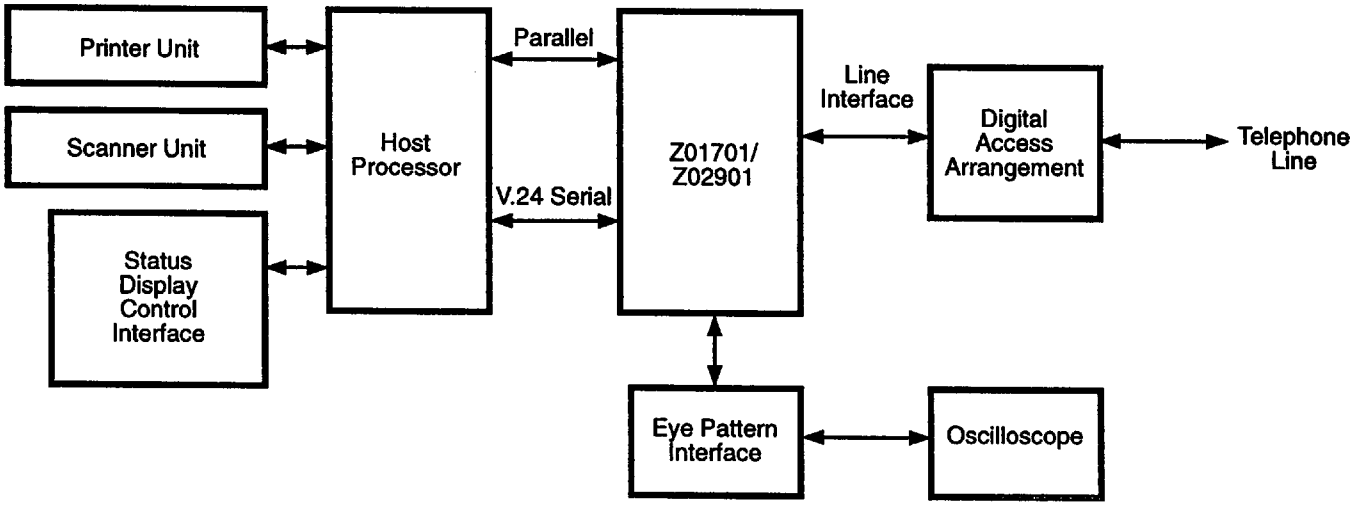


Figure 2. Z01701 System Block Diagram

PIN DESCRIPTION

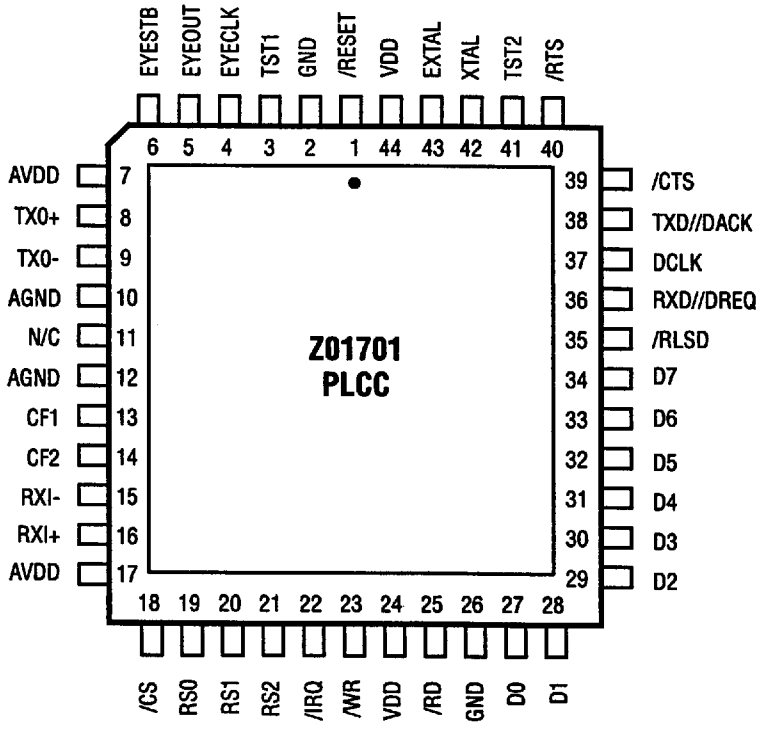


Figure 3. Z01701 44-Lead PLCC Pin Identification

Table 1. Z01701 Modem Pin Assignments

Pin No.	Symbol	Direction
1	/RESET	Input
2	GND	Power and Ground
3	TST1	Input
4	EYECLK	Output
5	EYEOUT	Output
6	EYESTB	Output
7	AV_{DD}	Ground
8	TXO+	Analog Output
9	TXO-	Analog Output
10-12	A_{GND}	Power and Ground
13	CF1	Analog Capacitance
14	CF2	Analog Capacitance
15	RXI-	Analog Input
16	RXI+	Analog Input
17	AV_{DD}	Power and Ground
18	/CS	Input
19	RS0	Input
20	RS1	Input
21	RS2	Input
22	/IRQ	Output
23	/WR	Input
24	V_{DD}	Power and Ground
25	/RD	Input
26	GND	Power and Ground
27	D0	I/O
28	D1	I/O
29	D2	I/O
30	D3	I/O
31	D4	I/O
32	D5	I/O
33	D6	I/O
34	D7	I/O
35	/RLSD	Output
36	RXD//DREQ	Output
37	DCLK	Output
38	TXD//DACK	Input
39	/CTS	Output
40	/RTS	Input
41	TST2	Input
42	XTAL	Output
43	EXTAL	Input
44	V_{DD}	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
T_{OPR}	Operating Temperature	0	70	°C
T_{STG}	Storage Temperature	–65	+150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Parameters will be tested as per the table referencing the DC Characteristics. The Z01701 tester has active loads which are used to test the loading for I_{OH} and I_{OR}

Available operating temperature range is:
S = 0°C to 70°C

Voltage Supply Range:
+4.5 V ≤ V_{CC} ≤ + 5.5 V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines.

POWER REQUIREMENTS

Voltage	Current Typical @ 25°C	Current Maximum @ 0°C
+5 V_{DC}, Operating	50 mA	< = 100 mA
+5 V_{DC}, Sleep	25 µA	< = 125 µA

Notes:

1) DSP Configuration Mode is controlled by the RAM location INSTR. DSP Configuration Mode may be terminated by a parallel write or reset.

2) All voltages are ±5% DC and must have ripple less than 0.1V. peak to peak. If switching supply is used, the frequency may be between 20 kHz and 150 kHz. No component of the switching frequency should be present outside of the supply greater than 500 µV peak.

DC CHARACTERISTICS

Table 1. DC Pin Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Units
Pin Types I & I/O: Input & Input-Output						
V_{IH}	Input High Voltage		2	–	V_{CC} +0.3	V
V_{IL}	Input Low Voltage		0	–	0.8	V
I_L	Input Leakage Current	GND <V0<V_{DD}		–	1.0	µA
Pin Types O & IO: Output & Input-Output						
V_{OH}	Output High Voltage	$I_{OH=}$ -200 mA	2.4	–		V
V_{OL}	Output Low Voltage	I_{OI-} 2.2 mA	0	–	0.4	V
I_{OZ}	Tri-state Leakage Current	GND<V0<V_{DD}	-10	–	10	µA
Pin Types I-PU & I-PD: Input with Internal pull-up/pull-down resistor						
V_{IH}	Input High Voltage		2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage		0		0.8	V
I_L	Input Current	GND <V0<V_{DD}	-10		10	µA
Pin Type XI: Crystal Input						
VIH	Input High Voltage		V_{DD} x0.8	V_{DD}	V	
VIL	Input Low Voltage					
Pin Type O-OD: Output with Open-Drain						
V_{OL}	Output Low Voltage	I_{OI}=2.2 mA	0		0.4	V
I_{OZ}	Tri-state Leakage Current	GND<V0<V_{DD}	-10		10	µA
Pin Type XO: Crystal output						
V_{OH}	Output High Voltage	I_{OH} = 1.0 mA	V_{DD} -1		V_{DD}	V
V_{OL}	Output Low Voltage	I_{OI} = -1.0 mA	0		1	V
Pin Type AI: Analog Input						
V_{DC}	Input Bias Offset		V_{REF} -15	V_{REF}	V_{REF} +15	mV
I_L	Input Current		-100		100	
C_{IN}	Input Capacitance			10	–	pF
R_{IN}	Input Resistance			20		kOhm
Pin Type AO: Analog Output						
VO	Analog Output Voltage		V_{REF} -1.163	V_{REF}	V_{REF} +1.163	mV
V_{OFF}	Output DC Offset		V_{REF} -40	V_{REF}	V_{REF} +40	mV
R_O	Output Resistance		-	0.8	-	Ohm
C_O	Output Capacitance		-	10	-	pF
Z_1	Load Impedance		400	600	Infinite	Ohm
Pin Type PWR: Power and Ground						
V_{DD}	Digital Supply Voltage		4.75	5	5.25	V
GND	Digital Ground	Voltage		–	0	–
AV_{DD}	Analog Supply Voltage		V_{DD}	V_{DD}	V_{DD}	V
	AGND		GND	GND	GND	V
I_{DD1}	Digital Supply Current	Operating	–	45	90	mA
I_{ADD1}	Analog Supply Current	Operating	–	5	10	mA
I_{DD2}	Digital Supply Current	DSP Config. Mode		20	100	µA
I_{ADD2}	Analog Supply Current	DSP Config. Mode		5	25	µA

AC CHARACTERISTICS

Timing Diagrams

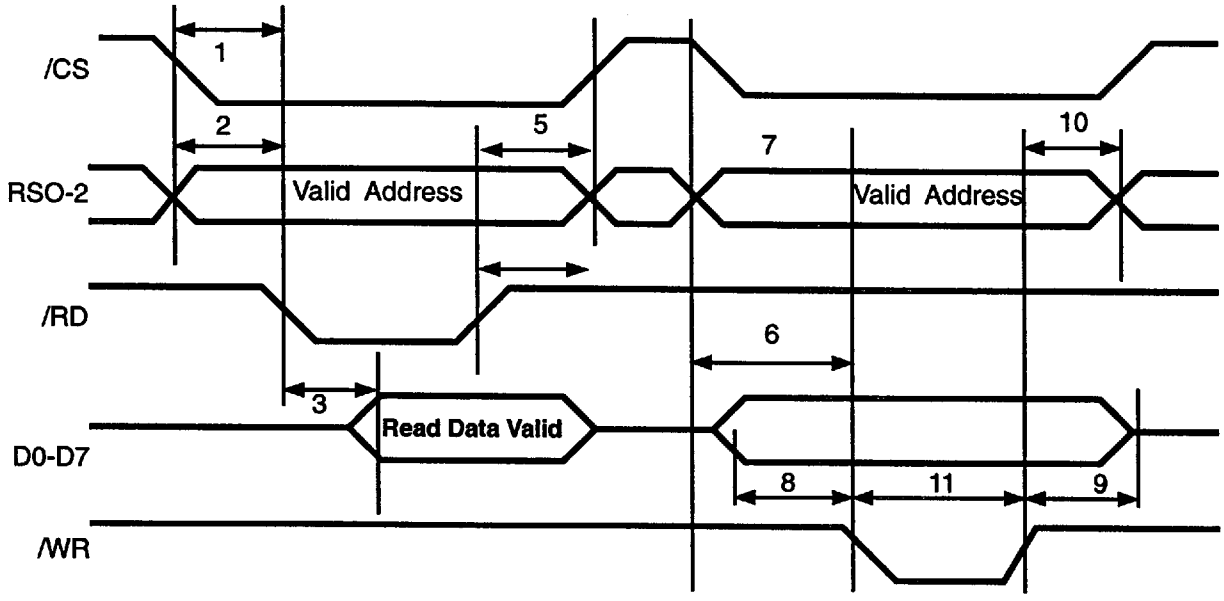


Figure 4. Microprocessor Interface Read/Write Diagram

Table 2. Microprocessor Interface Timing

Description	Parameter	Min	Type	Max	Units
Read Timing					
RSO-2 & /CS to /RD Setup Time	1	0	–	–	ns
RSO-2 to /RD Setup Time	2	0	–	–	ns
/RD to Data Access Time	3	-	25	85	ns
/RD Data Hold	4	0	10	–	ns
RSO-2 and /CS Hold From /RD	5	0	–	–	ns
Write Timing					
RSO-2 & CS to /WR Set-up Time	6	70	–	–	ns
/CS to /WR Setup Time	7	70	–	–	ns
Data to /WR Set-up Time	8	50	–	–	ns
/WR Data Hold	9	10	–	–	ns
RSO-2 and /CS Hold from /WR	10	10	–	–	ns
/WR Pulse Width	11	25	–	–	ns

AC CHARACTERISTICS (Continued)

Timing Diagrams

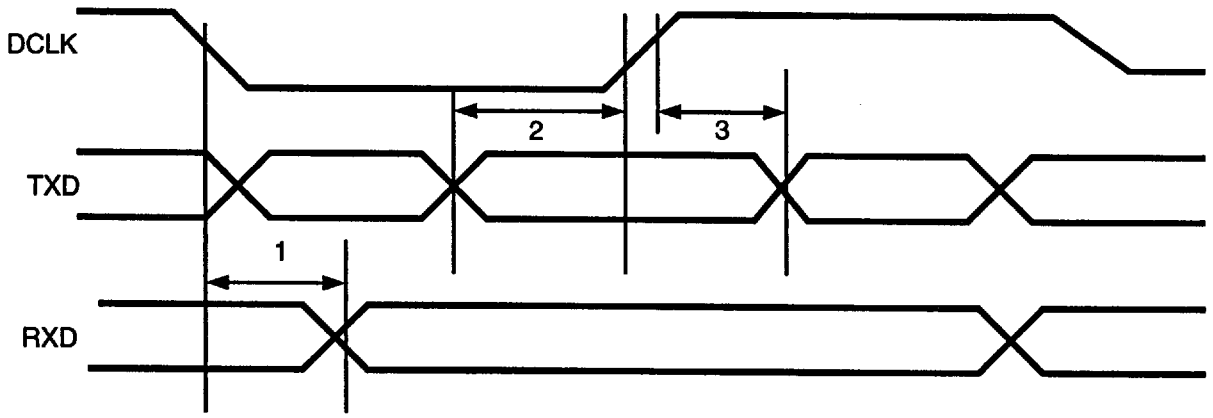
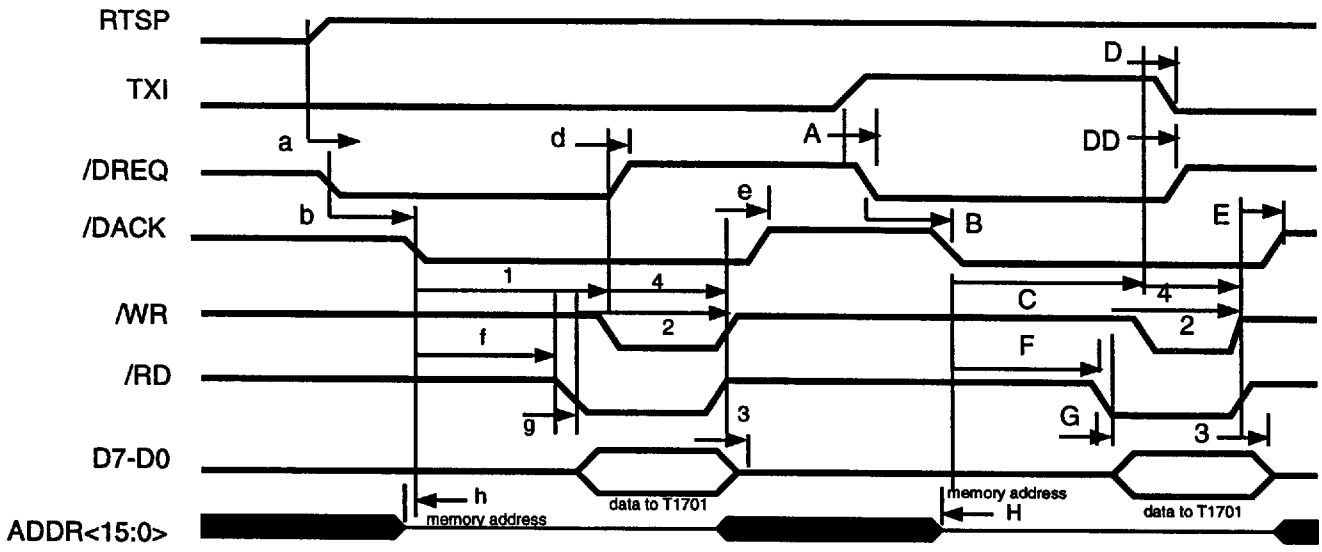


Figure 5. Serial Port Timing Diagram

Table 3. Serial Interface Timing

Description	Parameter	Min	Type	Max	Units
RXD Data Valid Delay Time	1	-	12	-	ns
TXD Data Setup Time	2	100	-	-	ns
TXD Data Hold Time	3	100	-	-	ns



Note: Signals denoted with alphabets are for information and illustrative purposes only. The actual timing is not significant.

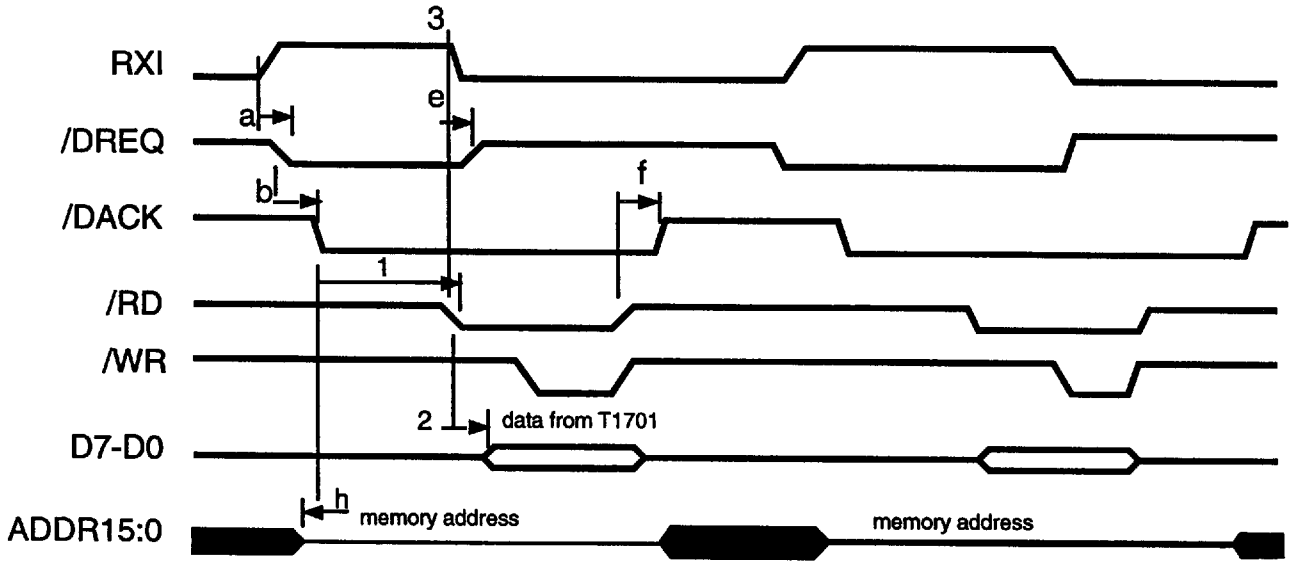
Figure 6. DMA Transmit Mode Diagram

Table 4. DMA Mode Transmit Timing

Description	Parameter	Min	Type	Max	Units
/DACK to /WR set-up time	1	5	-	-	ns
Data set-up to /WR	2	50	-	-	ns
Data hold time after /WR	3	10	-	-	ns
Minimum /WR time	4	20	-	-	ns

AC CHARACTERISTICS (Continued)

Timing Diagrams



Note: Signals denoted with alphabets are for information and illustrative purposes only.
The actual timing is not significant.

Figure 7. DMA Receive Mode Timing Diagram

Table 5. DMA Receive Timing

Description	Parameter	Min	Type	Max	Units
/DACK to /RD set-up time	1	5	–	–	ns
Data access time from /RD	2	50	–	–	ns
/RD to RXI time	3	–	–	10	ns

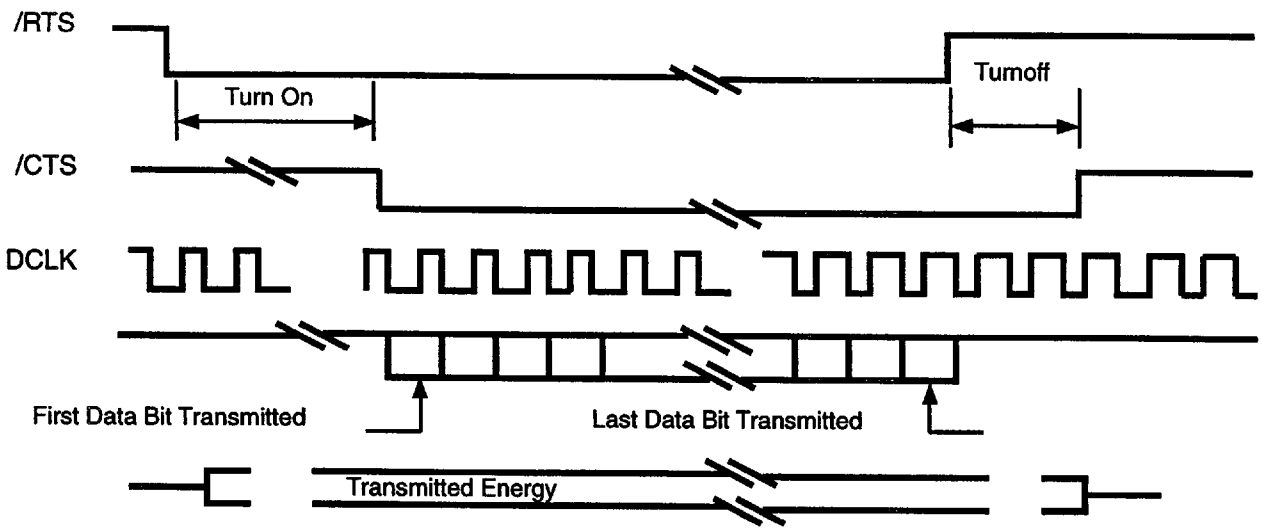


Figure 8. Transmitter Signal Timing Diagram

Table 6. Turn-on and Turn-off Sequences

Config.	RTS on to CTS on Echo Protector Tone Disabled	RTS on to CTS on Echo Protector Tone Enabled	Turn-off from RTS Off Remaining Data Scrambled Ones	Turn-off from RTS Off Silence After Transmitting
V17	TBD	TBD + 207.5	5 ms	20 ms
V.29 (All)	253 ms	461 ms	14 ms	20 ms
V.27 ter 4800	708 ms	916 ms	14 ms	20 ms
V.27 ter 2400	948 ms	1156	14 ms	20 ms
V.21	<= 15 ms	14 ms	14 ms	20 ms

Notes:
Echo protect is enabled through the RAM location CONTROL Echo protect tone is not generated for V.21. Echo protect tone consists of 187.5 ms unmodulated carrier followed by 20 ms of silence.

Turn-on is initiated by an off to on transition of RTS. CTS is asserted at the end of the turn-on sequence. Turn-off is initiated by an on to off transition of RTS. RX is asserted at the end of the turn-off sequence.

AC CHARACTERISTICS (Continued)

Timing Diagrams

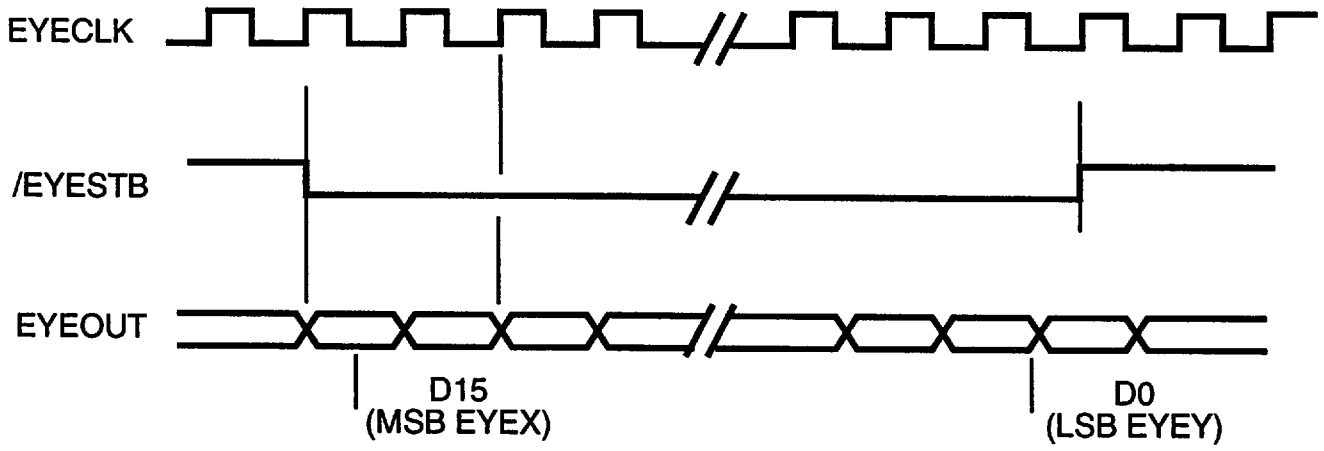


Figure 9. Eye Pattern Port Timing Diagram

Table 7. Analog Characteristics Table

Description	Parameter	Min	Type	Max	Units
Input impedance of interface	1	400	1200	–	Ohm
3 dB point of interface	2	21	26.5	32.5	kHz
External integration capacitance Type NPO (COG)	3	73	82	90	pF

ANALOG INPUTS: TYPE AI

Characteristics	Sym	Min	Type	Max	Units
Input Impedance (DC to V_{REF})	Z_{IN}	15K	25K	–	Ω
Power Supply Rejection	P_{SRRi}	40	–	–	dB
Input Current	I_i	-80	–	80	µA
Input Offset (differential)	V_{OFFI}	-20	0	+20	mV
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNi}	–	–	-72	dbm
Signal to Distortion	S_{TDi}	30	–	–	dB

These characteristics below are provided for information only. They are not tested except in the functional test vectors.

Characteristics	Sym	Min	Typ	Max	Units
Input Capacitance	C_{IN}	–	10	–	pF
Input Bias	V_{DCOFF}	–	+2.5	–	V
Analog Input Voltage (peak differential), (23)	V_{PKI}	-2.362	–	+2.362	V
Analog Input Voltage (per RX-. RX- pin)	V_{PKIP}	-1.181	–	+1.181	V

ANALOG OUTPUTS: TYPE A0

Characteristics	Sym	Min	Type	Max	Units
Output DC Offset (differential)	V_{OFFO}	-40	0	+40	mV
Power Supply Rejection	P_{SRRO}	40	–	–	dB
Signal to Distortion	S_{TDO}	35	–	–	dB
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNO}	–	–	-72	dBm
Out of Band Noise	N_{qo}				dBm
4-8 kHz		–	–	-20	
8-12 kHz		–	–	-40	
12 kHz and above in 4 kHz bandwidths		–	–	-55	

Characteristics	Sym	Min	Typ	Max	Units
Output Impedance	Zout	–	0.80	–	Ω
Output Capacitance	Cout	–	10	–	pF
Analog Output Voltage (peak differential), (24)	Vpko	-2.375	–	+2.375	V
Load Impedance (25)	ZI	400	600	–	Ω

CONFIGURING AS A TRANSMIT FACSIMILE DATA MODEM

The Z1701 can be configured to be a data transmitter as follows:

- Put the modem into DSP Configuration mode by writing the DSP configuration RAM (RAM # 01FFH) following the procedure for DSP RAM write.
- Read the Configuration RAM. The Configuration RAM should contain the DSP Configuration code. While in DSP Configuration, select the desired options (such as link line and cable equalizers) and enable these options by setting the appropriate bits in the control RAM following the DSP RAM write procedure.
- Select either parallel controller-to-DSP or serial controller-to-DSP transmit data transfer by setting the TDPM bit of RAM control register (Reg 4.4 bit) to 0 for parallel transfer or 1 for serial transfer.
- Activate the RTS* pin low or set the RSTP bit of the RAM control register (Reg 4.3) to logic 1.
- For parallel controller-to-DSP transmit data transfer, write the first byte to be transmitted to the DATAP register (Reg 3).
- Write the desired speed code to the configuration RAM from the configuration table.

Every byte period the modem will read the controllers transmit data from the transmit DATAP register (Reg 3). The controller can monitor when to update the data in the DATAP register in one of two ways (CASES):

Case 1:
Polling:

The controller can monitor when to update the data in DATAP register by polling the TXI bit of the DSP's Modem Status register (Reg 5.7). Whenever this bit is set then the controller can write a new byte to the DATAP register.

Case 2:
Interrupts (recommended):

The controller can monitor when to update the data in DATAP register by the more efficient interrupt method. In this case the IRQ* pin should be connected to one of the controller's interrupt input pin. The DSP IRQ* pin is an open-drain low output pin. The TXIE bit of the DSP RAM control register (Reg 4.7) should be enabled. Whenever the modem reads the DATAP register the controller will be interrupted. The controller should then read DSP's Modem Status register (Reg 5) and check the TXI bit (Reg 5.7). If the TXI bit is set to logic 0 then the controller can write the new byte to the DATAP register.

Note that it is important that the data in DATAP register be update as soon as possible after the DSP has read the old data because the DSP will simply retransmit the old data if the DATAP is not update on time. The fastest the DSP can service the DATAP register is very 1/2400 Hz.

Termination of transmit operation:

To terminate the transmit operation gracefully, the controller should set the RTSP bit of the DSP's modem control register (Reg 4.3) to 0 and set the external RTS* pin high (5.00 volts).

DSP Response to transmit termination:

Following the termination of the transmit instruction, the DSP will initiate the turnoff sequences. The turnoff sequence includes transmission of a sequence of binary 1's to flush the transmit filter buffers. At the completion of the turnoff sequences the DSP will go into receive mode at the selected speed. The controller should monitor the RX bit of the DSP's modem status register (Reg 5.4) to know when the modem has completed the turnoff sequence. The RX bit is always set to binary 0 whenever the DSP is in transmit mode and to binary 1 whenever the DSP is in standby or receive mode where mode is determined by the state of the logical or of the external RTS* pin and the RTSP bit (Reg 4.3).

CONFIGURING AS A TRANSMIT FACSIMILE DATA MODEM (Continued)

Table 8. Configuration

Value	Bit Rate	Baud Rate	Carrier Frequency	Valid Mode	ITU-T Type
0000				Standby	
0001	300 bps	300 sps	1750 Hz	transmit/receive**	V.21 ch 2
0002	14400 bps	2400 sps	1800 Hz	transmit/receive**	V.17-14400
0003	12000 bps	2400sps	1800Hz		V.17-12000
0004	9600 bps	2400sps	1700Hz		V.29-9600
0005	7200 bps	2400sps	1700Hz	transmit/receive**	V.29-7200
0006	Reserved	Reserved	Reserved	Reserved	Reserved
0007				transmit/Receive**	Tone/DTMF
0008	4800bps	1600sps	1800Hz	transmit/Receive	V.27ter-4800
0009	2400bps	1200sps	1800Hz	transmit/Receive**	V.27ter-2400
000A	9600bps	2400sps	1800Hz	transmit/Receive**	V.17-9600
000B	7200bps	2400sps	1800Hz	transmit/Receive**	V.17-7200

Notes:

* The constants associated with value are in Hexadecimal.

** To effect receive operation RTS* must be high (5.00 volts) and the RTSP bit (Reg 4.3) must be set to logic 0. If either the RTS* is activated or the RTSP bit is high then transmit operation is effected.

CONFIGURING AS A TONE/DTMF TRANSMITTER

The Z1701 can be configured as a TONE/DTMF transmitter as follows:

- Put the modem in standby mode by writing the STANDBY code to the Configuration RAM (RAM # 01FFH) following the procedure for DSP RAM write.
- Read the Configuration RAM. The Configuration RAM should contain the standby code. While in standby, select the desired tone or DTMF frequency to be transmitted by setting the appropriate bits in the TONE control RAM (RAM# 01FBh) following the DSP RAM write procedure.
- Activate the RTS* pin low or set the RSTP bit (Reg 4.3) of the RAM control register to logic 1. The USER programmable tones must be programmed before writing the TONE/DTMF code to the configuration RAM to effect use of the programmed tones. Once programmed, the constants remain in the DSP memory until reset or reprogrammed by the host.

The tone codes are as defined below in the TONE CODE table. In addition to 13 preprogrammed tone frequencies, the controller can program 3 additional tones for a total of 16 tones. The tone frequency can be determined from

$$Ft=(Fc/9600) *1024 *64$$

where $300 \leq Fc \leq 3300$ and Ft is rounded to the nearest integer. (1)

The computed Ft should be written to any one of the three user programmable tone transmit RAM (USRTXN1--USRTXN3). These RAM addresses corresponds to RAM 01F4H-01F6H in the same order. To select USRTXN1 for tone transmission, write 8000h to TONE RAM and using (1) compute the desired digital frequency constant. Write the hexadecimal equivalent of this constant to USRTXN1 RAM (RAM # 01F4). To select any one of the predefined T.30 signalling group frequencies, select the desired frequency from the TONE CODE table by writing the corresponding value to the TONE RAM (RAM # 01FBH). To effect DTMF transmission, select any two of the DTMF group frequency Value (Logical OR of the corresponding bits) and write this value to the TONE RAM.

Table 9. Tone Code (RAM# 01FBH)

TONE RAM Value[1]	Frequency Selected
8000	USER1 (default 400 Hz)
4000	USER2 (default 300 Hz)
2000	USER3 (default 3300 Hz)
1000	2100 Hz (CED)
0800	1100 Hz (CNG)
0400	462 Hz (PIS)
0200	1850 Hz
0100	1650 Hz
0080	697 Hz (DTMF Low)
0040	770 Hz (DTMF Low)
0020	852 Hz (DTMF Low)
0010	941 Hz (DTMF Low)
0008	1209 Hz (DTMF High)
0004	1333 Hz (DTMF High)
0002	1477 Hz (DTMF High)
0001	1633 Hz (DTMF High)

Note: The TONE RAM selection constants are in hexadecimal format. Logical OR of any of the DTMF group bits will produce the corresponding DTMF pair.

CONFIGURING AS A RECEIVE DATA MODEM

The Z1701 can be configured as a receiver follows:

- Put the modem in standby mode by writing the STANDBY code to the Configuration RAM (RAM # 01FFh) following the procedure for DSP RAM write.
- Read the Configuration RAM. The Configuration RAM should contain the standby code. While in standby, select the desired options (such as compromise link line equalizer, cable equalizer and the T space adaptive equalizer) and enable these options by setting the appropriate bits in the control RAM following the DSP RAM write procedure.
- Reset the RTS* pin by setting the RTS* pin high (5.0 volts) and reset the RSTP bit (b3) of the RAM control register (Reg 4) to logic 0.
- Write the desired speed code to the configuration RAM from the configuration table.

Every byte period the modem will update the DATAP register (Reg 3) with received byte. The received bit stream is simultaneously presented to the serial port. The controller can monitor when the data in DATAP register has been update by the DSP in one of two ways (CASES):

Case 1:
Polling:
The controller can monitor when the data in DATAP register has been update by the DSP by polling the RXI bit of the DSP's Modem Status Register (Reg 5). Whenever this bit is set then the controller can read the new received byte from the DATAP register.

Case 2:
Interrupts (Recommended)
The controller can monitor when the data in DATAP register has been update by the DSP by the more efficient interrupt method. In this case the IRQ* pin should be connected to one of the controller's interrupt input pin. The DSP IRQ* pin is an open-drain active low output pin. The DRXIE bit of the DSP DMA register (Reg 6) should be enabled. Whenever the DSP writes the DATAP register the controller will be interrupted. The controller should then read the DSP's Modem Status register (Reg 5) and check the RXI bit (b6). If the RXI bit is set (set to logic 1) then the controller should read the new byte of received data from the DATAP register.

Note that it is important that the data in DATAP register be read as soon as possible after the DSP has updated the DATAP register with the new received byte because the DSP will simply overwrite the old data if the DATAP has not been read by the controller. The fastest the DSP can service the DATAP register is every 1/2400 Hz.

CONFIGURING AS A TONE RECEIVER

The Z1701 is designed to detect any five or sixteen frequencies. Three of these frequencies can be programmed by the controller. The thirteen non-programmable frequencies includes all of the eighth DTMF frequencies as well as the five most important T.30 signalling frequencies. The three programmable frequencies can be used to effect call progress monitoring.

The Z1701 can be configured as a TONE/DTMF receiver as follows:

- Put the modem in mode by writing the DSP Configuration code to the Configuration RAM (RAM # 01FFH) following the procedure for DSP RAM write.
- Read the Configuration RAM. The configuration RAM should contain the DSP configuration code. Then while in DSP Configuration Mode, program the three USER programmable tone detect frequency constants that you desired to detect. The default frequencies to be detected are shown in the DETECT CODE below.
- Reset the RTS* pin by setting the RTS* pin High (5 volts) and reset the RSTP bit (b3) of the RAM control register (Reg 4) to logic 0.
- Write the TONE/DTMF configuration code to the configuration RAM from the configuration table.

The USER programmable detect tones must be programmed before writing the TONE/DTMF code to the configuration RAM to effect use of the programmed detect tones. Once programmed, the constants remain in the DSP memory until reset or reprogrammed by the host.

The detect tone codes are as defined below in the DETECT CODE table. In addition to 13 preprogrammed tone frequencies, the controller can program 3 additional detect tones for a total of 16 detect tones. The detect tone frequency can be determined from

$$Fd = \cos(2\pi\, Fc/9600) * 32767$$

where $300 \leq Fc \leq 3300$ and Fd is rounded to the nearest integer.

The computed Fd should be written to any one of the three user programmable detect tone receive RAM (USRRXN1-USRRXN3). These RAM addresses corresponds to RAM 01F7H-01F9H in the same order. To program USRRXN1 to detect 245 Hz, using (2) compute the desired digital frequency constant to be detected. Write the hexadecimal equivalent of this constant to USRRXN1 RAM (RAM # 01F7). To detect any one of the predefined T.30 signalling group frequencies, or the predefined DTMF frequencies write the TONE/DTMF configuration code to the configuration RAM. The DTMF/TONE detector is capable of detecting five unique frequencies. So instead of a DTMF frequency pair, if a multi-tone frequency is sent, the DTMF/TONE detect is capable of detecting five of the frequency. If more than five unique frequencies are present, then the DTMF/TONE detector will declare the frequencies invalid. The DTMF/TONE detector is capable of resolving ±37 Hz for frequencies greater than 500 Hz and is capable of resolving ±50 Hz for frequencies between 200 Hz and 500 Hz. The bits indicating the detected frequencies are contained in the DETEC RAM (RAM # 01FAH). Each bit position represents the frequency detected. When multiple frequencies are detected, the corresponding bits are set. Up to 5 bits may be set.

Table 10. Detect Code Table (RAM # 01FAH)

DETECT RAM Value[1]	Frequency Detected
8000	USER1 (default 400 Hz)
4000	USER2 (default 300 Hz)
2000	USER3 (default 3300 Hz)
1000	2100 Hz (CED)
0800	1100 Hz (CNG)
0400	462 Hz (PIS)
0200	1850 Hz
0100	1650
0080	697 Hz (DTMF Low)
0040	770 Hz (DTMF Low)
0020	852 Hz (DTMF Low)
0010	941 Hz (DTMF Low)
0008	1208 Hz (DTMF High)
0004	1333 Hz (DTMF High)
0002	1477 Hz (DTMF High)
0001	1633 Hz (DTMF High)

Notes: The DETECT RAM constants are in hexadecimal format. Detection of multiple frequencies will set the corresponding bits.

USING THE TONE RECEIVER FOR CALL PROGRESS MONITORING

The Z1701 DTMF/TONE detector can be used to effect the call monitoring function often associated with the T.30 protocol. The most important call progress functions associated with the T.30 handshake is the detection of the busy tone and the off hook tone. The tone frequencies associated with the call progress is in between 250 Hz to 650 Hz. The major distinguishing characteristics of the call progress tones is the cadence of the tones. The busy tone and the offhook tones are not part of the default tone detection frequencies the controller must use the programmable detect tone features of the DTMF/TONE detector. The DTMF/TONE detector can be programmed to detect the call progress tones as follows:

Write the DSP Configuration code to the configuration RAM to put the DSP in DSP Configuration Mode. Divide the call progress tone frequency range of 250 Hz to 650 Hz into two sets. The first set will cover a frequency range of 250 Hz to 450 Hz and the second set will cover 450 Hz to 650 Hz. Program the three receive user programmable tone detector RAM locations (USRRXTN1[01F7H]-USRRXTN4(01F9h) using the equation:

$$Fd=[\cos(2\pi\, Fc/9600) * 32767]$$

where $300 \leq Fc \leq 3300$ and Fd is rounded to the nearest integer.

The three associated center frequencies to cover the frequency range of 250 Hz to 450 Hz are Fc1=285 Hz, Fc2=355 Hz and Fc3=425 Hz. These are computed and written to the 3 user programmable receive tone detection RAM (USRRXN1[01F7h)--USRRXN3[01F9H]). The controller should then monitor the DETECT RAM. The status of the DETECT RAM is update every 128 samples. Where a sample time is 1/9600 Hz. Similarly for the frequency range 450 Hz to 650 Hz the frequency range can be appropriately split to and centered to cover the 450 Hz to 650 Hz. Again the controller can monitor the DETECT RAM to measure the frequency and the cadence of the frequency detected. The controller should alternate between these two frequency bands until a tone is detected or until timed out. The timeout can be more stringent than that allowed by the T.30 specifications.

If the tone signal is guaranteed to be great than 35 dBm then the frequency band between 250 Hz to 650 Hz can be split in 3 with the appropriate center frequencies written to the three user programmable receive tone detection RAM.

Because the call progress tones ranges and cadence are country dependent the detailed measurements for the call progress frequencies should be programmed option determined by the controller.

Development Projects:
Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this project.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

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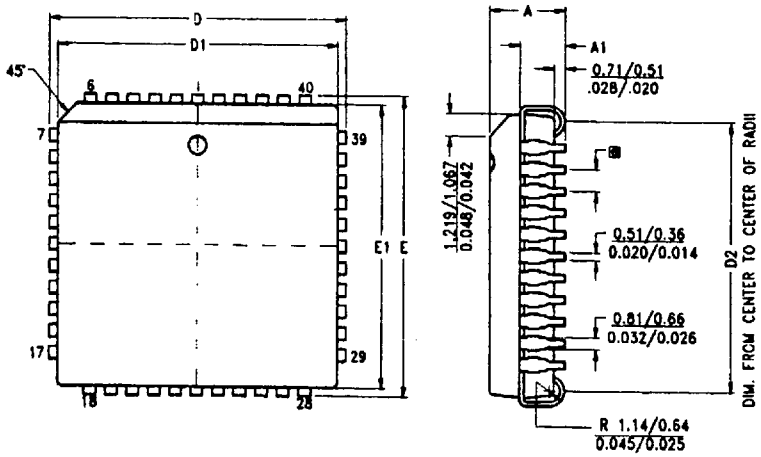
Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056

PACKAGE INFORMATION

PLCC (Plastic Leaded Chip Carrier)

1. Solderability — MIL-STD-883C Method 2003.5
   Eight Hours Steam Age
2. Mark Permanency — 3X soak into Alpha 2110 at 63-70°C.
   30 sec. duration each soak.
   Mech. brush after each soak
3. Coplanarity — Maximum 4 mils deviation



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
■	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

44-Lead Plastic Leaded Chip Carrier (PLCC)