NEC
NEC Electronics Inc.

μPD72001
CMOS, Advanced Multiprotocol, Serial Communications Controller

T-75-37-07

Description

The μPD72001 advanced multiprotocol serial controller (AMPSC) is a high-performance, single-chip, serial communications controller designed to meet a wide variety of communications requirements. The AMPSC contains two independent full-duplex channels which can be configured to transmit and receive data in either asynchronous protocol or one of two synchronous protocols: character-oriented protocol (COP) or bit-oriented protocol (BOP). The COP and BOP synchronous protocols include cyclic redundancy check (CRC) generation and checking.

The AMPSC has several interrupt modes, including vectored and nonvectored. Separate direct memory access (DMA) requests are available for the transmitter and receiver on each channel, allowing high speed operation. The AMPSC is easily interfaced to most microprocessors with a minimum of logic.

The μPD72001 AMPSC is an upgraded CMOS version of the μPD7201A MPSCC with the following additions: four internal baud rate generator (BRG)/timers, two digital phase-locked loops (DPLL), two crystal oscillators, and the capability of synchronous data link control (SDLC) loop operation. The BRG's can be used as independent timers, when they are not being used as baud rate generators. Each timer generates its own zero count interrupt. These features simplify design requirements and at the same time enhance the flexible architecture of the μPD7201A.

Features

- ☐ Advanced version of the μPD7201A
- ☐ Functional superset of industry standard 8530
- ☐ CMOS technology
- ☐ Multiprotocol
  - — Asynchronous
  - — Synchronous
  - — Character-oriented (BISYNC/MONO-SYNC)
  - — Bit-oriented (SDLC/HDLC)
- ☐ Two independent full-duplex channels
- ☐ Versatile host-system interface
  - — Software polling
  - — Interrupt
  - — DMA
- ☐ Interface to a majority of microprocessors (V-Series, 8080, 8085, 80X86/88, and others)
- ☐ DC to 2.2-Mb/s data rate
- ☐ Modem control signals
- ☐ NRZ, NRZI, and FM encoding/decoding, Manchester decoding
- ☐ Digital phase-locked loop per channel
- ☐ Two baud rate generator/timers per channel (receive and transmit)
- ☐ Crystal oscillator per channel
- ☐ Loopback test mode
- ☐ SDLC loop mode
- ☐ Mark idle detection
- ☐ Short frame detection
- ☐ Single +5 V power supply
- ☐ Standby mode for reduced power consumption
- ☐ Two speed versions: 8 MHz and 11 MHz systems and input data clocks
- ☐ Available in DIP, PLCC, and quadflat packages

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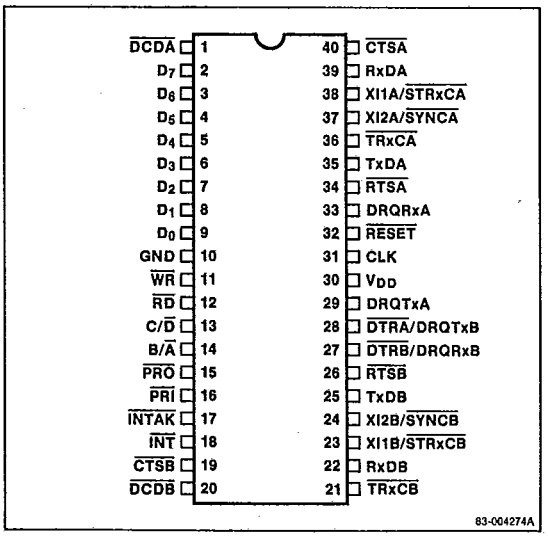
Ordering Information

Part No.	Package Type	Max Clock Speed
μPD72001C	40-pin plastic DIP	8 MHz
μPD72001C-11	40-pin plastic DIP	11 MHz
μPD72001GC-3B6	52-pin plastic miniflat	8 MHz
μPD72001GC-3B6-11	52-pin plastic	11 MHz
μPD72001L	52-pin plastic leaded chip carrier (PLCC)	8 MHz
μPD72001L-11	52-pin plastic leaded chip carrier (PLCC)	11 MHz

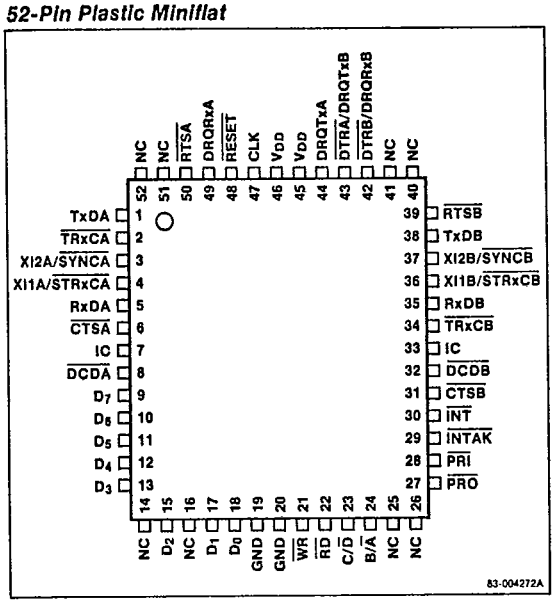
Pin Configurations

40-Pin Plastic DIP

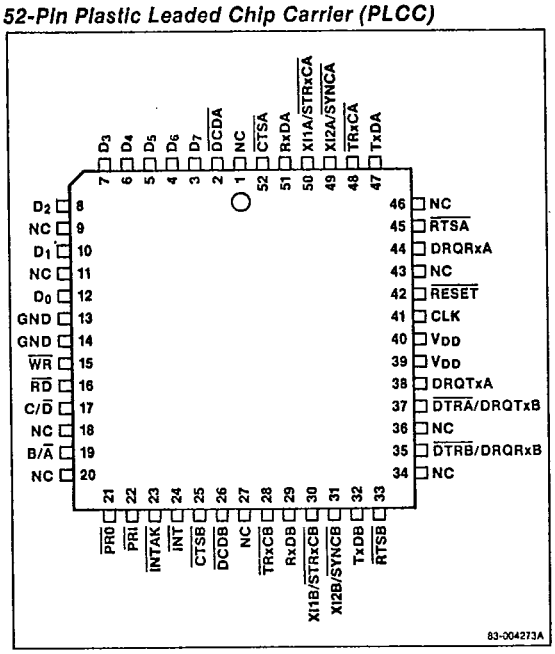


Pin Configurations (cont)

52-Pin Plastic Miniflat



52-Pin Plastic Leaded Chip Carrier (PLCC)



Pin Identification

Symbol	Function
B/$\overline{A}$	Channel B or channel A select input from host computer
C/$\overline{D}$	Control/data input select from host computer
CLK	System clock input from host computer
$\overline{CTSA}$	Clear-to-send input for channel A
$\overline{CTSB}$	Clear-to-send input for channel B
$\overline{DCDA}$	Data carrier detect input for channel A
$\overline{DCDB}$	Data carrier detect input for channel B
$\overline{DTRA}$/DRQTxB	Data terminal ready output for channel A or DMA request output for transmit channel B; determined by control register CR2A
$\overline{DTRB}$/DRQRxB	Data terminal ready output for channel B or DMA request output for receive channel B; determined by control register CR2A
DRQRxA	DMA request output for receive channel A
DRQTxA	DMA request output for transmit channel A
D_7-D_0	System data bus
$\overline{INT}$	Interrupt request output to host computer
$\overline{INTAK}$	Interrupt acknowledge input from host computer
$\overline{PRI}$	Priority input, interrupt daisy chain control
$\overline{PRO}$	Priority output, interrupt daisy chain control
$\overline{RD}$	Read control input from host computer
$\overline{RESET}$	System reset input from host computer
$\overline{RTSA}$	Request-to-send output for channel A
$\overline{RTSB}$	Request-to-send output for channel B
RxDA	Receive data input for channel A
RxDB	Receive data input for channel B
$\overline{TRxCA}$	Transmit-receive clock input for channel A
$\overline{TRxCB}$	Transmit-receive clock input for channel B
TxDA	Transmit data output for channel A
TxDB	Transmit data output for channnel B
$\overline{WR}$	Write control input from host computer
XI1A/$\overline{STRxCA}$	External crystal connection for channel A or transmit-receive clock source input for channel A
XI2A/$\overline{SYNCA}$	External crystal connection for channel A or synchronization input for channel A
XI1B/$\overline{STRxCB}$	External crystal connection for channel B or transmit-receive clock source input for channel B
XI2B/$\overline{SYNCB}$	External crystal connection for channel B or synchronization input for channel B
GND	System ground
V_{DD}	+5 V (typical)

Pin Functions

CPU Interface

B/$\overline{A}$ [Channel Select]. The input to this pin selects the channel to be accessed for a write or read operation. A low input selects channel A; a high input selects channel B.

C/$\overline{D}$ [Control/Data Select]. The input to this pin selects the type of data on the data bus during a write or read access. A low input selects data; a high input selects a control or status register.

CLK [System Clock]. This input supplies the clock for the internal operation of the device. It is separate from the data clocks. The system clock input must be more than five times the serial data transfer rate.

$\overline{INT}$ [Interrupt]. The interrupt request output signal at this pin goes low if an interrupt cause occurs within the AMPSC. The output is an open-drain transistor and requires a pull-up resistor.

$\overline{INTAK}$ [Interrupt Acknowledge]. An active-low input signal at this pin is used in response to an interrupt request. In the Vector mode (CR2A bit D7 = 1), it causes the interrupt vector to be placed on the data bus. The output vector mode determines the number of cycles of $\overline{INTAK}$ toggling that are required for each interrupt acknowledge cycle (see CR2A bits D3-D5). In the Nonvector mode (D7 = 0), this pin must be pulled high. If unused, this pin must also be pulled high.

$\overline{PRI}$ [Priority Input]. The $\overline{PRI}$ signal controls interrupt request generation and interrupt vector output. The pin is the input for the interrupt priority daisy chain that determines how interrupts from multiple devices are resolved. A high level prevents the AMPSC from presenting an interrupt vector during the INTAK sequence. A low level allows the vector to be presented. If unused, this pin must be tied low.

$\overline{PRO}$ [Priority Output]. This is an output to the interrupt priority daisy chain. It controls interrupt requests from lower-priority devices. It indicates the existence of a higher-priority interrupt, either within the AMPSC or, if no internal interrupt exists, the condition of the $\overline{PRI}$ input.

$\overline{RESET}$ [Reset]. Applying a low signal continuously for two or more clock cycles (t_{CYK}) to this pin resets the AMPSC (system reset) and places it in Standby mode. A system reset disables the transmitter, receiver, interrupt, and DMA functions and sets the TxD and general-purpose output pins to high. It also resets all bits of the control registers.

$\overline{RD}$ [Read]. The active-low $\overline{RD}$ input signal causes status or receive (Rx) data to be read out of the AMPSC. The data is presented on pins D_0-D_7. The values are dependent on the state of the B/$\overline{A}$ and C/$\overline{D}$ inputs and the internal state of the device.

$\overline{WR}$ [Write]. The active-low $\overline{WR}$ input signal causes control words or transmit (Tx) data to be written into the AMPSC. The data written is input on pins D0-D7 (data bus). The destination of the data is determined by the state of the B/$\overline{A}$ and C/$\overline{D}$ pins and the value of the internal register pointer.

D_7-D_0 [Data Bus]. These pins constitute a three-state, 8-bit, bidirectional data bus. The bus is connected to the host processor's data bus to transfer control words, status information, and send/receive data.

Channel Interface

RxDA, RxDB [Receive Data]. Receive data enters the AMPSC on these pins.

TxDA, TxDB [Transmit Data]. Transmit data exits the AMPSC on these pins.

DRQTxA, DRQTxB [DMA Transmit Requests]. These active-high outputs for channels A and B are DMA requests to the DMA controller. The pin is set to high when the Tx buffer is emptied. The conditions under which this occurs depend on the status of control register CR1 bit D2. (DRQTxB and $\overline{DTRA}$ are dual functions of the same pin.)

DRQRxA, DRQRxB [DMA Receive Requests]. These active-high outputs for channels A and B are DMA requests to the DMA controller. The pin is set to high when the receiver enters the Rx Character Available state. It is reset when received data is read out of the channel. (DRQRxB and $\overline{DTRB}$ are dual functions of the same pin.)

$\overline{TRxCA}$, $\overline{TRxCB}$ [Transmit/Receive Clock]. If bit D2 of control register CR15 is zero, these pins are transmit or receive clock inputs. Also, they are inputs if bits D5 and D6 or D3 and D4 are set to one and zero, respectively, overriding the state of bit D2.

If none of the conditions above are true, the pins function as outputs with the source selectable between the crystal oscillator, the BRG, the DPLL, and the transmit clock. Selection is made with bits D0 and D1 of CR15.

$\overline{STRxCA}$, $\overline{STRxCB}$ [Clock Source]. These pins are the transmit or receive clock source inputs for channels A and B, respectively. They can be routed internally to the transmitter, receiver, BRG's, or DPLL. An alternative function as an external crystal connection point (XI) is selected by control register CR15 bit D7.

XI1A, XI2A and XI1B, XI2B [Crystal Connections]. These two pin pairs may be connected to external crystals that control the internal oscillators for channels A and B, respectively. (See $\overline{\text{STRxCA}}$ and $\overline{\text{STRxCB}}$.)

Modem Control

RTSA, RTSB [Request to Send]. These are general-purpose outputs usable, as an example, for modem control. Pin status is set by CR5 bit 01 and Auto Enable bit status (CR3 bit D5).

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ [Clear to Send]. These are general-purpose inputs usable, as an example, for modem control. A status change on $\overline{\text{CTSA}}$ or $\overline{\text{CTSB}}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{\text{CTSA}}$ and $\overline{\text{CTSB}}$ can be used with the Tx Enable bit (CR5 bit D3) to control transmitter operation.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$ [Data Carrier Detect]. These are general-purpose inputs usable, as an example, for modem control. A status change on $\overline{\text{DCDA}}$ or $\overline{\text{DCDB}}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{\text{DCDA}}$ and $\overline{\text{DCDB}}$ can be used with the Rx Enable bit (CR3 bit D0) to control receiver operation.

$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$ [Data Terminal Ready]. These are general-purpose active-low outputs controlled by control register CR5A bit D7. (DRQTxB and DRQRxB have dual pin functions with $\overline{\text{DTRA}}$ and $\overline{\text{DTRB}}$.)

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$ [Sync Input or Output]. In accordance with the settings of control regsister CR4 bits D7-D2, and with CR15 bit D7 = 0, the three functions of these pins are as follows.

(1) Asynchronous mode: general-purpose input that functions like $\overline{\text{DCD}}$ and $\overline{\text{CTS}}$.

(2) External sync mode: active-low input indicates to the AMPSC that synchronization has occurred.

(3) Internal sync mode: active-low output indicates when synchronization is detected by the AMPSC.

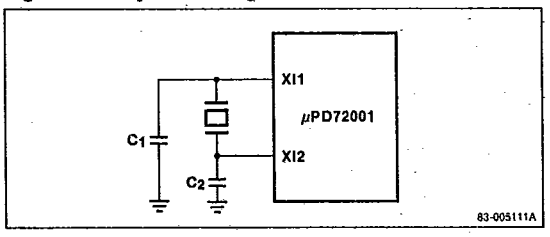
Crystal Recommendations

The crystals used with the μPD72001 internal crystal oscillators should be parallel resonant, fundamental mode, with an AT cut. For frequency stability, two capacitors can be added from the pins of the crystal to ground (figure 1). The value of the capacitors can be calculated by the following formula:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_S$$

C_L is the load capacitance of the crystal and C_S is all stray capacitance in parallel with the crystal. The C_S value should include the input capacitance (C_{IO} and C_{IN}) of the μPD72001 and any wiring or socket capacitance.

Figure 1. Crystal Configuration Circuit



Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	−0.5		+0.8	V	All pins except CLK
	V_{ILC}	−0.5		+0.6	V	CLK pin
Input high voltage	V_{IH}	+2.2		V_{DD} + 0.5	V	All pins except CLK
	V_{IHC}	+3.3		V_{DD} + 0.5	V	CLK pin
Output low voltage	V_{OL}			+0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OUT} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OUT} = 0 V
Input leakage current, high	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IN} = 0 V
V_{DD} supply current	I_{DD}		20	40	mA	All outputs at high level; t_{CY} = 0.125 μs
Standby current	I_{DDI}		1	20	μA	f_{RxC} = f_{TxC} = f_{CLK} = DC
			1	2	mA	Standby mode

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Input capacitance	C_{IN}		10	pF	f_C = 1 MHz; unmeasured pins returned to 0 V.
I/O capacitance	C_{IO}		20	pF	

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Limits, 8 MHz Min	Max	Limits, 11 MHz Min	Max	Unit	Test Conditions
Clock							
Clock cycle (Note 1)	t_{CYK}	125	2000	91	2000	ns	
Clock high level width	t_{WKH}	50	1000	40	1000	ns	
Clock low-level width	t_{WKL}	50	1000	40	1000	ns	
Clock rise time	t_{KR}		10		10	ns	1.5 to 3.0 V
Clock fall time	t_{KF}		10		10	ns	3.0 to 1.5 V

Notes:

(1) In all modes, the system clock frequency must be more than five times the maximum data rate.

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AC Characteristics (cont)

Parameter	Symbol	Limits, 8 MHz Min	Limits, 8 MHz Max	Limits, 11 MHz Min	Limits, 11 MHz Max	Unit	Test Conditions
Read Cycle							
Address setup time to $\overline{RD}\downarrow$	t_{SAR}	0		0		ns	
Address hold time from $\overline{RD}\uparrow$	t_{HRA}	0		0		ns	
$\overline{RD}$ pulse width	t_{WRL}	150		150		ns	
Data output delay time from address	t_{DAD}		120		120	ns	
Data output delay time from $\overline{RD}\downarrow$	t_{DRD}		120		120	ns	
Data float delay time from $\overline{RD}\uparrow$	t_{FRD}	10	85	10	85	ns	
Write Cycle							
Address setup time to $\overline{WR}\downarrow$	t_{SAW}	0		0		ns	
Address hold time from $\overline{WR}\uparrow$	t_{HWA}	0		0		ns	
$\overline{WR}$ pulse width	t_{WWL}	150		150		ns	
Data setup time to $\overline{WR}\uparrow$	t_{SDW}	120		120		ns	
Data hold time from $\overline{WR}\uparrow$	t_{HWD}	0		0		ns	
Read/Write Cycle							
$\overline{RD}/\overline{WR}$ recovery time (Note 2)	t_{RV}	160		160		ns	
Transmit or Receive Cycle							
Transmit/receive data cycle	t_{CYD}	5		5		t_{CYK}	
$\overline{STRxC}$, $\overline{TRxC}$ input clock cycle	t_{CYC}	125		91		ns	
$\overline{STRxC}$, $\overline{TRxC}$ input clock pulse							
High-level width	t_{WCH}	50		40		ns	
Low-level width	t_{WCL}	50		40		ns	
Transmit Cycle							
TxD delay time from $\overline{STRxC}\downarrow$, $\overline{TRxC}\downarrow$	t_{DTCTD1}		100		100	ns	x1 mode
	t_{DTCTD2}		300		300	ns	x16, x32, x64 mode
$\overline{INT}$ delay time from TxD	t_{DTDIQ}	4	6	4	6	t_{CYK}	Tx INT mode
DRQTx delay time from TxD	t_{DTDDQ}	4	6	4	6	t_{CYK}	Tx DMA mode

Notes (cont):

(2) For all operations except Tx/Rx data transfer

AC Characteristics (cont)

Parameter	Symbol	Limits, 8 MHz Min	Limits, 8 MHz Max	Limits, 11 MHz Min	Limits, 11 MHz Max	Unit	Test Conditions
Receive Cycle							
RxD setup time to $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{SRDRC}	0		0		ns	
RxD hold time from $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{HRCRD}	140		140		ns	
INT delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCIQ}	7	11	7	11	t_{CYK}	Rx IN mode
DRQRx delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCDQ}	7	11	7	11	t_{CYK}	Rx DMA mode
DMA Request Control							
DRQRx ↓ request delay time from $\overline{RD}$ ↓	t_{DRDQ}		120		120	ns	
DRQTx ↓ request delay time from $\overline{WR}$ ↓	t_{DWDQ}		120		120	ns	
Interrupt Control							
$\overline{INTAK}$ low-level width	t_{WIAL}	150		150		ns	
$\overline{PRO}$ delay time from $\overline{PRI}$	t_{DPIPO}		50		50	ns	
$\overline{PRI}$ setup time to $\overline{INTAK}$ ↓	t_{SPIIA}	0		0		ns	When vector output is selected.
PRI hold time from $\overline{INTAK}$ ↑	t_{HIAPI}	20		20		ns	
Data output delay time from $\overline{INTAK}$ ↓	t_{DIAD}		120		120	ns	
Data float delay time from $\overline{INTAK}$ ↑	t_{FIAD}	10	85	10	85	ns	
Modem Control							
$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse							
High-level width	t_{WMH}	2		2		t_{CYK}	
Low-level width	t_{WML}	2		2		t_{CYK}	
INT delay time from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	t_{DMIQ}		2		2	t_{CYK}	
Sync Control							
$\overline{SYNC}$ delay $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{DTRCSY}	0	2	0	2	t_{CYK}	COP external synchronization
Crystal Oscillator							
XI1 input cycle time	t_{CYX}	125	1000	91	1000	ns	
Reset							
$\overline{RESET}$ pulse width	t_{WRSL}	2		2		t_{CYK}	

Notes [cont]:

(3) $\overline{STRxC}$ or $\overline{TRxC}$, whichever is used for the receive clock

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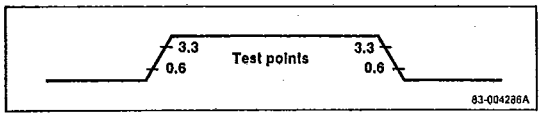
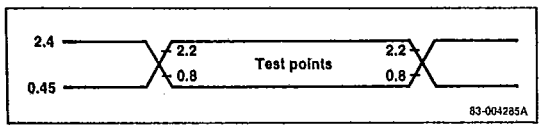
Timing Waveforms

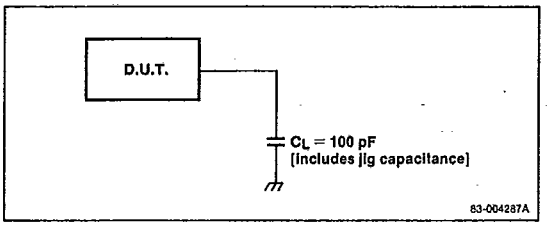
Clock Input Test Points



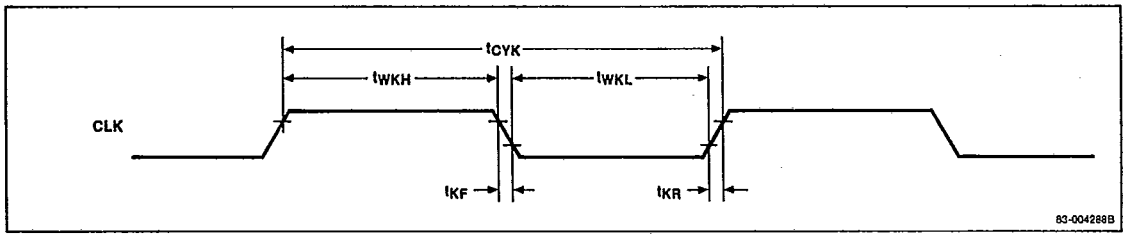
I/O Waveform Test Points



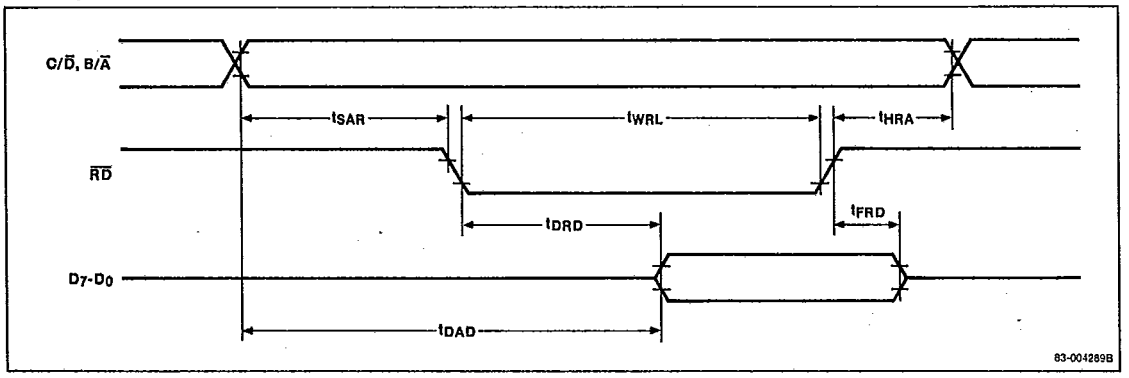
AC Test Load Circuit



Clock Timing

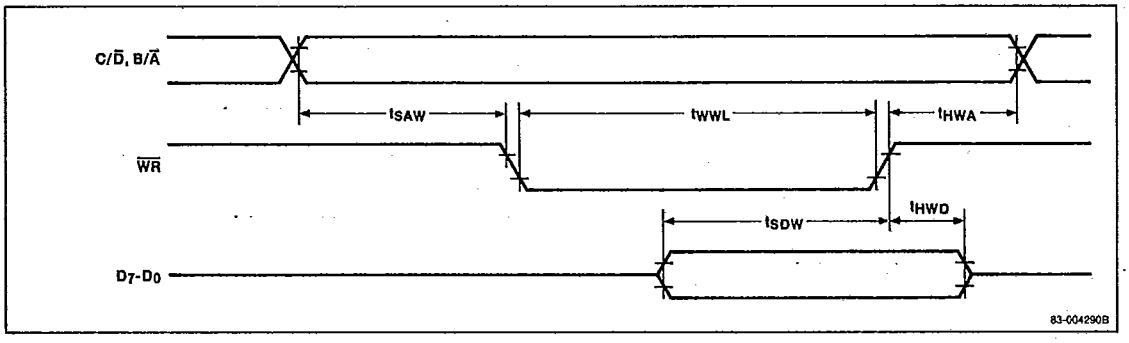


Read Cycle

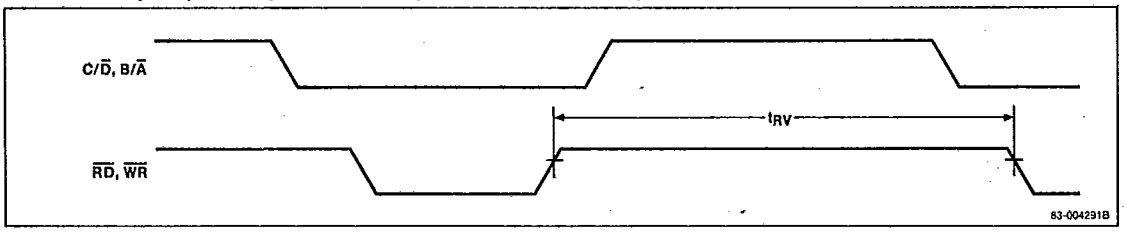


Timing Waveforms (cont)

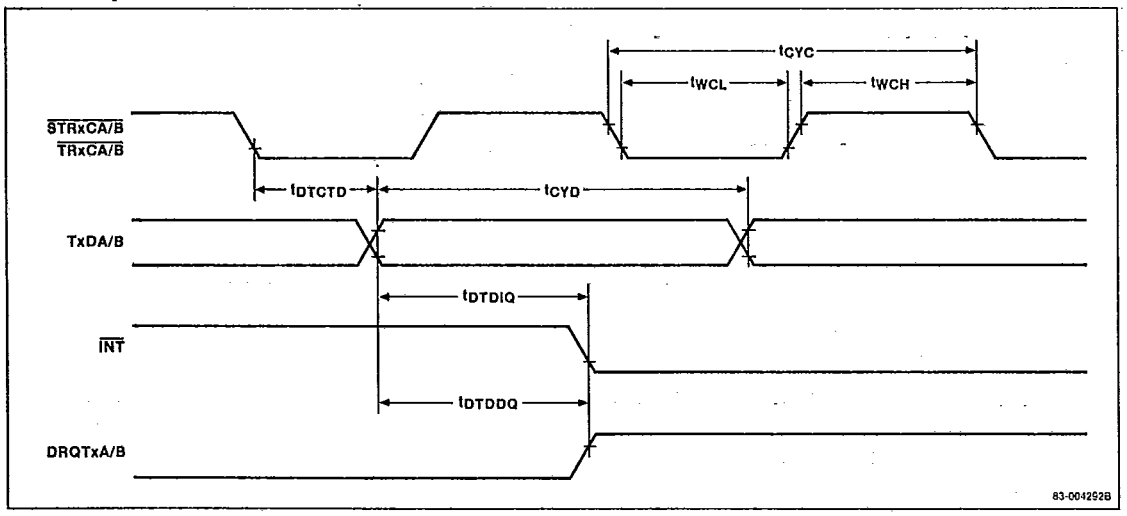
Write Cycle



Read/Write Cycle (for all operations except Tx/Rx data transfer)

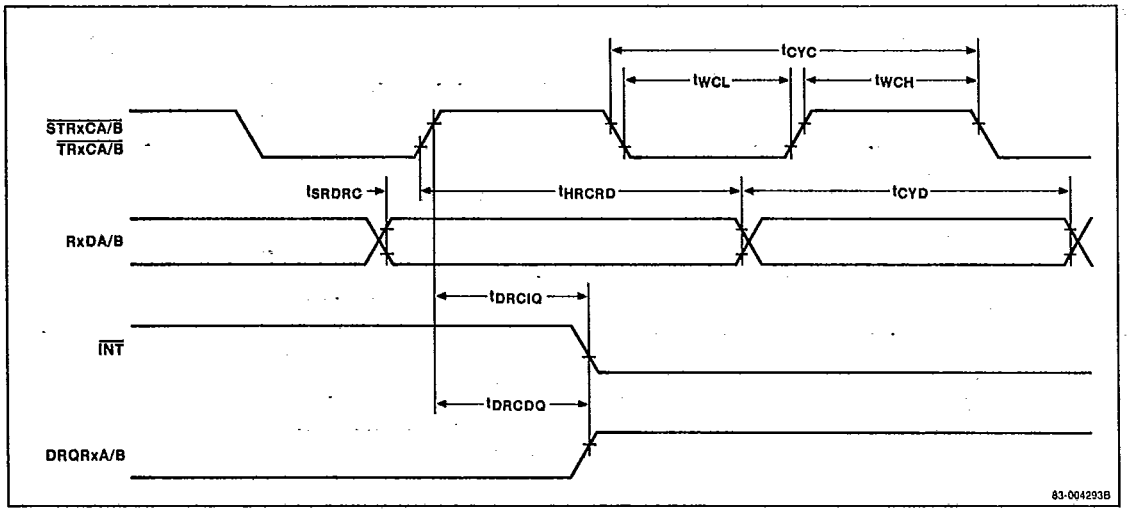


Transmit Cycle

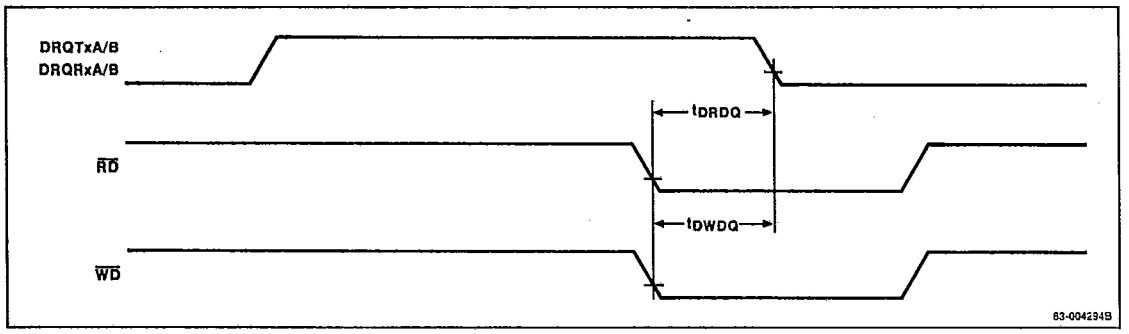


Timing Waveforms (cont)

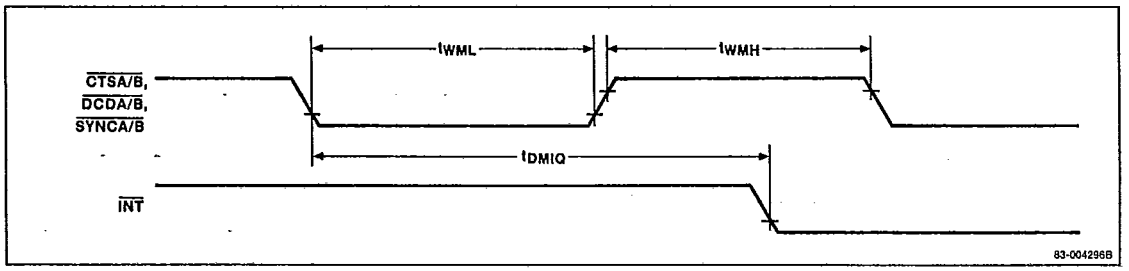
Receive Cycle



DMA Request Control

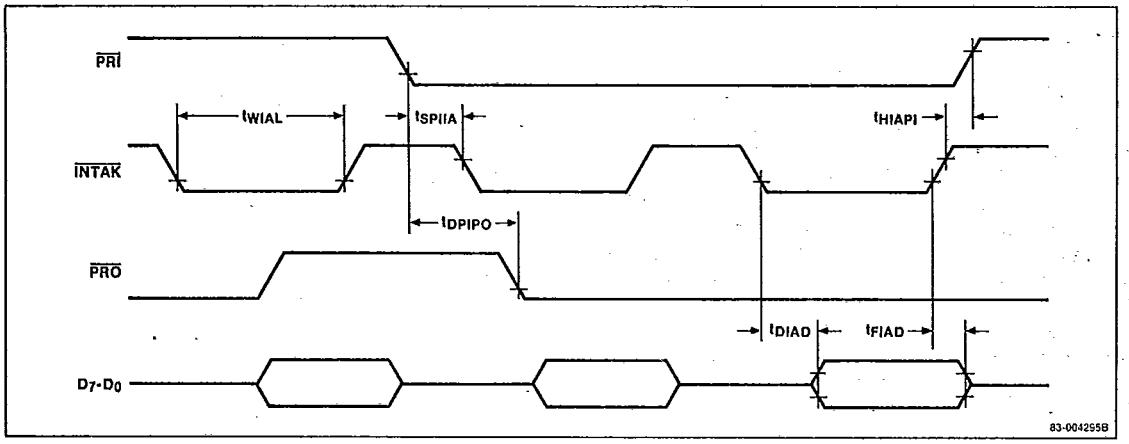


Modem Control

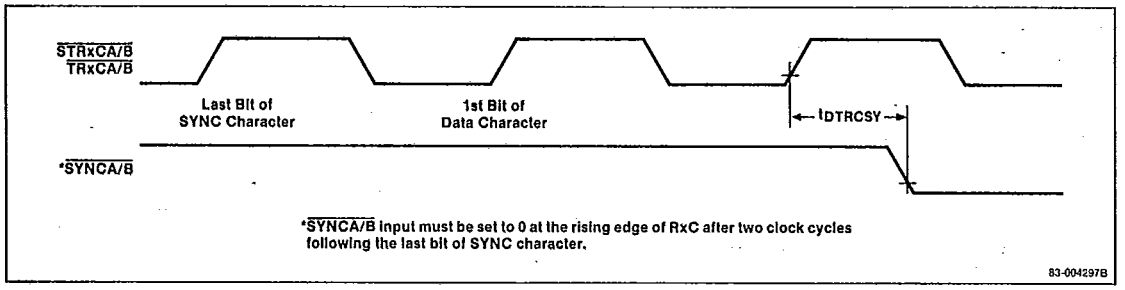


Timing Waveforms (cont)

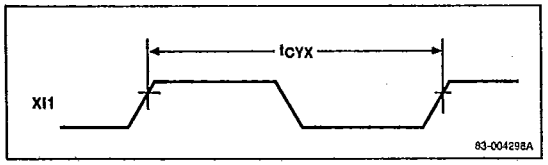
Interrupt Control



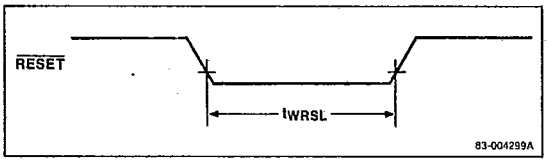
Sync Control



Crystal Oscillator



Reset



Functional Operation

Refer to the μPD72001 AMPSC block diagram (figure 2) for an overview of the four major functional blocks of logic listed below.

- System clock control
- Interface control
- Transmitter
- Receiver

System Clock Control

The system clock control logic receives and manages the system clock (CLK), which operates the internal circuitry of the μPD72001. The system clock and internal circuitry must be operating in order for the transmitters and receivers of the μPD72001 to function. In standby mode, the system clock is blocked by the clock control circuitry and the transmitters and receivers can not operate. In clocked operation, the system clock can be used as the source for the data clock, which is used by the transmitters and receivers.

The internal registers of the μPD72001 are static in nature and do not require the system clock to retain their contents.

Interface Control

The interface control logic contains the signals used to control the transfer of data and status information between the host CPU and the AMPSC. This logic block has four types of interface lines. The read/write and control lines ($\overline{RD}$, $\overline{WR}$, C/$\overline{D}$, B/$\overline{A}$) select what data is to be transferred and the direction of the transfer. The reset line ($\overline{RESET}$) which is part of this group, resets the internal state of the μPD72001 when held active. The interrupt control line ($\overline{INT}$) sends a signal to the host CPU when the AMPSC requires attention. The interrupt acknowledge line ($\overline{INTAK}$) signals the μPD72001 when the host CPU is ready to service its request for attention. The interrupt priority lines ($\overline{PRI}$, $\overline{PRO}$) are used to form the interrupt priority daisy chain, which arbitrates the interrupt service priority.

The DMA control lines (DRQRxA, DRQTxA, DRQRxB, DRQTxB), inform the DMA controller when a data transfer is ready. The data bus buffer provides temporary storage of the data (D7-D0) being transferred from the internal registers of the μPD72001 to the host CPU.

Transmitter

Each channel's transmitter accepts parallel byte data and sends it out serially. The data is sent out at a rate determined by the transmit data clock (TxCLK). The source of this clock is determined by the clock control multiplexer. Bytes are loaded into the transmit buffer. When the transmit shift register is empty, the contents of the transmit buffer are loaded into the transmit shift register.

The transmitter is also responsible for the transmit CRC calculation and sending flags and sync characters. The transmitter can be made to send breaks and aborts using commands from the host CPU.

The internal loopback feature connects the transmitter to the receiver and disconnects the receiver from the RxD pin.

The echo loop feature connects the receiver to the TxD pin and disconnects the transmitter.

The Baud Rate Generators (BRGs) divide down the selected clock source to produce data clocks that can be used for the transmitter and receiver. The clock multiplexer selects the clock sources for them. By selecting the correct value for the BRG count, the BRG can be used as a timer with a wide dynamic range. The clock source for the timer can be selected from the system clock, the data clock, an external source, or a crystal.

Receiver

The receivers in the AMPSC accept serial data into the receive shift register, which in turn assembles this serial data into parallel characters (byte). The assembled byte is transferred into the receive buffer (FIFO), which can contain up to three bytes. The receive status of each byte is transferred along with it through the receive buffer. In this way, the status reported by the μPD72001 is always current for the byte that is about to be removed from the FIFO.

The receive shift register also checks for flags and sync characters in the synchronous modes. Flags are automatically removed from the data stream, while sync characters have the option of being retained. This is determined by a CPU command.

The receiver in synchronous modes, calculates the received CRC and checks it against the CRC that is received with the data. A difference is reported to the host processor.

The digital phase-locked loop (DPLL) is used to separate the data from the clocking information in the NRZI, FM, and Manchester encoded received bit streams. It locks in on the received data and provides an accurate and stable clock for the receiver.

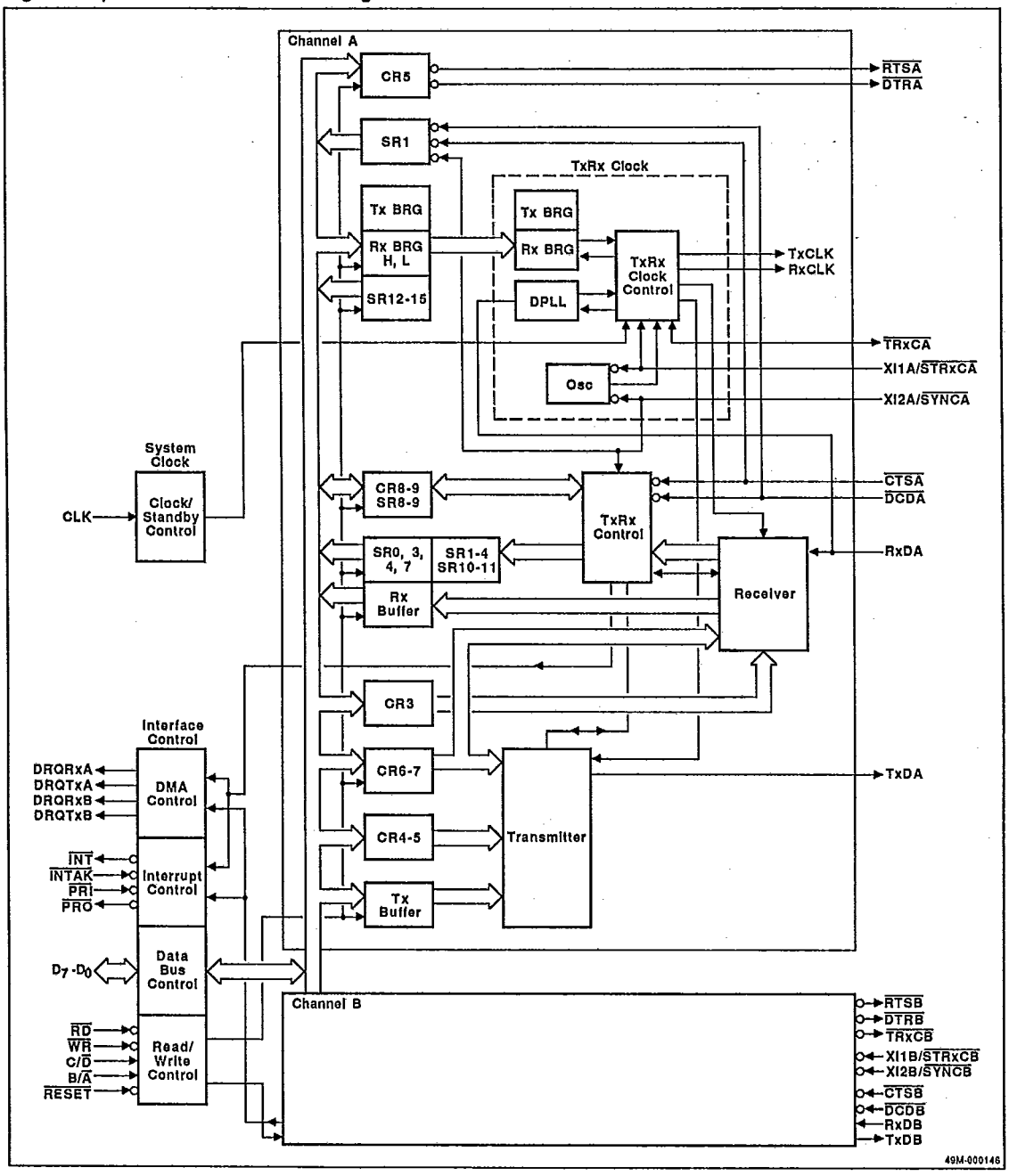
Standby Mode

The μPD72001 enters the standby mode after a hardware reset or by issuing the standby command (CR13 bit D0). In standby mode, the system and data clocks are blocked internally by the clock multiplexer. This shuts down the AMPSC and reduces power consumption greatly. System power requirements can be further reduced by externally stopping the input clock transitions.

In standby mode, the μPD72001 retains all register values, but no internal functions operate and read operations of the AMPSC will not transfer any data.

To release the standby mode, a write cycle must be performed to CR0. To resume normal operation without affecting the internal state of the device, a zero can be written to CR0.

Figure 2. μPD72001 AMPSC Block Diagram



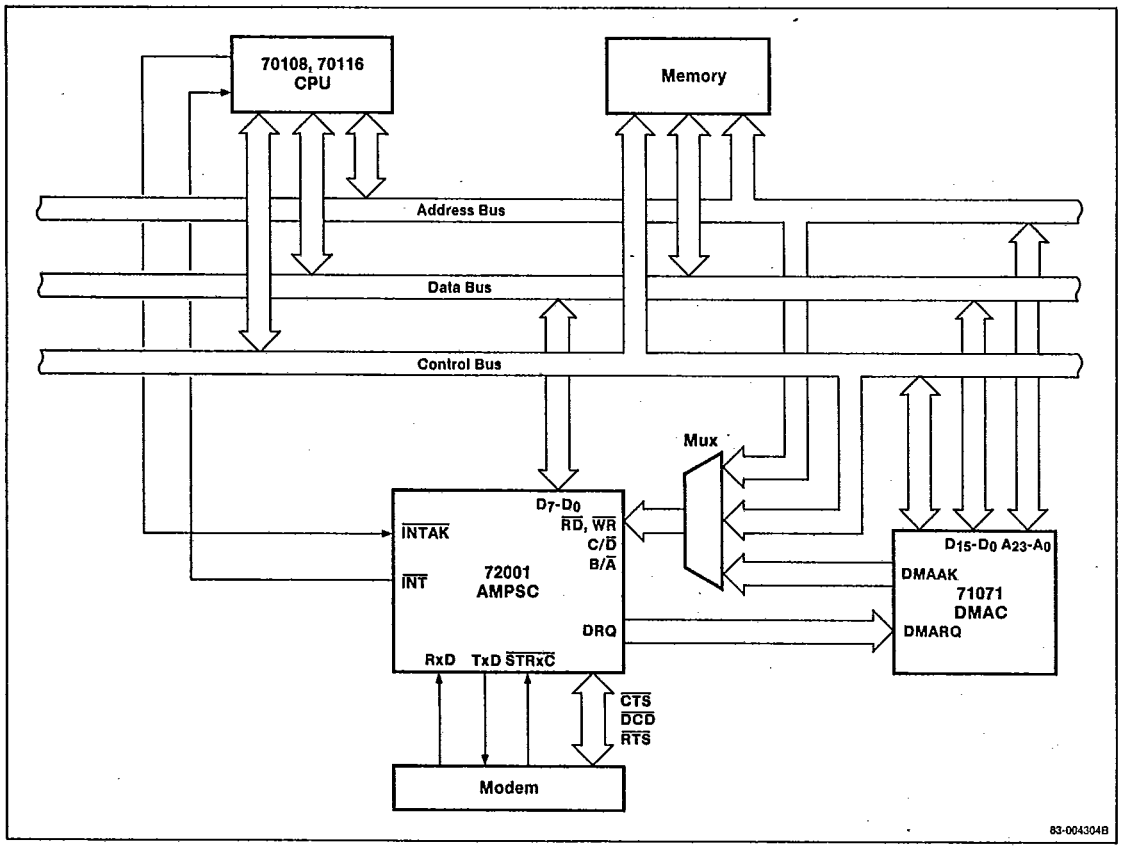
System Configuration Example

In the system configuration example (figure 3), the μPD72001 is used as a high-speed interface to a modem. It controls the modem interface and serial data flow. The AMPSC is used with a direct memory access controller (DMAC), such as the μPD71071 in order to speed the data transfer and reduce the host CPU overhead.The μPD72001 directly interfaces with the host CPU, without requiring an interrupt controller, such as the μPD71059. Extra hardware is not required, since the AMPSC can generate its own interrupt vectors.

The interface between the μPD72001 and the host CPU is not very complex. It requires only address decoding logic for I/O operations. A multiplexer can be used to decode DMA acknowledge signals. However, it is not necessary with DMA controllers, such as the μPD71071, which are able to do their own I/O addressing.

The AMPSC's flexible interface to a variety of host processors makes connection simple.

Figure 3. System Configuration Example



Programming the AMPSC

Software programming the AMPSC utilizes separate data and command/status paths. The data path uses an 8-bit register. The command/status path has a set of 8-bit registers structured for efficient and complete control with a minimum of interaction from the host processor.

The internal registers (table 1) are divided into control registers (CRs) and status registers (SRs). Also, unless otherwise noted in table 1, each channel has its own set of registers; for example, CR1A and CR1B are the CR1 control registers for channels A and B.

The control and status registers for a given channel are all accessed through the same I/O address. The different registers are selected by using the register pointer in CR0 (bits D0-D2). The register pointer is reset to zero after each register operation. For example, to write to CR2, a two is initially written to the control address (C/$\overline{D}$ pin set high). After this the value to be written into CR2 is also written to the control address. To read from SR2, a two is written to the control address, and then a read cycle at the control address reads the value in SR2. A zero is not required to be written before CR0 and SR0 are accessed.Control registers (figure 4) set up the device operation mode or control device operations. The host processor writes control words into these registers.

Status registers (figure 5) hold device status information. The host processor can sense the AMPSC device status by reading these registers.

Frequently used information is retained in control register CR0 and status register SR0. This information can be sent or received by writing or reading a single byte. In normal operation, CR0 is initially loaded with a command to reset the AMPSC. Next, CR2 is loaded to set the interface mode. This is followed by the remaining registers, beginning with CR4 to set the protocol type.

Table 1. AMPSC Internal Register Configuration

Control Registers	CR0	
	CR1	
	CR2	Functions differ for CR2A and CR2B
	CR3	
	CR4	
	CR5	
	CR6	
	CR7	
	CR8, CR9	Registers for each channel are used in pairs: CR8A/CR9A; CR8B/CR9B
	CR10	
	CR11	
	CR12	Tx/Rx BRG registers are loaded by setting bits 0 and 1 of CR12
	CR13	
	CR14	
	CR15	
Status Registers	SR0	
	SR1	
	SR2B	No register SR2A
	SR3	
	SR4A	No register SR4B
	SR5, SR6, SR7	No registers
	SR8	
	SR9	
	SR10	
	SR11	
	SR12, SR13	Registers for each channel are used in pairs: SR12A/SR13A; SR12B/SR13B
	SR14, SR15	Registers for each channel are used in pairs: SR14A/SR15A; SR14B/SR15B

Figure 4. Control Register Bit Functions

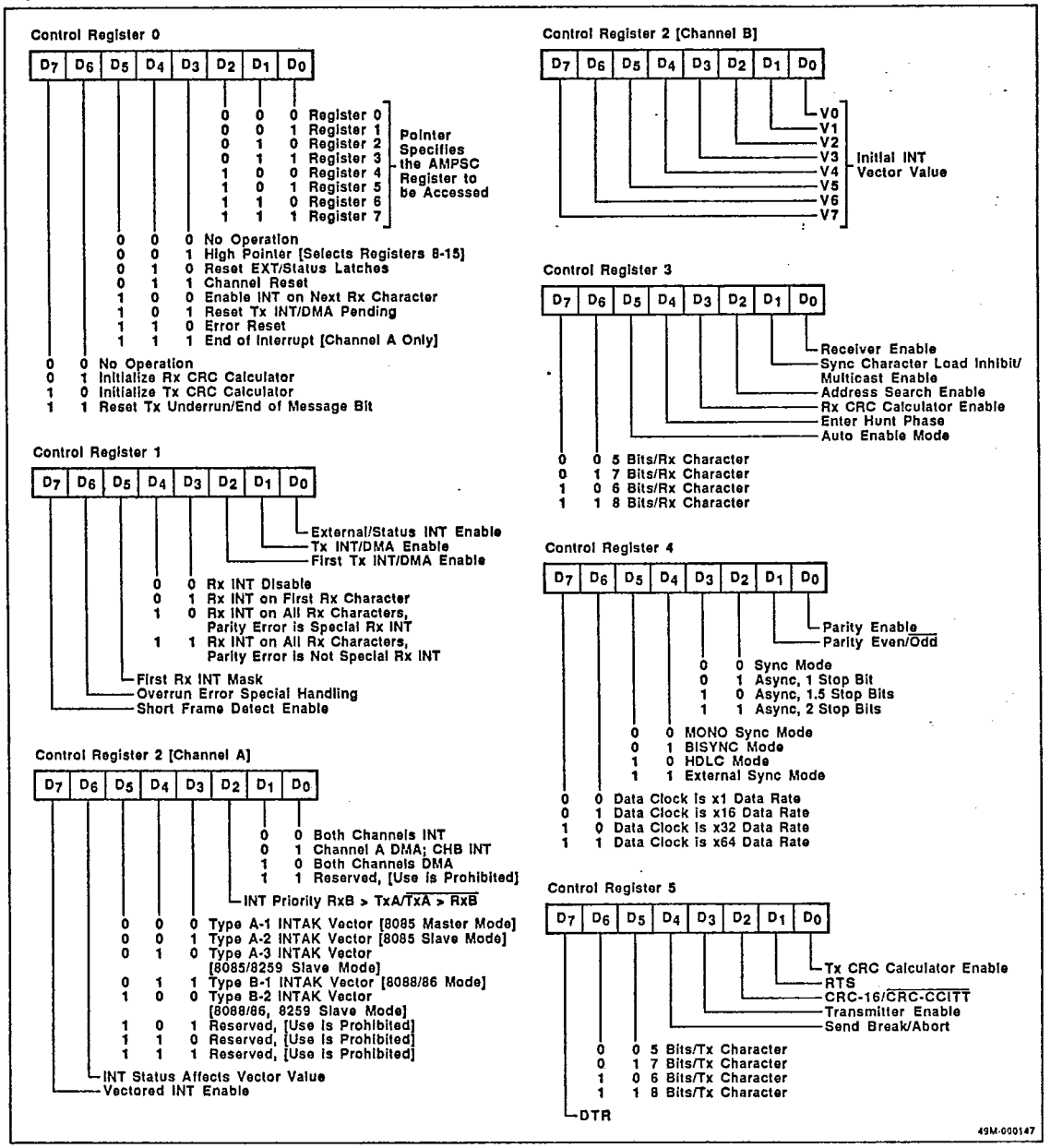


Figure 4. Control Register Bit Functions (cont)

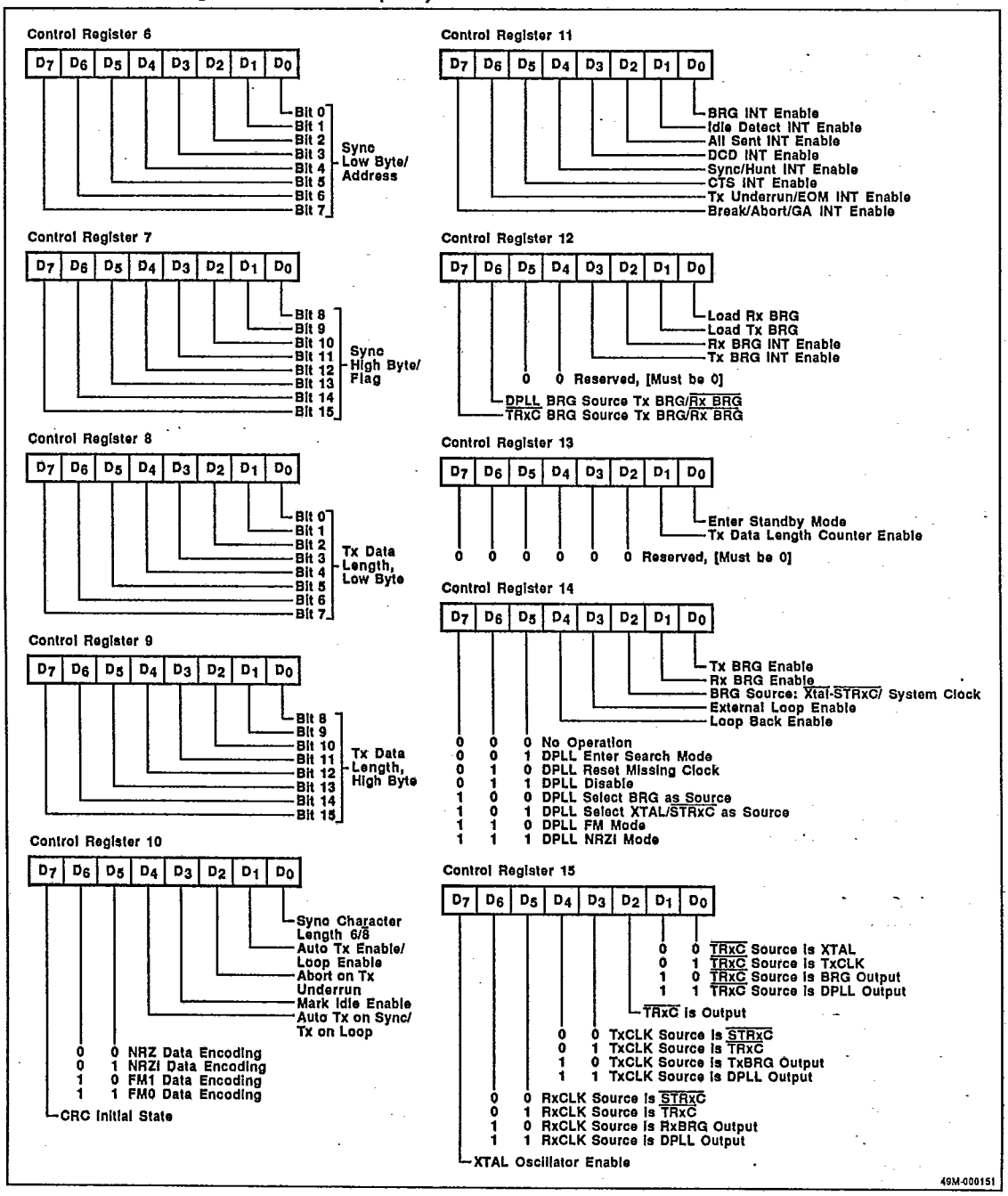


Figure 5. Status Register Bit Functions

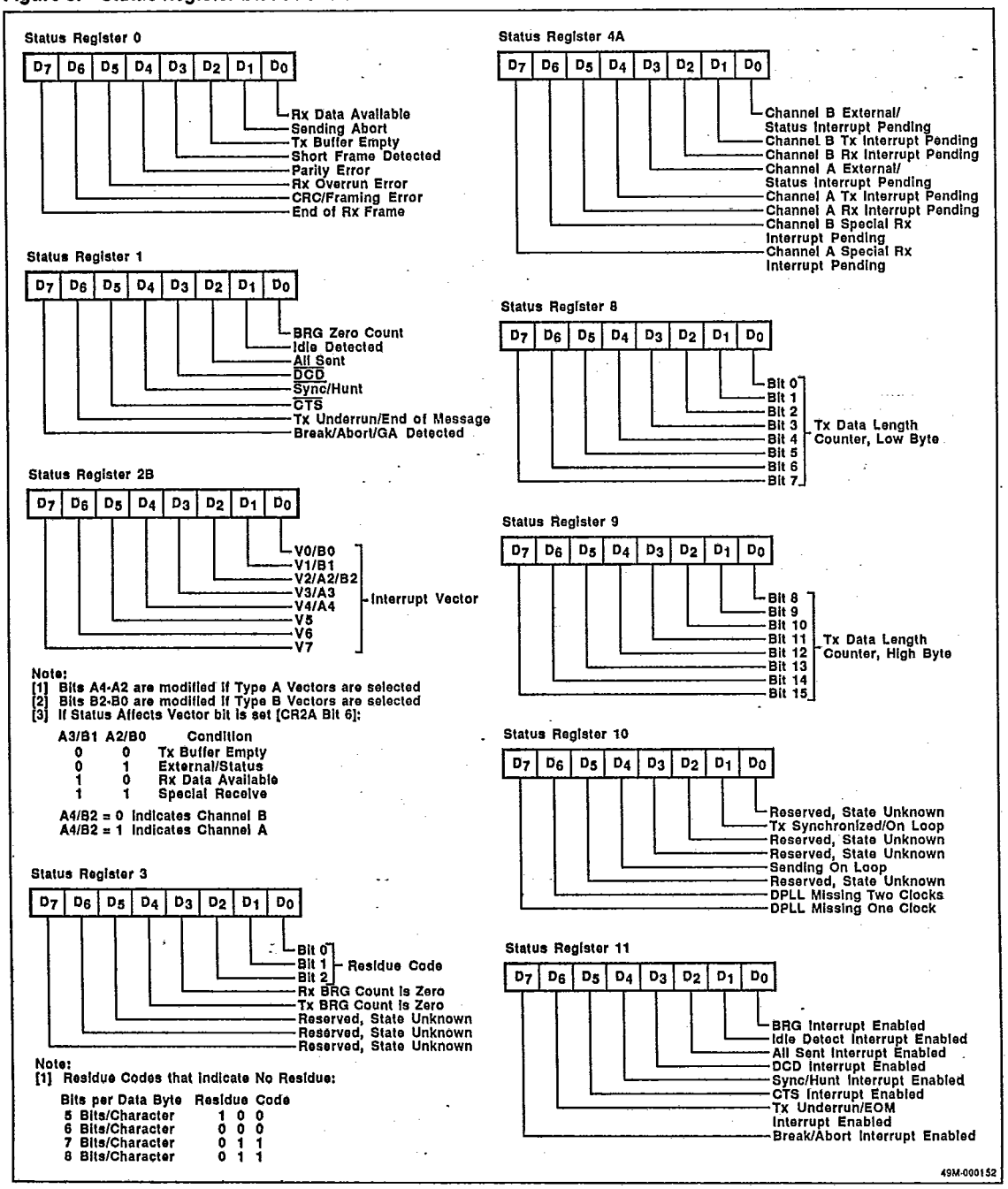
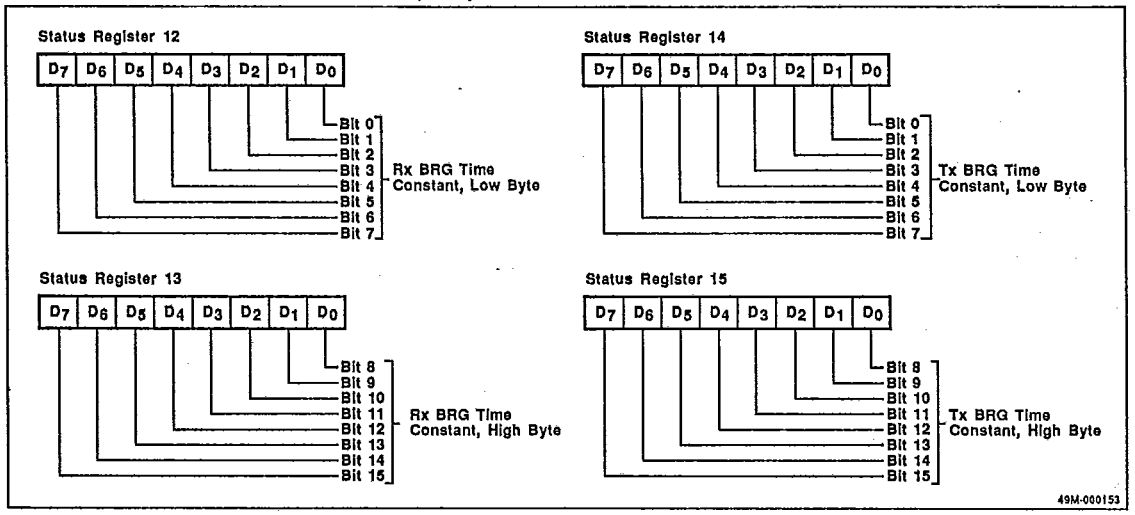


Figure 5. Status Register Bit Functions (cont)



Control Register CR0

CRC Control [D7-D6]

These bits are valid when the COP or BOP mode is selected. They are not used in the asynchronous mode.

No Operation [00]. This command has no effect.

Initialize Rx CRC Calculator [01]. This command initializes the receiver (Rx) CRC calculator. The command should be issued before data reception starts. However, before this command is issued, the initial value of the Rx CRC calculator must be set by the value of CR10 bit D7.

This command is not required in the BOP mode, since the CRC calculator is automatically initialized upon receipt of the flag value according to the value of CR10 bit D7.

Initialize Tx CRC Calculator [10]. This command initializes the transmit (TX) CRC calculator. It should be issued before data transmission is started. However, before the command is issued, the initial value of the Tx CRC calculator must be set by the value of CR10 bit D7.

In the BOP mode, if CR10 bit D7 is set to one, the Tx CRC calculator is automatically initialized to one, when a flag value is loaded into the transmit shift register within the AMPSC.

Reset Tx Underrun/EOM Bit [11]. This command resets SR1 bit D6 from one to zero (transmit underrun/end-of-message bit). If data is not loaded into the transmit buffer before the transmit shift register begins transmitting its last bit, the AMPSC enters the Tx Underrun/EOM state. At this point, the AMPSC checks to see if a CRC SYNC/Flag or abort is to be sent, which depends on the value of SR1 bit D6 and the operating mode. Therefore, SR1 bit D6 must be reset before transmission of the last byte starts. At the occurrence of Tx underrun, the CRC or the SYNC character/flag is sent when the SR1 bit D6 is a zero or one, respectively.SR1 bit D6 is set when the CRC or SYNC/Flag byte is written to the Tx register by the AMPSC.

In the BOP mode, bit D6 of SR1 is automatically set to zero when the first data byte of a frame is written into the AMPSC.

Command [D5-D3]

These bits control the state of the device.

No Operation [000]. This command has no effect.

High Pointer [001]. This command is used in conjunction with CR0 bits D2-D0 (Register Pointer) to access status registers 8 through 15. For example, to access SR11, bits D5-D0 of CR0 are set to 001011.

Reset E/S Bit Latches [010]. This Reset External/Status Bit Latch command is issued when an E/S bit (each bit of SR1) latch operation has occurred. It opens the E/S latches and prepares for the latching of a new E/S bit status change. If E/S interrupt is enabled, an E/S interrupt will occur and the latches will latch when an E/S bit's status changes. Not all state transitions will cause latching and an interrupt to occur. See the description of SR1 for details. New status will not be available in SR1 until this command is issued.

Channel Reset [011]. This command resets an AMPSC channel. It performs a function similar to the $\overline{\text{RESET}}$ pin. Executing the channel reset command halts channel operation. After a channel reset, three system clock periods (t_{CY}) should elapse before any further commands or data are sent to the channel.

Enable Next Rx Character Interrupt [100]. This command is valid only when the First Rx INT mode (CR1 bits D4-D3 = 01) is selected. It is issued at the end of a message to request an additional Rx interrupt for the first received byte of the next message. The additional Rx interrupt occurs when the next data byte is received after the command is issued.

This command has no effect when the First Rx INT mask is on (CR1 bit D5 = 1), even if the First Rx INT mode is selected.

Reset Tx Interrupt/DMA Pending [101]. This command is used to clear a pending Tx interrupt request or Tx DMA request while the Tx buffer is empty (SR0 bit D2 = 1). It is typically used to clear a Tx interrupt or Tx DMA request caused by the Tx buffer empty state that occurs after the last byte is written into the AMPSC.

Error Reset [110]. This command is used to reset the pertinent bits (SR0 bits D7-D3) if a Special Rx Condition has occurred. If it occurs when the First Rx INT mode is selected, any data that is subsequently received is not transferred to the last stage of the AMPSC internal Rx buffer, but will remain in the first and second stages until this command is issued.

End of Interrupt [111]. This command is used so that the AMPSC can recognize the end of interrupt service processing. It should be issued when interrupt service for the AMPSC is completed. Command execution resets the internal interrupt service latch and re-enables lower priority interrupt requests. This command is required when the start of interrupt service has been indicated by either conducting an $\overline{\text{INTAK}}$ cycle, or by reading SR2B.

Register Pointer [D2-D0]

These bits specify which AMPSC register number is to be accessed. The bits are reset to 000 when system reset is executed or when the AMPSC is accessed after a Register Pointer value is specified. For registers numbered 8 and above, the High Pointer command (D5-D3 = 001) is used inconjunction with the Register Pointer to access them.

Control Register CR1

Short Frame Detect [D7]

Valid only in BOP mode, this bit detects short HDLC frames (frames that are less than 32 bits long).

Short Frame Detect Disabled [0]. Short frame detection is disabled.

Short Frame Detect Enabled [1]. Short frame detection is enabled. If a short frame is received, SR0 bit D3 (Short Frame Detect) is set to 1, causing a Special Rx condition interrupt.

Overrun Error INT [D6]

This bit selects the timing of overrun error detection.

Normal Mode [0]. In this mode, an overrrun error is indicated when the received data that caused the overrun error is transferred to the last stage of the receive buffer. A Special Rx Condition interrupt occurs at this time.

Special Mode [1]. In this mode, the Rx Overrun Error bit immediately reflects an overrun error within the AMPSC. A Special Rx Condition interrupt also occurs at this time. The received data that caused the overrun error may not be the byte at the last stage of the RxFIFO.

Receive Interrupt on First Character Mask [D5]

This bit is enabled only if the First Rx INT mode (CR1 bits D4-D3 = 01) is selected. It is used to mask Rx interrupts caused by received data. Setting this bit to 1 causes all first receive interrupts to be masked. It does not mask Special Receive interrupts. It is used in data transfers when no interrupt service is desired or required, such as DMA only data transfer.

Receive Interrupt Mode [D4-D3]

These bits set the Rx INT mode. They specify the way received data is managed.

Disable Mode [00]. This Receive Interrupt Disable mode is used to accept received data using status polling, or to disable the receive interrupt request.

First Rx Character Mode [01]. In this mode, which is typically used with DMA data transfer, an Rx interrupt occurs only when the first byte is received. This occurs when Rx is enabled after initialization or after the Enable Next Received Character interrupt command is issued.

All Receive-1 Mode [10]. This mode causes a receive interrupt to be generated for each byte received. In this mode, a parity error causes a Special Rx Condition interrupt.

All Receive-2 Mode [11]. This mode is the same as All Receive-1, except that parity error does not cause a Special Rx Condition interrupt.

First Transmit Interrupt/DMA Enable [D2]

This bit determines whether a Tx INT/DMA request is generated immediately after the transmitter is enabled. It is valid when INT/DMA is enabled (CR1 bit D1 = 1).

A transmit interrupt or DMA request is issued if bit D2 is 1 when the transmitter is enabled, but not if the bit is 0. Regardless of the state of bit D2, an interrupt or DMA request is generated when the Tx buffer makes the full-to-empty transition.

Transmit Interrupt/DMA Enable [D1]

This bit enables the transmit interrupt or DMA request. Each time a transmit interrupt condition exists and provided bit D1 is set, an interrupt or DMA request is generated.

External/Status Interrupt Enable [D0]

If bit D0 is set, a change in state of the external/status bits causes an interrupt and the state of the bits is latched. The latches must be reset with the Reset External/Status Bit Latch command (CR0 bits D5-D3), before subsequent interrupts can occur.

Control Register CR2A

Vectored Interrupt Enable [D7]

This bit enables transmission of the interrupt vector. If the bit is set, the interrupt vector is placed on the data bus during the INTAK cycle. If the bit is reset, the vector is never placed on the bus; It can be read by the host processor. In this mode, the $\overline{INT}$ signal is released after the host processor reads SR2B or clears the interrupt condition.

Interrupt Status Affects Vector [D6]

This bit determines if the value of an interrupt vector is modified by the cause of interrupt. If the bit is set, the vector is modified as specified by bits D5-D3. If the bit is reset, the vector is not modified and the cause of interrupt must be determined by reading SR0 and SR1.

Interrupt Vector Mode [D5-D3]

These bits determine the interrupt vector operation. The bits also select which bits of an interrupt vector are to be changed when the Status Affects Vector is set by CR2A bit D6. For details of how the vector is modified, refer to the description of register SR2B. Table 4 shows the vector operation determined by bits D5-D3.

Interrupt Priority Select [D2]

This bit selects the priority of interrupt requests within the AMPSC. The priority does not apply to DMA transfer.

If bit D2 = 0, the priority from high-to-low is RxA, TxA, RxB, TxB, E/S A, E/S B.

If bit D2 = 1, the priority from high-to-low is RxA, RxB, TxA, TxB, E/S A, E/S B.

Interrupt/DMA Mode [D1-D0]

These bits select the data transfer mode for each channel. The E/S, Rx, and Special Rx Condition interrupts can be enabled in both modes. The Tx interrupts are disabled on any channel in DMA mode. The three modes are as follows:

Bits D1-D0	Mode
00	Both channels interrupt
01	DMA on channel A, interrupt on channel B
10	DMA on both channels

Control Register CR2B

Bits D7-D0 of CR2B set the initial value of an interrupt vector.

Table 4. Interrupt Vector Operation Throughout INTAK Sequence

CR2A						Data Bus Status (INTAK response of AMPSC)							
D5	D4	D3	Mode	PRI	INTAK Cycle	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	A1	*	1st.	1	1	0	0	1	1	0	1
				low	2nd.	V7	V6	V5	M4	M3	M2	V1	V0
				low	3rd.	0	0	0	0	0	0	0	0
				*	1st.	1	1	0	0	1	1	0	1
				high	2nd.				High Impedance				
				high	3rd.				High Impedance				
0	0	1	A2	*	1st.				High Impedance				
0	1	0	A3	low	2nd.	V7	V6	V5	M4	M3	M2	V1	V0
				low	3rd.	0	0	0	0	0	0	0	0
				*	1st.				High Impedance				
				high	2nd.				High Impedance				
				high	3rd.				High Impedance				
0	1	1	B1	*	1st.				High Impedance				
1	0	0	B2	low	2nd.	V7	V6	V5	V4	V3	M2	M1	M0
				*	1st.				High Impedance				
				high	2nd.				High Impedance				

Notes:

(1) * = Don't care.

(2) When Status Affects Vector (bit 6 of CR2A) is set, the M data bits are modified to indicate the interrupt source.

(3) Modes A3 and B2 ignore the state of PRI. They are slave modes for use with an interrupt controller such as the μPD71059.

Control Register CR3

Receive Character Bit Length [D7-D6]

These bits determine the number of bits per character in the received data.

Bits D7-D6	Bits/Character
00	5
01	7
10	6
11	8

Auto Enable Mode [D5]

Bit D5 enables and disables the auto enable mode. In this mode, the $\overline{CTS}$ and $\overline{DCD}$ pins control operation of the transmitter and receiver, respectively. If the input pin is high, the Tx or Rx is disabled. The $\overline{RTS}$ pin outputs the current transmitter status. The pin remains low during transmission and returns high only after all characters have been sent. The auto enable mode is enabled by setting bit D5 to one and disabled by resetting bit D5 to zero. With bit D5 = 0, $\overline{CTS}$, $\overline{DCD}$, and $\overline{RTS}$ function as normal inputs and outputs.

Enter Hunt Phase [D4]

Valid in COP or BOP mode, this bit forces the AMPSC to enter the Hunt Phase. In the Hunt Phase, the μPD72001 searches the received data stream for either a sync or flag before it begins loading data into the Rx FIFO.

Receive CRC Calculator Enable [D3]

Valid only in COP or BOP mode, bit D3 determines whether or not a CRC calculation is to be performed on the received data. The CRC is calculated 8 bit times after a byte is transferred into the receive FIFO. If bit D3 is reset before this time, the byte will not be included in the CRC calculation. The bit must be set again after the next byte is received to resume the CRC calculation.

Address Search Mode Enable [D2]

Valid only in BOP mode, bit D2 determines whether or not the address field value of a received frame is to be compared with the value set in CR6. If the bit is set to one, Address Search is enabled and the AMPSC checks the first byte of the frame. If the byte matches CR6 or the global address (FFH), the frame is received. If the byte does not match, the AMPSC enters the Hunt mode again, and the byte and the rest of the frame are blocked and not received. If Multicast mode is enabled (bit D1), only the four most significant bits (D7-D4) of the address byte are compared.

Sync Character Load Inhibit/Multicast Enable [D1]

Valid only in COP or BOP mode, bit D1 has a different meaning in each mode. In COP mode, setting bit D1 to one enables the Sync Character Load Inhibit function. This prevents any byte that matches the value in CR6 from being loaded into the receive FIFO and being included in the CRC calculation.

In BOP mode, bit D1 enables the Multicast function. In this mode, which is a modified form of the address search mode, only the most significant four bits of the received address are compared with the identical bits of CR6. Frame acceptance will function in the same way as in the address search mode.

Receiver Enable [D0]

This bit enables and disables the receiver. Setting bit D0 enables the receiver, resetting it disables the receiver.

Control Register CR4

Clock Rate [D7-D6]

Bits D7 and D6 select the clock rate divisor. They are ignored in the internal synchronous modes. In the external synchronous mode, only the x1 and x16 selections are valid.

In asynchronous mode, the following values apply:

Bits D7-D6	Divisor
00	x1
01	x16
10	x32
11	x64

The divisor value is the factor by which the supplied data clock is greater than the data rate for the transmitter and receiver. The data clock source is selected by the clock multiplexer. It can be set to any of the BRG, DPLL, or external clock sources. The divisor determines the number of times that the received data is sampled per bit time by the receiver. Also, it determines the composition of the transmitter output.

Protocol Mode [D5-D4]

Bits D5-D4 select the synchronous protocol, which are used when synchronous mode is selected with bits D3-D2.

Bits D5-D4	Mode
00	Mono-Sync, character synchronous
01	Bisync, character synchronous
11	External Sync, character synchronous
10	HDLC, bit synchronous

Tx Stop Bits/Sync Mode [D3-D2]

Bits D3-D2 select the number of stop bits sent after each byte in Asynchronous mode, or they select the Synchronous mode.

Bits D3-D2	Mode
00	Sync mode
01	Async mode, 1 stop bit
10	Async mode, 1.5 stop bits
11	Async mode, 2 stop bits

Parity Select [D1]

Valid in Asynchronous and COP modes, bit D1 selects the parity type: 0 = odd and 1 = even. It is used only when the Parity Enable bit D0 of CR4 is set to one.

Parity Enable [D0]

Bit D0 enables the parity bit calculation on transmitted data and parity checking on received data. Setting bit D0 enables parity; resetting bit D0 disables parity. If the length of the received character is 7 bits or less, the parity bit can be read in the received data byte. If parity is disabled, no parity bit is transmitted and none is expected on receipt.

Control Register CR5

$\overline{\text{DTR}}$ Control [D7]

This bit controls the $\overline{\text{DTR}}$ pin status: 0 = high and 1 = low. The $\overline{\text{DTR}}$ pin function is disabled if channel B is operating in the DMA mode (CR2A bits D1-D0 = 10)

Transmit Character Bit Length [D6-D5]

These bits specify the bit count per character in transmitted data.

Bits D6-D5	Bits/Character
00	5 or fewer
01	7
10	6
11	8

If the bit count per character is 6 or 7, only the low-order bits of the byte are valid and the most significant bit(s) are ignored. If the count is 5 bits or lower when writing into the transmit data register, refer to the data format that is shown in table 5.

Table 5. Parallel Data Format for One to Five Bits per Character

Bits	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	0	0	D0
2	1	1	1	0	0	0	D1	D0
3	1	1	0	0	0	D2	D1	D0
4	1	0	0	0	D3	D2	D1	D0
5	0	0	0	D4	D3	D2	D1	D0

Dn = Effective data bit

Send Break/Abort [D4]

Bit D4 controls the break or abort transmission according to the selected operation mode. In asynchronous mode, bit D4 controls sending the break signal (TxD set to spacing (0) condition). Setting bit D4 to one begins sending the break signal; resetting it to zero returns the transmitter to normal operation.

In COP mode with Tx on Loop selected (bits 4 and 1 in CR10), setting bit D4 causes the transmitter to be synchronized with the receiver. The bit is reset automatically when synchronization is achieved.

In BOP mode, setting bit D4 to one causes eight 1-bits (abort sequence) to be sent. After completion of the message, bit D4 is reset automatically and the transmitter returns to the idle state.

Transmit Enable [D3]

Disable. Setting bit D3 to the zero state disables the transmitter function. If the transmitter is currently sending a character, the AMPSC waits until the character is completed before setting TxD to the marking (1) state. If bit D3 is reset during transmission of a CRC character, a SYNC character or flag is sent in place of the CRC character.

If D3 is reset in the COP or BOP mode, the Tx Underrun/EOM bit (SR1 bit D6) is set.

If the AMPSC is in the SDLC Loop mode (refer to CR10) or Echo Loop Test (refer to CR14), the TxD pin is connected to RxD, and is not set to marking.

Enable. Setting bit D3 to the one state enables the transmitter to start transmission. If the Auto Enable mode is selected (CR3 bit D5 = 1), the signal applied to the CTS pin controls the transmitter operation.

CRC Polynomial [D2]

This bit selects the polynomial used for CRC calculation. It is valid only in COP or BOP mode. Only the CCITT polynomial is used in BOP mode. Bit 7 of CR10 sets the initial value of the CRC calculator.

D2 = 0 (CRC-CCITT): The generating polynomial expression is $X^{16} + X^{12} + X^5 + 1$.

D2 = 1 (CRC-16): The generating polynomial expression is $X^{16} + X^{12} + X^2 + 1$.

$\overline{\text{RTS}}$ Control [D1]

Bit D1 controls the $\overline{\text{RTS}}$ pin. Setting bit D1 to the zero state causes $\overline{\text{RTS}}$ to be high, setting it to the one state causes it to go low. If Auto Enable mode is selected in Asynchronous mode, $\overline{\text{RTS}}$ operates differently. If the bit remains at zero from the start of transmission through to the end, $\overline{\text{RTS}}$ will stay high. If it is set to one, it remains low. If it starts set to one and is then set to zero while transmitting, $\overline{\text{RTS}}$ will not go high until all data is transferred out of the Tx shift register.

Transmit CRC Calculator Enable [D0]

Valid only in the COP or BOP mode, bit D0 determines whether or not transmitted data is included in the CRC calculation. If bit D0 is set when the byte is transferred into the Tx shift register, the byte is included in the Tx CRC calculation. Bit D0 should be set or reset before loading a data byte into the AMPSC.

Control Register CR6

Valid only in the COP or BOP mode, this byte (bits D7-D0) specifies the SYNC character pattern or address value.

In Monosync or External Sync mode, D7-D0 holds the transmit Sync character. In Bisync mode, the low-order byte of the Sync pattern is set in D7-D0.

If the sync character is 6 bits (CR10 bit D0 = 1), bits D3-D0 should be set to one.

In mono or external sync bits D1 and D0 are repeated in positions D7 and D6.

In BOP mode, this byte is the secondary address.

Control Register CR7

Valid only in the COP or BOP mode, these bits specify the Sync character or flag.

In Monosync mode, D7-D0 holds the receive Sync character. In BISYNC mode, the high-order byte of the Sync character is set in D7-D0. These bits are not used in External Sync mode.

In BOP mode, the flag pattern (01111110) is set in bits D7-D0.

Control Register CR8

Valid only in the BOP mode, CR8 bits D7-D0 hold the low byte (bits 7-0) of the transmit data length. Register pair CR8 and CR9 must be set before the Tx Data Length Counter Enable bit (D1 of CR13) and Tx Enable bit (D3 of CR5) are set. The transmit data length register (TxDLR) is used to automate the sending of HDLC frames. See the description of CR13 for detail information.

Control Register CR9

Valid only in the BOP mode, CR9 bits D7-D0 hold the high byte (bits 15-8) of the transmit data length. Register CR9 is paired with CR8.

Control Register CR10

Initial CRC State [D7]

Valid only in the COP or BOP mode, bit D7 specifies the initial state of the CRC calculation circuit. Setting this bit to zero causes the CRC to be initialized to zero when the Initialize CRC command (CR0 bits 7-6) is performed. Setting this bit to one causes the CRC to be set to all ones.

Data Format [D6-D5]

These bits specify the serial data format and enable the corresponding encoder/decoder.

Bits D6-D5	Format
00	NRZ
01	NRZI
10	FM1
11	FM0

With NRZ format, it is possible to decode Manchester encoded data by setting the DPLL mode to FM (CR14 bits D7-D5 = 110).

Auto Tx on Sync/Tx on Loop [D4]

Bit D4 is valid only in the COP or BOP mode. In COP mode, it synchronizes the receiver with the transmitter. In BOP mode, it controls SDLC loop operation. The bit is valid only when the Loop Enable state (CR10 bit D1 = 1) is selected.

In COP mode, bit D4 provides the Auto Tx on Sync function to synchronize receiver and transmitter operation.

(1) D4 = 0. The Auto Tx on Sync function (CR10 bit D1 = 1) is disabled. Once synchronization is established after this bit is set to 1, resetting the bit to 0 does not affect synchronization.

(2) D4 = 1. If bit D1 (Loop Enable) is also set to one, the transmitter is disabled and the receiver enters the Hunt Phase. When the SYNC character is detected, character synchronization is established, the transmitter is enabled, and data transmission can begin. The state of character synchronization can be determined from the state of the Tx Sync/GA Detect bit (SR10 bit D1).

In BOP mode, bit D4 set to one enables or bit D4 set to zero disables the Tx on Loop function. It is used for data transmission during the SDLC loop operation.

(1) D4 = 0. Once the AMPSC forms a loop and starts transmission, bit D4 must be reset to zero. This allows the CRC and flag to be automatically transmitted if a Tx Underrun/EOM occurs and allows the AMPSC to be subsequently placed in Loop mode with a 1-bit delay. Bit D4 must be reset before the CRC transmission is completed.

(2) D4 = 1. When the Loop Enable bit (CR10 bit D1) is set to one, SDLC Loop Operation mode is selected, in which the RxD input is connected to the TxD output within the AMPSC to form a loop. The GA (Go Ahead) pattern detection is initiated. If the GA pattern (11111110 = FEH) is detected, a 1-bit delay is inserted between RxD and TxD and the GA pattern detection is continued. At this point, the transmitter remains disabled. The receiver can be enabled at this point. Subsequently, if the GA pattern is detected, the transmitter is enabled. At this point, the GA pattern is automatically transformed into a flag so that any data in the Tx buffer may be transmitted following the flag. Once transmission is started, bit D4 must be reset before the end of the frame.

Idle Condition [D3]

Valid only in BOP mode, bit D3 determines the type of information to be transmitted following a closing flag or completion of the Send Abort. If bit D3 is zero, flags will be sent; if it is a one, continuous marks (ones) will be sent.

Transmit Condition on Underrun [D2]

Valid only in the BOP mode, bit D2 determines transmitter action when a Tx Underrun condition occurs. If bit D2 is reset, Tx Underrun/EOM generates either the CRC followed by a flag or just a flag depending on the state of the Tx Underrun bit (SR1 bit D6) and the CRC enable bit (CR5 bit D0). If the CRC is disabled or the Tx underrun bit is a one, only flags are sent. Otherwise, the CRC is sent followed by flags. If bit D2 is set, the abort message is sent followed by flags.

Auto Tx/Loop Enable [D1]

Valid only in the COP or BOP mode, bit D1 enables the two types of loop operations that are set with bit D4. This bit should be set before the transmitter or receiver is enabled.

SYNC Character Length [D0]

Valid only in the COP mode, bit D0 determines the number of bits per SYNC character. Setting bit D0 to zero gives a character length of 8 bits in Mono-sync and 16 bits in Bisync. With bit D0 = 1, the character lengths are 6 and 12 bits, respectively.

Control Register CR11

Each bit of CR11 controls an E/S interrupt request generated by the AMPSC. An interrupt is set if the E/S interrupts are enabled (CR1 bit D0 = 1). For the causes of interrupts assigned to each, refer to the description of SR1. Setting each bit to one enables it as a source of interrupts.

Break/Abort/Go Ahead Interrupt Enable [D7]

In Asynchronous and COP modes, bit D7 enables interrupts at the beginning and end of each detected break condition (a null character plus a framing error).

In BOP mode, when not in SDLC loop, bit D7 enables interrupts at the beginning and end of each received abort condition (seven or more consecutive 1-bits). In SDLC loop mode, bit D7 also enables interrupts for detecting the GA pattern (11111110 = FEH).

Transmitter Underrun/End of Message Interrupt Enable [D6]

Valid only in the COP or BOP mode, bit D6 enables interrupts caused by transmitter underrun and Tx End of Message detection.

$\overline{\text{Clear to Send}}$ Interrupt Enable [D5]

Bit D5 enables interrupts caused by a change of state on the $\overline{\text{CTS}}$ pin.

$\overline{\text{SYNC}}$/Hunt Interrupt Enable [D4]

Bit D4 enables interrupts caused by a change in the $\overline{\text{SYNC}}$/Hunt state.

$\overline{\text{Data Carrier Detect}}$ Interrupt Enable [D3]

Bit D3 enables interrupts caused by a change of state on the $\overline{\text{DCD}}$ pin.

All Sent Interrupt Enable [D2]

Valid only in the Asynchronous or BOP mode, bit D2 enables interrupts generated by the All-Sent condition.

Idle Detect Interrupt Enable [D1]

Valid only in the BOP mode, bit D1 enables interrupts caused by a change in the Idle Detection condition.

BRG Interrupt Enable [D0]

Bit D0 enables interrupts caused by one of the baud rate generator/timers (BRG) counting down from one to zero. Also, each of the BRGs must be enabled in CR12 bits D3-D2.

Control Register CR12

BRG Select for TRxC [D7]

When BRG is selected as the source of the clock at the TRxC pin (CR15 bits D1-D0 = 10), and the TRxC pin is set to output (CR15 bit D2 = 1), bit D7 selects TxBRG (one state) or RxBRG (zero state).

BRG Select for DPLL [D6]

Bit D6 selects the source (TxBRG or RxBRG) for the DPLL. It is valid when the BRG is selected as the source for the DPLL circuit (CR14 bits D7-D5 = 100). Setting bit D6 to one selects TxBRG and setting it to zero selects RxBRG.

Transmit BRG Interrupt Enable [D3]

Bit D3 enables an E/S interrupt when the TxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Receive BRG Interrupt Enable [D2]

Bit D2 enables an E/S interrupt when the RxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Transmit BRG Register Set [D1]

Bit D1 is used to write the time constant value into the TxBRG register. When D1 is set to one, the next two bytes written to the AMPSC are assumed to be the time constant value. The lower byte is written in the first write cycle and the upper byte in the second write cycle. Bit D1 is automatically reset after the register is loaded.

The time constant value is calculated by using the following formula.

$$\text{Time constant} = \frac{\text{Source clock frequency (Hz)}}{2 \times (\text{Data clock rate (BPS)})} - 2$$

The data clock rate is the transmitted or received data rate multiplied by the clock factor specified in CR4 bits D7-D6.For example, if the system clock is selected as the BRG source (CR14 bit D2 = 1) at 8 MHz and the BRG is the transmitter source (CR15 bits D4-D3 = 10) with a clock factor of x16 (CR4 bits D7-D6 = 01) and data rate of 9600 bits per second, the calculation would be as follows.

$$\frac{8 \times 10^6}{2 \times (9600 \times 16)} - 2 = 24.04 = 0018 \text{ (hex)}$$

The loading sequence in hexadecimal for the TxBRG would be; 0C, 02, 18, and 00.

If data is being written while the BRG is running, the value will not be loaded into the BRG until it counts down to zero.

Receive BRG Register Set [D0]

Bit D0 is used to write the count value into the RxBRG register. It operates in the same manner as bit D1 for the TxBRG register.

Control Register CR13

Transmit Data Length Counter Enable [D1]

Bit D1 enables the transmit data length counter (TxDLC) that is used to determine the end of a transmitted frame and is only valid in BOP mode. When bit D1 is set to one, the TxDLC (SR8-SR9) is incremented each time a Tx interrupt or DMA request is generated, and the value is compared with the value in the transmit length register (TxLR) (CR8-CR9). If the two values are equal, Tx interrupts/DMA requests are masked.

The subsequent Tx buffer empty interrupt is masked and no interrupt or DMA request is made. This results in a transmitter underrun. The AMPSC then sends the CRC and a closing flag. After this the AMPSC issues an external status interrupt with the All Sent bit set.If the transmitter underruns and the transmit length values do not match, then the MPSC sends an abort and sets the Sending Abort bit (SR0 bit D1). An E/S Interrupt for the All Sent is generated. The TxLC value (SR8-SR9) can also be compared with the frame length to determine if correct transmission occurred. After the abort is sent, the TxDLC enable bit must be set to one again in order to generate new Tx interrupts/DMA requests.

Standby Mode Set [D0]

Setting bit D0 to one places the AMPSC in the Standby mode. This mode consumes very little power but saves all internal register values. Greater power reduction is possible by not toggling any of the AMPSC inputs. In this mode, the system clock (CLK) and the data clocks are not circulated within the AMPSC.

The AMPSC enters the Standby mode automatically after RESET. Writing 00H to CR0, restores normal operation. Table 6 lists the status of the pins in standby mode.

During Standby mode, the $\overline{WR}$ and $\overline{RD}$ pins must be held high and the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins can not be toggled. Read cycles that are conducted will not result in data being driven onto the bus.

Table 6. Pin Status In Standby Mode

Pin Symbol	Input/Output	Pin Status
$\overline{WR}$	Input	Unchanged
$\overline{RD}$	Input	Unchanged
B/$\overline{A}$	Input	Unchanged
C/$\overline{D}$	Input	Unchanged
D_7-D_0	Input/Output	High impedance
$\overline{INT}$	Output	Retains the current state
$\overline{INTAK}$	Input	Unchanged
$\overline{PRI}$	Input	Unchanged
$\overline{PRO}$	Output	Depends on PRI
DRQTxA	Output	Retains the current state
DRQRxA	Output	Retains the current state
$\overline{DTRA}$/DRQTxB	Output	Retains the current state
$\overline{DTRB}$/DRQRxB	Output	Retains the current state
TxDA, TxDB	Output	Retains the current state
RxDA, RxDB	Input	Unchanged
$\overline{TRxCA}$, $\overline{TRxCB}$	Input/Output	High impedance
$\overline{STRxCA}$, XI1A	Input	Unchanged
$\overline{STRxCB}$, XI1B	Input	Unchanged
XI2A/$\overline{SYNCA}$	Input/Output	High impedance
XI2B/$\overline{SYNCB}$	Input/Output	High impedance
$\overline{RTSA}$, $\overline{RTSB}$	Output	Retains the current state
$\overline{CTSA}$, $\overline{CTSB}$	Input	Unchanged
$\overline{DCDA}$, $\overline{DCDB}$	Input	Unchanged

Control Register CR14

DPLL Command [D7-D5]

These bits control the digital phase-locked loop (DPLL). After reset, the DPLL is disabled, the $\overline{STRxC}$ pin is selected as the source clock, and the NRZ1 mode is selected. The DPLL commands corresponding to the eight states of bits D7-D5 are described below.

No Operation [000]. This command causes no operation.

Enter Search [001]. This command causes the DPLL to start the detection of edges in received data. Circuit operation depends on the data format.

Reset Missing Clock [010]. Valid when FM mode is selected, this command resets the Missing Clock bits (SR10 bits D7-D6).

Disable [011]. This command stops DPLL operation and resets the Missing Clock bits.

Source BRG Select [100]. This command selects one BRG as the clock source for the DPLL. Selection of TxBRG or RxBRG is determined by CR12 bit D6 (BRG Select for DPLL).

Source Xtal/$\overline{\text{STRxC}}$ Select [101]. This command is used when the crystal-controlled oscillator or a clock applied to the $\overline{\text{STRxC}}$ pin is to be the source clock for the DPLL. Selection between the crystal OSC and the $\overline{\text{STRxC}}$ input is specified by CR15 bit D7 (Xtal Select).

FM Mode [110]. This command is used when received data is to be treated as FM format. Setting the data format to NRZ (CR10 bits D6-D5 = 00) allows the μPD72001 to decode Manchester encoded data.

NRZI Mode [111]. This command is used when received serial data is to be treated as NRZI format.

Local Self Test [D4]

When bit D4 is set to one, the transmitter output is directly connected to the input of the receiver within the AMPSC. Signals applied to the RxD pin will be ignored. In this mode, Autoenable cannot be used to control the transmitter or receiver.

Echo Loop Test [D3]

When bit D3 is set to one, the RxD input pin is connected to the TxD output pin in the AMPSC, so that the received data is echoed back to the remote sender for line testing. The AMPSC transmitter is disabled.

BRG Source Select [D2]

Bit D2 selects the source clock for the BRGs. The selected source clock is shared by the TxBRG and the RxBRG. If D2 is set to one, the system clock is used as the source clock. If D2 is set to zero, the source clock can either be the crystal oscillator (CR15 bit D7 = 1) or the $\overline{\text{STRxC}}$ input (CR15 bit D7 = 0).

Receive BRG Enable [D1]

Setting bit D1 to one starts the RxBRG, which takes two clocks to begin operating.

Transmit BRG Enable [D0]

Setting bit D0 to one starts the TxBRG, which takes two clocks to begin operating.

Control Register CR15

Crystal Select [D7]

If bit D7 is set to one, the on-chip crystal oscillator is enabled and a crystal can be connected across pins XI1 and XI2. If bit D7 is zero, the oscillator is disabled and the pins become $\overline{\text{SYNC}}$ and $\overline{\text{STRxC}}$.

Receive Clock Select [D6-D5]

These bits select the source for the receive data clock.

Bits D6-D5	Receive Clock Source
00	Clock applied to $\overline{\text{STRxC}}$ pin
01	Clock applied to $\overline{\text{TRxC}}$ pin (CR15 bits D2-D0 are invalid)
10	RxBRG output
11	DPLL output

Transmit Clock Select [D4-D3]

These bits select the source for the transmit data clock.

Bits D4-D3	Transmit Clock Source
00	Clock applied to $\overline{\text{STRxC}}$ pin
01	Clock applied to $\overline{\text{TRxC}}$ pin (CR15 bits D2-D0 are invalid.)
10	TxBRG output
11	DPLL output

$\overline{\text{TRxC}}$ Input/Output [D2]

Bit D2 determines whether the $\overline{\text{TRxC}}$ pin will be an input or an output. It is an input if bit D2 = 0 or if the pin is specified as an input by bits D6-D5 or D4-D3.

$\overline{\text{TRxC}}$ Source Select [D1-D0]

When the $\overline{\text{TRxC}}$ pin is selected as an output, these bits determine the output source. Refer to the preceding descriptions for D6-D5, D4-D3, and D2 to determine when the $\overline{\text{TRxC}}$ pin is an output.

Bits D1-D0	Output at Pin $\overline{\text{TRxC}}$
00	On-chip crystal oscillator (if enabled)
01	Transmit data clock
10	TxBRG or RxBRG as selected by CR12 bit D7
11	DPLL output

Status Register SR0

End of Frame [D7]

Valid only in the BOP mode, bit D7 indicates if reception of a single frame is complete. When this bit is one, a complete frame has been received and the CRC Error bit (SR0 bit D6) and Residue Code (SR3 bits D2-D0) are valid. The EOF condition causes a Special Rx Condition interrupt. The Error Reset command resets this bit.

CRC/Framing Error [D6]

In the asynchronous mode, bit D6 indicates a framing error. It is set to one if a zero is detected at the stop bit position. It generates a Special Rx Condition interrupt. Bit D6 is reset by an Error Reset command or reception of a normal data byte.

In the COP or BOP mode, bit D6 set to one indicates a CRC error. Bit D6 set to zero indicates no CRC error.

In the COP mode, bit D6 is valid 20 bit times subsequent to the last bit of the second CRC byte that is input at the RxD pin, or 16 bit times after the second CRC byte is transferred to the Rx buffer.

In the BOP mode, bit D6 is valid when the End-of-Frame bit (SR0 bit D7) is set to one.

A CRC error does not generate a Special Rx Condition interrupt.

Receive Overrun Error [D5]

A one in bit D5 indicates an Rx Overrun error. This error occurs each time the AMPSC attempts to transfer an additional byte from the Rx shift register to the Rx FIFO and the FIFO is already full.

An Rx Overrun error causes a Special Rx Condition interrupt. The timing of the Rx Overrun Error and the resulting Special Rx Condition interrupt will differ depending on the setting of the Overrun Error INT bit (CR1 bit D6). For more details, refer to the description of control register CR1.

The Rx Overrun Error bit is reset by the Error Reset command.

Parity Error [D4]

Valid only in the Asynchronous or COP mode when parity is enabled (CR4 bit D0 = 1). A one in bit D4 indicates that a parity error occurred in a received byte. The Parity Error bit is reset by the Error Reset command.

In the All Receive INT-1 mode (CR1 bits D4-D3 = 10), a parity error causes a Special Rx Condition interrupt.

Short Frame Detect [D3]

Valid only in the BOP mode when Short Frame Detect Enable is selected (CR1 bit D7 = 1), bit D3 is set when a short frame is received and is reset by the Error Reset command. A short frame has less than 32 bits between two flags.

Detection of a short frame causes a Special Rx Condition interrupt.

Transmit Buffer Empty [D2]

A one in bit D2 indicates that the Tx buffer is empty and can be loaded with the next Tx byte. Bit D2 is zero when the Tx buffer contains a byte that has not been transferred to the Tx shift register. Bit D2 is also zero in the COP or BOP mode during CRC transmission.

Sending Abort [D1]

Valid only in the BOP mode, a one in bit D1 indicates that the AMPSC is sending an abort sequence.

Bit D1 is reset by the Error Reset command. Status changes in bit D1 do not cause an interrupt.

Receive Data Available [D0]

A one in bit D0 indicates the presence of valid received data in the Rx buffer of the AMPSC.

Status Register SR1

This register consists of external status bits that indicate the causes of E/S interrupts. If the E/S INT is enabled (CR1 bit D0 = 1) and an interrupt by an specific E/S bit is enabled, the changes in the pertinent E/S bit states are latched and cause an E/S interrupt. If the E/S interrupt is disabled, changes in the E/S bit status will not be latched.

Break/Abort/Go Ahead Detect [D7]

Bit D7 is valid only in the Asynchronous or BOP mode. In the Asynchronous mode, a one in bit D7 indicates that a Break (character in which the start, stop, and data bits are all zeros) has occurred. Data received during the Break (all zeros) are not loaded into the Rx FIFO.

In the BOP mode, bit D7 indicates the reception of an abort (seven or more consecutive ones). In SDLC Loop mode, bit D7 indicates reception of the Go Ahead message (11111110 = FEH).

Transmit Underrun/End of Message [D6]

Valid only in the COP or BOP mode, a one in bit D6 indicates that all transmit data has been transferred to the Tx shift register. CRC transmission, when the transmitter underruns, can be controlled by manipulating this bit.

If CRC transmission is desired when the transmitter underruns, bit D6 must be reset to zero by the Reset Tx Underrun/EOM command bit (CR0 bits D7-D6 = 11). Before this command is issued, the transmitter must be enabled and at least one byte must have been transferred to the Tx buffer.

In the BOP mode, bit D6 is automatically reset to zero when the first byte is transferred after transmission is enabled. A status change from one to zero in this bit does not cause an E/S interrupt.

Clear To Send [D5]

Bit D5 indicates the inverted state of the $\overline{CTS}$ pin. Any change causes an interrupt.

Sync/Hunt [D4]

In the Asynchronous or external sync COP mode, bit D4 indicates the inverted state of the SYNC pin.

In the internal sync COP or BOP mode, bit D4 indicates the AMPSC synchronization state. A zero in bit D4 indicates that synchronization is established. A one indicates that the AMPSC is in the Hunt Phase or that the receiver is disabled.

Any change in state generates an interrupt.

Data Carrier Detect [D3]

Bit D3 indicates the inverted state of the $\overline{DCD}$ pin. Any change generates an interrupt.

All Sent [D2]

Valid only in the Asynchronous or BOP mode. Bit D2 set to one indicates that all the transmit data within the AMPSC has left the Tx shift register. The one to zero state transition of this bit does not generate an interrupt.

Idle Detect [D1]

Bit D1 set to one indicates detection of the Idle state (15 or more consecutive 1's) in BOP mode. The one to zero state transition of this bit does not generate an interrupt.

BRG Zero Count [D0]

Bit D0 set to one indicates that one of the BRG's has counted down to zero. Bits D4-D3 of SR3 determine which BRG counted out. The one to zero state transition of this bit does not generate an interrupt.

Status Register SR2B

This register indicates the value of the interrupt vector. It can only be read from the B channel. The value depends on the state of CR2A bit D6 (Status Affects Vector bit). If bit D6 is zero, SR2B will always equal CR2B. If bit D6 is one, the value of SR2B is modified by the cause of the highest priority interrupt source within the μPD72001.

The bits of SR2B that are affected depend on the Output Vector Type setting. Bits V4-V2 are affected for Type A vectors, and bits V2-V0 for Type B vectors. All other bits remain unchanged. Table 7 gives the value returned for the various types of interrupts.

Table 7. Vector Values in SR2B

V4, V2	V3, V1	V2, V0	Channel	Condition
0	0	0	B	Tx buffer empty
0	0	1		External/status
0	1	0		Rx data available
0	1	1		Special Rx condition
1	0	0	A	Tx buffer empty
1	0	1		External/status
1	1	0		Rx data available
1	1	1		Special Rx condition

When interrupts are available in the non-vectored mode (CR2A bit D7 = 0), SR2B is read in order to indicate to the μPD72001 that interrupt service has started. This clears the interrupt request (INT) and prevents lower priority interrupts from being generated until the End of Interrupt command (CR0) is issued.

Status Register SR3

TxBRG Zero Count [D4]

Bit D4 is valid when TxBRG is enabled (CR14 bit D0 = 1). A one in bit D0 indicates that the TxBRG counted down to zero. This bit in conjunction with the SR1 bit D0, causes an external/status interrupt and is latched on a transition from zero to one. The transition from one to zero does not cause an interrupt.

RxBRG Zero Count [D3]

Bit D3 is valid when RxBRG is enabled (CR14 bit D1 = 1). A one in bit D3 indicates that the RxBRG counted down to zero. This bit functions in the same manner as bit D4.

Residue Code [D2-D0]

Valid only in the BOP mode, bits D2-D0 indicate the number of valid bits in the last data byte received in a frame. The meaning of these bits depends on the number of bits per data byte. The previous character refers to the last character read before the end of frame, and so on. See Table 8. Figure 6 is an example of a residue code of 000 and a character length of 8 bits. It indicates that bits zero and one in the last byte are valid.

Figure 6. Example of Valid Bits in the I-Field (Residue Code = 000)

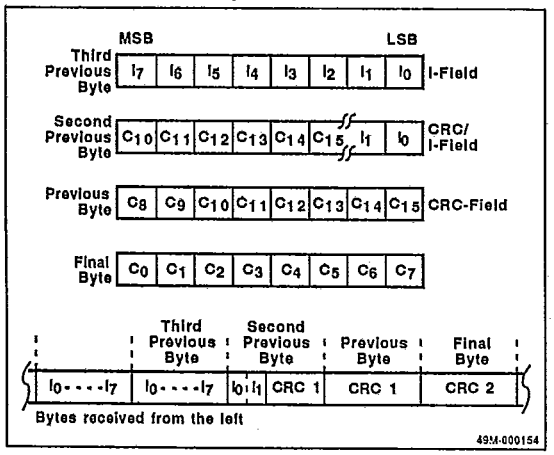


Table 8. Residue Codes

D2	D1	D0	Previous Character MSB							LSB	2nd Previous Character MSB							LSB
8 Bits per Character																		
0	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D
0	0	1	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D
0	1	0	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D
0	1	1*	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D
1	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D
1	0	1	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D
1	1	0	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D
1	1	1	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D	D
7 Bits per Character																		
0	0	0	X	C	C	C	C	C	C	D	X	D	D	D	D	D	D	D
0	0	1	X	C	C	C	C	C	C	C	X	C	C	D	D	D	D	D
0	1	0	X	C	C	C	C	C	C	C	X	C	C	C	C	D	D	D
0	1	1*	X	C	C	C	C	C	C	C	X	D	D	D	D	D	D	D
1	0	0	X	C	C	C	C	C	C	C	X	C	C	C	C	C	D	D
1	0	1	X	C	C	C	C	C	C	C	X	C	D	D	D	D	D	D
1	1	0	X	C	C	C	C	C	C	C	X	C	C	C	D	D	D	D
6 Bits per Character																		
0	0	0*	X	X	C	C	C	C	C	C	X	X	D	D	D	D	D	D
0	0	1	X	X	C	C	C	C	C	C	X	X	C	C	D	D	D	D
0	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	D	D
1	0	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	C	D
1	0	1	X	X	C	C	C	C	C	C	X	X	C	D	D	D	D	D
1	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	D	D	D
5 Bits per Character																		
0	0	0	X	X	X	C	C	C	C	C	X	X	X	C	D	D	D	D
0	0	1	X	X	X	C	C	C	C	C	X	X	X	C	C	D	D	D
0	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	D
1	0	0*	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	C
1	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	D	D

C = CRC bit
D = Valid data
X = Invalid
* = No residue (boundary of the last received data matches the boundary between one byte and the CRC).

Status Register SR4A

Each bit of this register indicates whether or not a corresponding cause of interrupt exists within the AMPSC. A bit is set to one when its matching interrupt is being serviced or if a lower-priority interrupt is pending during the servicing of a higher-priority interrupt. Otherwise, it is zero. Although this register can be read only on channel A, its function is shared by both channels.

Bit	Chan	Description
D7	A	Special Rx condition; INT pending
D6	B	Special Rx condition; INT pending
D5	A	Rx INT pending
D4	A	Tx INT pending
D3	A	E/S INT pending
D2	B	Rx INT pending
D1	B	Tx INT pending
D0	B	E/S INT pending

Status Register SR8

Valid only in the BOP mode, bits D7-D0 of SR8 are the low order byte of the Tx Data Length counter. Register SR8 is normally used to determine if frame transmission completed correctly. If the value of CR8/CR9 does not equal the value of SR8/SR9 when the transmitter underruns, the AMPSC automatically transmits an Abort. Registers SR8 and SR9 are cleared by a reset or when the TxDLC enable bit (CR13 bit D8) is set to one.

Status Register SR9

Valid only in the BOP mode, bits D7-D0 of SR9 are the high order byte of the Tx Data Length counter. Registers SR8 and SR9 are used in conjunction with each other.

Status Register SR10

One Clock Missing [D7]

This bit indicates if a transition has been detected in the received data. It is valid when the FM data format is selected and the DPLL is in operation. With FM data format, a transition (rising or falling) must occur within one bit time at a bit boundary or center. The DPLL uses this transition as a reference for clock generation.

If no transitions occur, the DPLL clock generation may not operate properly. The DPLL detects transitions every 2 bits.

A one in bit D7 indicates no transition was detected in the received data. This bit is latched, and is reset by the Reset Missing Clock command (CR14 bits D7-D5 = 010) or the Enter Search command (CR14 bits D7-D5 = 001).

Two Clocks Missing [D6]

Bit D6 indicates that two consecutive transitions in the received data were missed.

Sending on Loop [D4]

Bit D4 set to the one state indicates that the AMPSC is in the SDLC loop connection and is transmitting. It is valid only in the BOP mode when the SDLC Loop is selected (CR10 bits D4, D1 = 1,1).

Tx Sync/On Loop [D1]

Bit D1 is valid only in the COP or BOP mode. In the COP mode, a one in bit D1 indicates that the transmitter and receiver are synchronized (SYNC character detection on the receiver has been completed) after both the Auto Tx on Sync and the bit D4 Enable bits (CR10 bits D4,D1) were reset, and transmission is enabled for the device.

In the BOP mode, a one in bit D1 indicates that a GA pattern was detected and a 1-bit delay was inserted between the RxD input and the TxD output. Bit D1 remains a one during the time that the SDLC loop is formed. When D1 is zero, the TxD and RxD lines are connected without the delay in loop mode. Bit D1 is also zero when the AMPSC is not in the loop mode.

Status Register SR11

This register directly indicates the value set in CR11 for interrupt enables. The host processor can use SR11 to read the interrupt enable states for the various interrupt sources within the AMPSC.

Status Register SR12

This register indicates the lower 8 bits (bits 7-0) of the value set in the Rx BRG.

Status Register SR13

This register indicates the upper 8 bits (bits 15-8) of the value set in the Rx BRG.

Status Register SR14

This register indicates the lower 8 bits (bits 7-0) of the value set in the Tx BRG.

Status Register SR15

This register indicates the upper 8 bits (bits 15-8) of the value set in the Tx BRG.