High Speed Dual MOSFET Driver

Features

- 6ns rise and fall time with 1000pF load
- 2.0A peak output source/sink current
- 1.2V to 5V input CMOS compatible
- 4.5V to 13V total supply voltage
- Smart logic threshold
- Low jitter design
- Two matched channels
- Outputs can swing below ground
- Low inductance package
- Thermally-enhanced package

Applications

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Nondestructive evaluation
- PIN diode driver
- CCD Clock driver/buffer
- High speed level translator

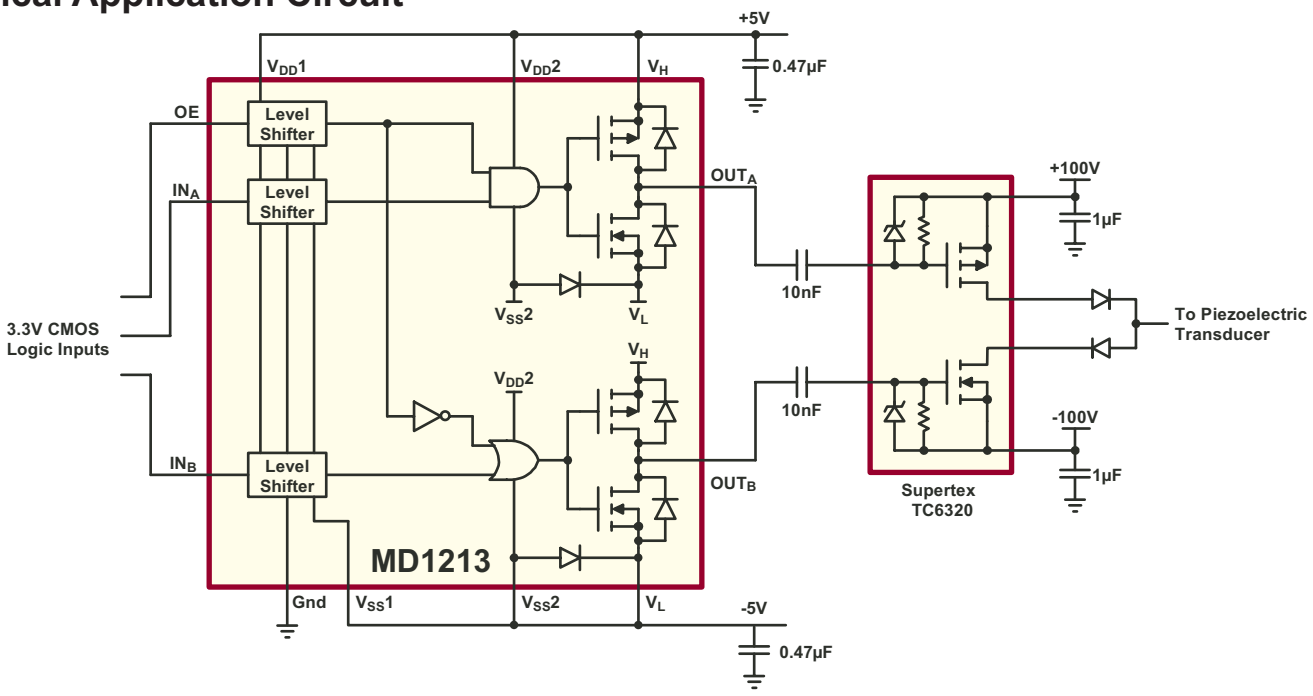
General Description

The Supertex MD1213 is a high speed, dual MOSFET driver. It is designed to drive high voltage P and N-channel MOSFET transistors for medical ultrasound and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1213 can operate from 1.2V to 5.0V logic interface with an optimum operating input signal range of 1.8V to 3.3V. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic 0 and logic 1 levels. The input logic levels may be ground referenced, even though the driver is putting out bipolar signals. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1213 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0 and 1.8volts, the control logic may be powered by +5.0V and –5.0V, and the output L and H levels may be varied anywhere over the range of –5.0V to +5.0V. The output stage is capable of peak currents of up to ±2.0A, depending on the supply voltages used and load capacitance present.

The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Secondly, when OE is low, the outputs are disabled, with the A output high and the B output low. This assists in properly pre-charging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair.

Typical Application Circuit

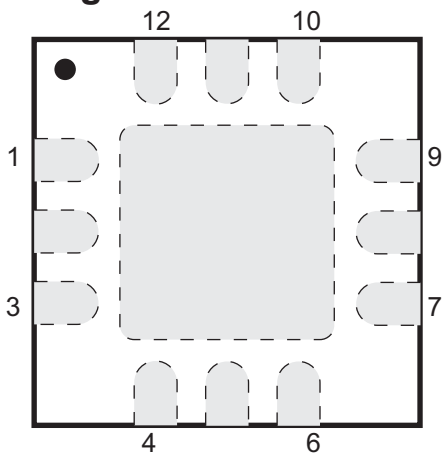


Ordering Information

DEVICE	Package Option
	12-Lead 4x4x0.8pitch QFN
MD1213	MD1213K6-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



12-Lead QFN (K6)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{DD}-V_{SS}, logic supply voltage	-0.5V to +13.5V
V_H, output high supply voltage	V_L - 0.5V to V_{DD} +0.5V
V_L, output low supply voltage	V_{SS} - 0.5V to V_H +0.5V
V_{SS}, low side supply voltage	-7.0V to +0.5V
Logic input levels	V_{SS}-0.5V to V_{SS}+7.0V
Maximum junction temperature	+125°C
Storage temperature	-65°C to 150°C
Operating temperature	-20°C to 85°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Package Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

12-Lead QFN (K6)

DC Electrical Characteristics

(Over operating conditions unless otherwise specified, $V_H = V_{DD1} = V_{DD2} = 12V$, $V_L = V_{SS1} = V_{SS2} = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD} - V_{SS}	Logic supply voltage	4.5	-	13	V	---
V_{SS}	Logic side supply voltage	-5.5	-	0	V	---
V_H	Output high supply voltage	V_{SS} + 2.0	-	V_{DD}	V	---
V_L	Output low supply voltage	V_{SS}	-	V_{DD} - 2.0	V	---
I_{DD1Q}	V_{DD1} quiescent current	-	0.55	-	mA	No input transitions
I_{DD2Q}	V_{DD2} quiescent current	-	-	10	µA	
I_{HQ}	V_H quiescent current	-	-	10	µA	
I_{DD1}	V_{DD1} average current	-	0.88	-	mA	One channel on at 5.0Mhz, No load
I_{DD2}	V_{DD2} average current	-	6.6	-	mA	
I_H	V_H average current	-	23	-	mA	
V_{IH}	Input logic voltage high	V_{OE} - 0.3	-	5.0	V	For logic inputs IN_A and IN_B
V_{IL}	Input logic voltage low	0	-	0.3	V	
I_{IH}	Input logic current high	-	-	1.0	µA	
I_{IL}	Input logic current low	-	-	1.0	µA	

Outputs ($V_H = V_{DD1} = V_{DD2} = 12V$, $V_L = V_{SS1} = V_{SS2} = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	OE Input logic voltage high	1.2	-	5.0	V	For logic input OE
V_{IL}	OE Input logic voltage low	0	-	0.3	V	
R_{IN}	Input logic impedance to GND	12	20	30	KΩ	
C_{IN}	Logic input capacitance	-	5.0	10	pF	All inputs
θ_{JA}	Thermal resistance to air	-	47	-	°C/W	1oz. 4-layer 3x4" PCB with thermal pad and thermal via array
θ_{JC}	Thermal resistance to case	-	7.0	-	°C/W	---
R_{SINK}	Output sink resistance	-	-	12.5	Ω	I_{SINK} = 50mA
R_{SOURCE}	Output source resistance	-	-	12.5	Ω	I_{SOURCE} = 50mA
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

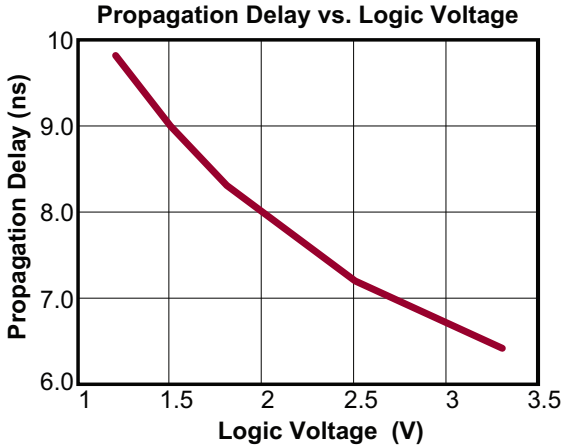
AC Electrical Characteristics ($V_H = V_{DD1} = V_{DD2} = 12V$, $V_L = V_{SS1} = V_{SS2} = 0V$, $V_{OE} = 3.3V$, $T_J = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Inputs or OE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high	-	7.0	-	ns	C_{LOAD} = 1000pF, see timing diagram Input signal rise/fall time of 2ns
t_{PHL}	Propagation delay when output is from high to low	-	7.0	-	ns	
t_{POE}	Propagation delay OE to outputs	-	9.0	-	ns	
t_r	Output rise time	-	6.0	-	ns	
t_f	Output fall time	-	6.0	-	ns	
$\lvert t_r - t_f \rvert$	Rise and fall time matching	-	1.0	-	ns	For each channel
$\lvert t_{PLH} - t_{PHL} \rvert$	Propagation low to high and high to low matching	-	1.0	-	ns	
Δt_{dm}	Propagation delay match	-	±2.0	-	ns	Device to device delay match

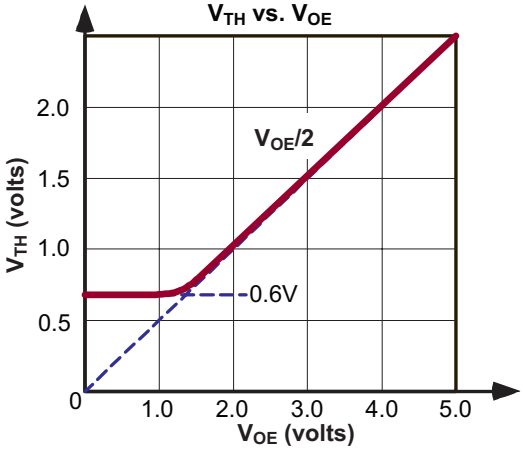
Logic Truth Table

Logic Inputs			Output	
OE	IN_A	IN_B	OUT_A	OUT_B
H	L	L	V_H	V_H
H	L	H	V_H	V_L
H	H	L	V_L	V_H
H	H	H	V_L	V_L
L	X	X	V_H	V_L

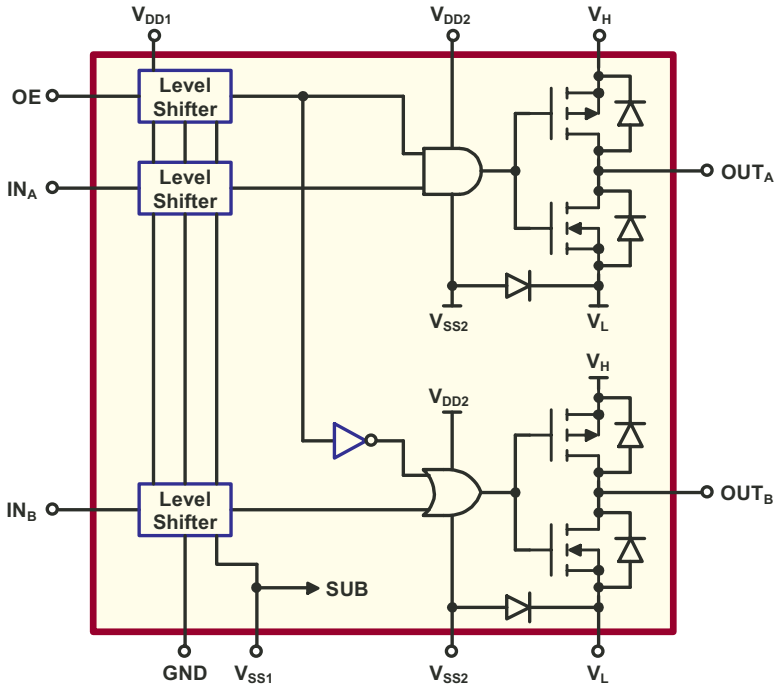
Propagation Delay



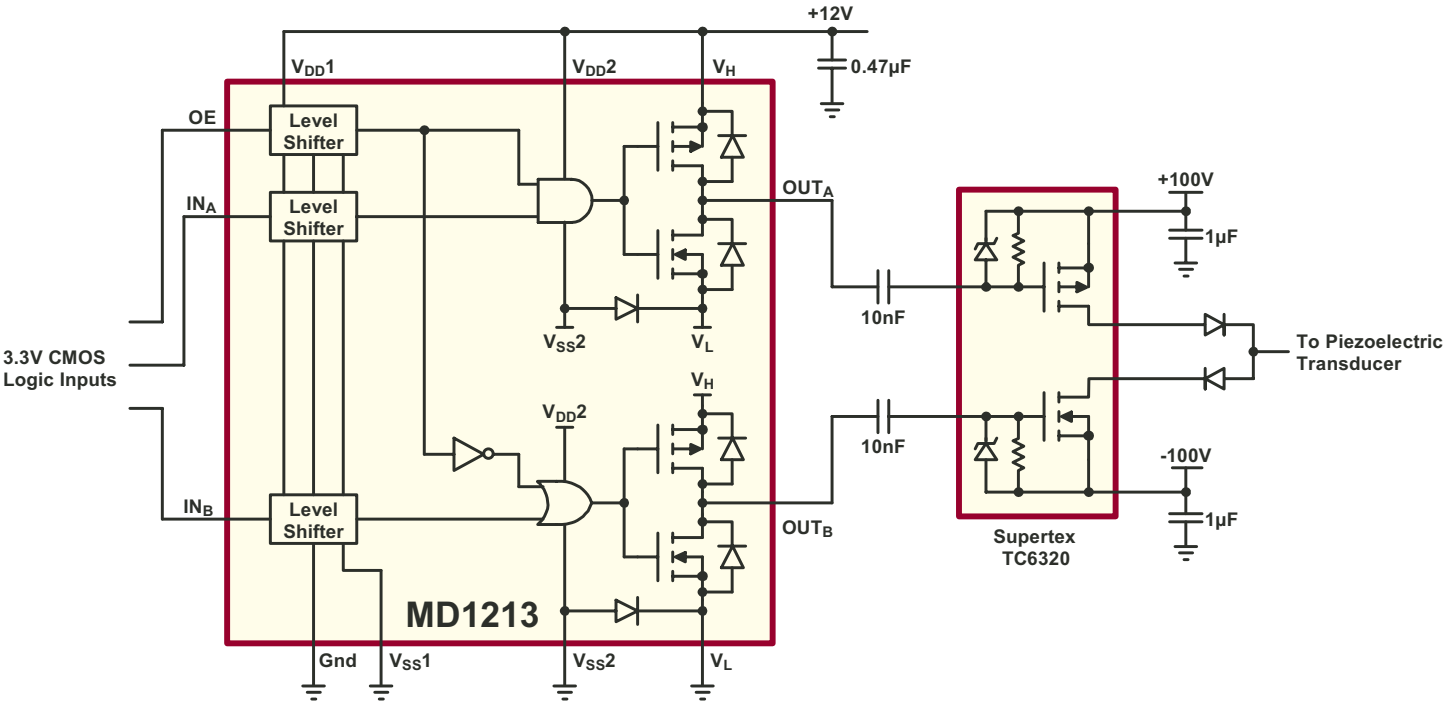
Logic Input Threshold



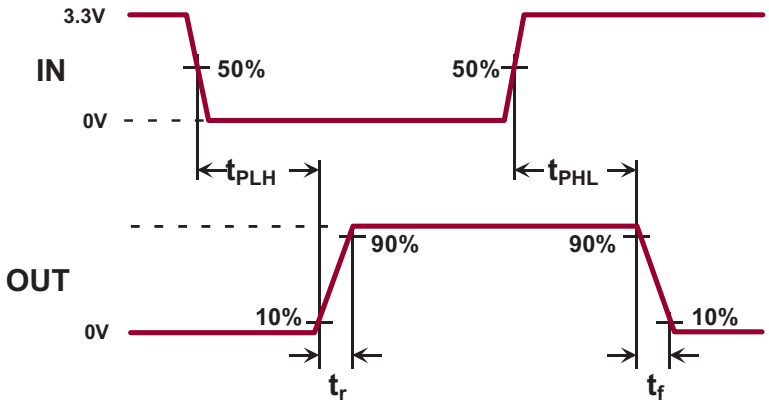
Detailed Block Diagram



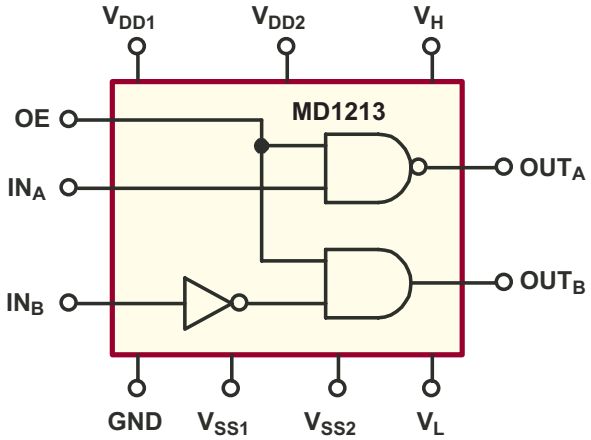
Single Supply Application Circuit



Timing Diagram



Simplified Block Diagram



Application Information

For proper operation of the MD1213, low inductance bypass capacitors should be used on the various supply pins. The GND input pin should be connected to the digital ground. The INA, INB, and OE pins should be connected to their logic source with a swing of GND to logic level high, which is 1.2V to 5.0V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1213 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS1}, V_{SS2}, and V_L pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connections V_{DD1} and V_{DD2} should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads. A common capacitor and voltage source may be used for these two pins, which should always have the same DC voltage applied. For applications sensitive to jitter and noise, separate decoupling networks may be used for V_{DD1} and V_{DD2}.

The supplied voltages of V_H and V_L determine the output logic levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistor in series with the output signal to obtain better waveform integrity at the load terminals.

This will of course reduce the output voltage slew rate at the terminals of a capacitive load. Pay particular attention to the parasitic coupling from the driver output to the input signal terminals. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that the circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

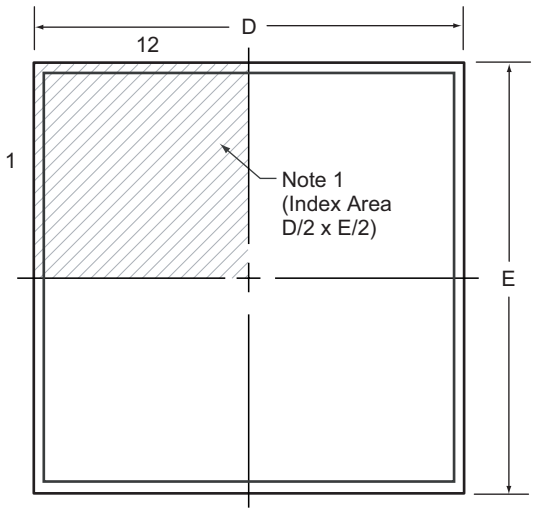
Pin Description

Pin #	Name	Description
1	IN_A	Logic input. Controls OUT_A when OE is high. Input logic high will cause the output to swing to V_L. Input logic low will cause the output to swing to V_H.
2	V_L	Supply voltage for N-channel output stage.
3	IN_B	Logic input. Controls OUT_B when OE is high. Input logic high will cause the output to swing to V_L. Input logic low will cause the output to swing to V_H.
4	GND	Logic input ground reference.
5	V_{SS1}	Low side analog circuit and level shifter supply voltage. Should be at the same potential as V_{SS2}.
6	V_{SS2}	Low side gate drive supply voltage.
7	OUT_B	Output driver. Swings from V_H to V_L. Intended to drive the gate of an external N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUT_B will swing to V_L turning off the external N-channel MOSFET.
8	V_H	Supply voltage for P-channel output stage.
9	OUT_A	Output driver. Swings from V_H to V_L. Intended to drive the gate of an external P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUT_A will swing to V_H turning off the external P-channel MOSFET.
10	V_{DD2}	High side gate drive supply voltage.
11	V_{DD1}	High side analog circuit and level shifter supply voltage. Should be at the same potential as V_{DD2}.
12	OE	Output-enable logic input. When OE is high, $(V_{OE} + V_{GND})/2$ sets the threshold transition between logic level high and low for IN_A and IN_B. When OE is low, OUT_A is at V_H and OUT_B is at V_L regardless of IN_A and IN_B

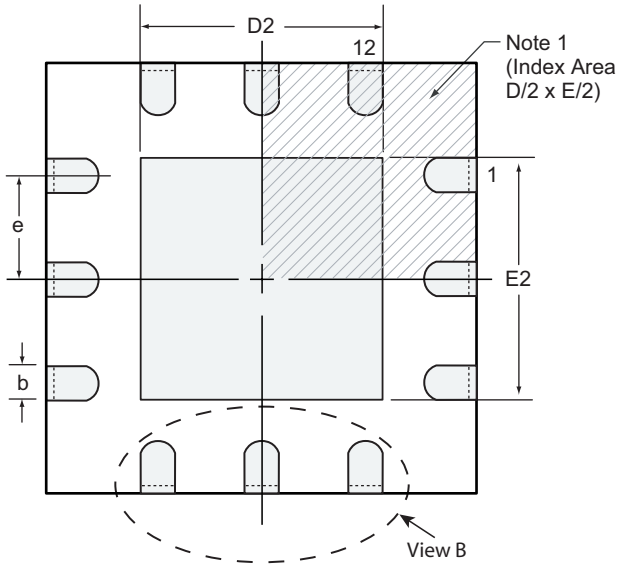
Note: *1.Thermal Pad and Pin#5 (V_{SS1}) must be connected externally.*
2. Index Pad and Thermal Pad are connected internally

12-Lead QFN Package Outline (K6)

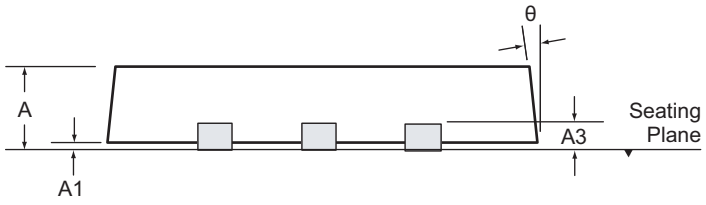
4x4mm body, 1.0mm height (max), 0.80mm pitch



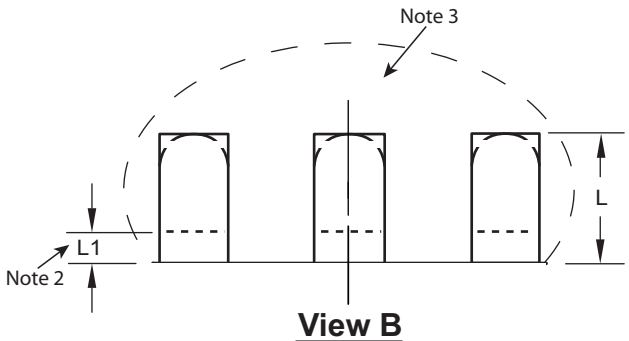
Top View



Bottom View



Side View



View B

Notes:

1. *Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.20	4.00 BSC	2.00	4.00 BSC	2.00	0.80 BSC	0.30	0.03	0°
	NOM	0.90	0.02		0.30		2.15		2.15		-	-	-
	MAX	1.00	0.05		0.35		2.25		2.25		0.50	0.15	14°

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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