2.5 V 184-pin Registered DDR-I SDRAM Modules

256MB, 512MB & 1 GByte Modules

Preliminary Datasheet Rev. 0.9

- 184-pin Registered 8-Byte Dual-In-Line DDR-I SDRAM Module for PC and Server main memory applications
- One bank 32M × 72, 64M x 72 and two bank 64M x 72, 128M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 256Mbit DDR-I SDRAMs in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Jedec standard MO-161 form factor: 133.35 mm × 43.18 mm × 4.00 mm (8.00 mm when stacked)
- Jedec standard reference layout: Rev 0.9 of R/C A, R/C B and RC C
- Gold plated contacts

- Performance:

		-7	-7.5	-8	Unit
	Component Speed Grade	PC266A	PC266B	PC200	
	Module Speed Grade	PC2100	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	143	133	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	100	100	MHz

The HYS 72Dxx000GR are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 32M × 72, 64M × 72 and 128M × 72. The memory array is designed with Double Data Rate Synchronous DRAMs (2.5V DDR-I) for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC266A:			
HYS 72D32000GR-7	PC266AR-20330-A1	one bank 256 MB Reg. DIMM	256 MBit
HYS 72D64000GR-7	PC266AR-20330-B1	one bank 512 MB Reg. DIMM	256 Mbit
HYS 72D64020GR-7	PC266AR-20330-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS 72D128020GR-7	PC266AR-20330-C1	two banks 1 GByte Reg. DIMM	256 MBit (stacked)
PC266B:			
HYS 72D32000GR-7.5	PC266BR-25330-A1	one bank 256 MB Reg. DIMM	256 MBit
HYS 72D64000GR-7.5	PC266BR-25330-B1	one bank 512 MB Reg. DIMM	256 Mbit
HYS 72D64020GR-7.5	PC266BR-25330-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS 72D128020GR-7.5	PC266BR-25330-C1	two banks 1 GByte Reg. DIMM	256 MBit (stacked)
PC200R:			
HYS 72D32000GR-8	PC200R-20220-A1	one bank 256 MB Reg. DIMM	256 MBit
HYS 72D64000GR-8	PC200R-20220-B1	one bank 512 MB Reg. DIMM	256 Mbit
HYS 72D64020GR-8	PC200R-20220-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS 72D128020GR-8	PC200R-20220-C1	two banks 1 GByte Reg. DIMM	256 MBit (stacked)

Note: All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request.
Example: HYS 72D32000GR-8-A, indicating Rev.A die are used for SDRAM components.

Pin Definitions and Functions

A0 - A12	Address Inputs	V_{DD}	Power (+ 2.5 V)
BA0, BA1	Bank Selects	V_{SS}	Ground
DQ0 - DQ63	Data Input/Output	V_{DDQ}	I/O Driver power supply
CB0 - CB7	Check Bits (x72 organization only)	V_{DDID}	VDD Indentification flag
$\overline{RAS}$	Row Address Strobe	V_{DDSPD}	EEPROM power supply
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	SCL	Serial bus clock
CKE0 - CKE1	Clock Enable	SDA	Serial bus data line
DQS0 - DQS8	SDRAM low data strobes	SA0 - SA2	slave address select
CLK, $\overline{CLK}$	Differential Clock Input	WP	Write prodect flag
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes	NC	no connect
$\overline{S0}$ - $\overline{S3}$	Chip Selects	$\overline{RESET}$	Reset pin (forces register inputs low)

Address Format

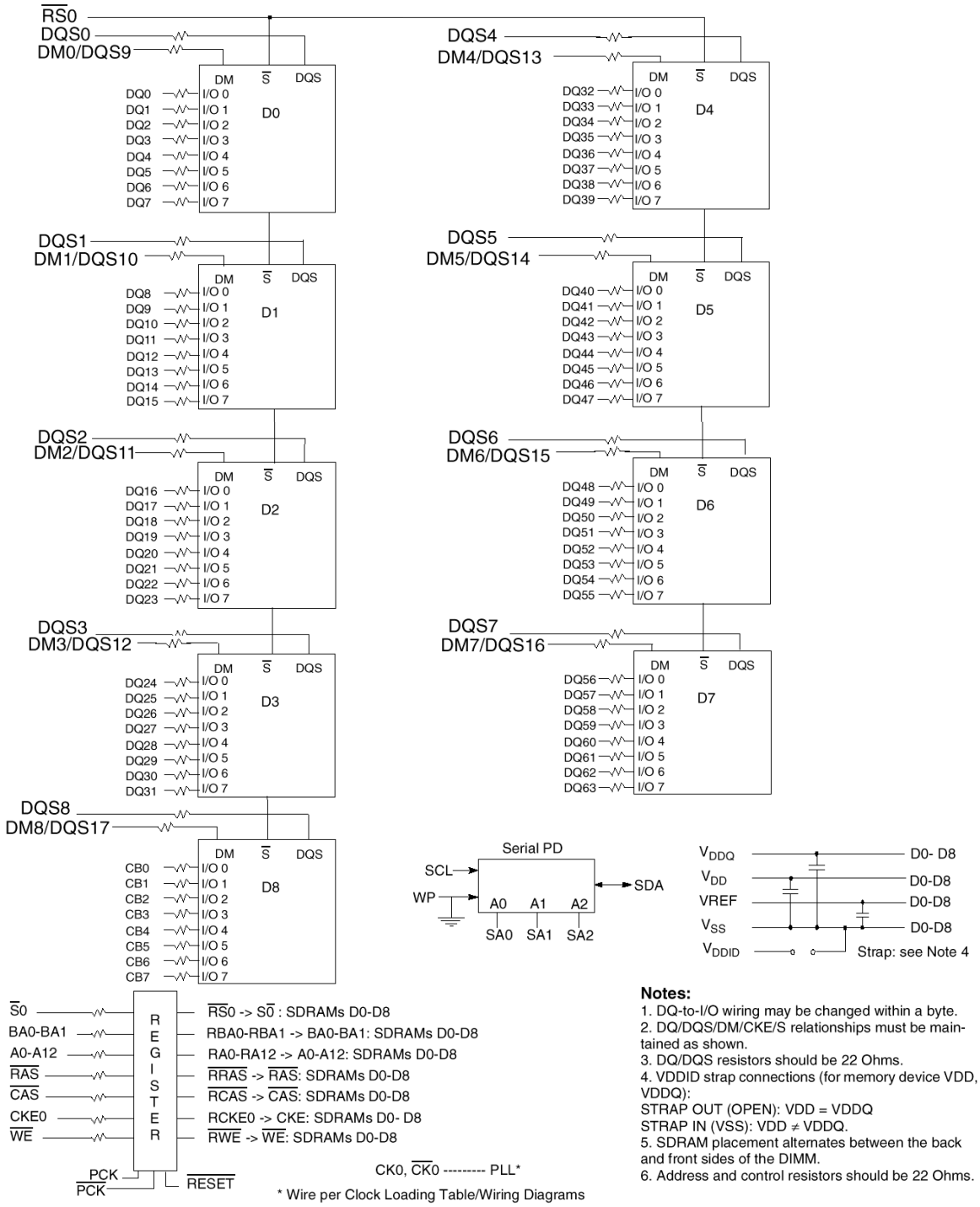
Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	1	64M × 4	18	13/2/11	8k	64 ms	7.8 µs
512 MB	64M x 72	2	32M x 8	18	13/2/10	8k	64 ms	7.8 µs
1 GB	128M × 72	2	64M × 4	36	13/2/11	8k	64 ms	7.8 µs

Pin Configuration

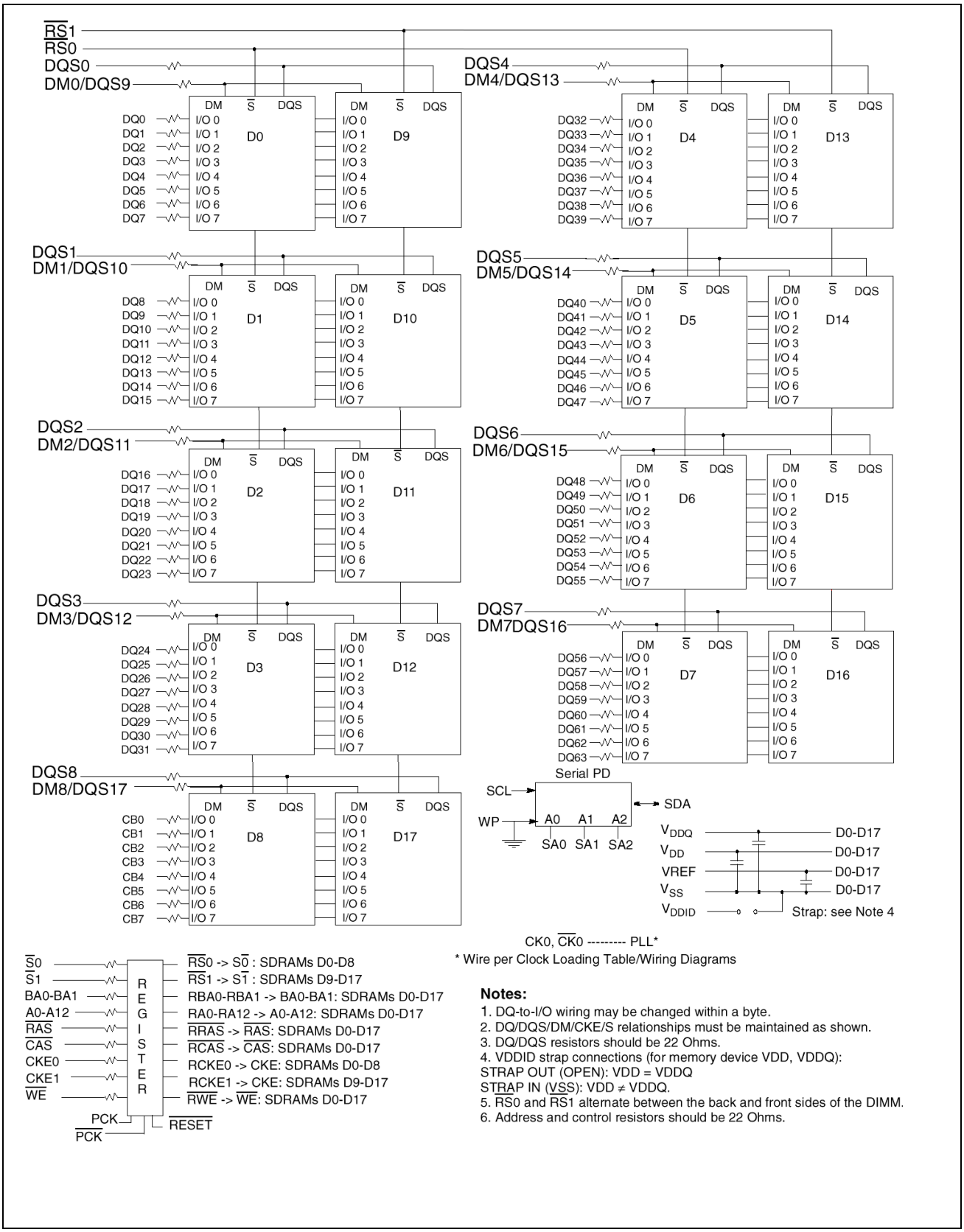
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol		Symbol
1	VREF	48	A0	93	VSS	140	DM8/DQS17
2	DQ0	49	CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	CB6
4	DQ1	51	CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	CB7
6	DQ2	53	DQ32	98	DQ6	145	VSS
7	VDD	54	VDDQ	99	DQ7	146	DQ36
8	DQ3	55	DQ33	100	VSS	147	DQ37
9	NC	56	DQS4	101	NC	148	VDD
10	$\overline{\text{RESET}}$	57	DQ34	102	NC	149	DM4/DQS13
11	VSS	58	VSS	103	A13	150	DQ38
12	DQ8	59	BA0	104	VDDQ	151	DQ39
13	DQ9	60	DQ35	105	DQ12	152	VSS
14	DQS1	61	DQ40	106	DQ13	153	DQ44
15	VDDQ	62	VDDQ	107	DM1/DQS10	154	$\overline{\text{RAS}}$
16	DU (CLK1)	63	$\overline{\text{WE}}$	108	VDD	155	DQ45
17	DU ($\overline{\text{CLK1}}$)	64	DQ41	109	DQ14	156	VDDQ
18	VSS	65	$\overline{\text{CAS}}$	110	DQ15	157	$\overline{\text{S0}}$
19	DQ10	66	VSS	111	CKE1	158	$\overline{\text{S1}}$
20	DQ11	67	DQS5	112	VDDQ	159	DM5/DQS14
21	CKE0	68	DQ42	113	BA2	160	VSS
22	VDDQ	69	DQ43	114	DQ20	161	DQ46
23	DQ16	70	VDD	115	A12	162	DQ47
24	DQ17	71	NC, $\overline{\text{S2}}$	116	VSS	163	NC, $\overline{\text{S3}}$
25	DQS2	72	DQ48	117	DQ21	164	VDDQ
26	VSS	73	DQ49	118	A11	165	DQ52
27	A9	74	VSS	119	DM2/DQS11	166	DQ53
28	DQ18	75	DU (CLK2)	120	VDD	167	NC
29	A7	76	DU ($\overline{\text{CLK2}}$)	121	DQ22	168	VDD
30	VDDQ	77	VDDQ	122	A8	169	DM6/DQS15
31	DQ19	78	DQS6	123	DQ23	170	DQ54
32	A5	79	DQS0	124	VSS	171	DQ55
33	DQ24	80	DQ51	125	A6	172	VDDQ

Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol		Symbol
34	VSS	81	VSS	126	DQ28	173	NC
35	DQ25	82	VDDID	127	DQ29	174	DQ60
36	DQS3	83	DQ56	128	VDDQ	175	DQ61
37	A4	84	DQ57	129	DM3/DQS12	176	VSS
38	VDD	85	VDD	130	A3	177	DM7/DQS16
39	DQ26	86	DQS7	131	DQ30	178	DQ62
40	DQ27	87	DQ58	132	VSS	179	DQ63
41	A2	88	DQ59	133	DQ31	180	VDDQ
42	VSS	89	VSS	134	CB4	181	SA0
43	A1	90	NC	135	CB5	182	SA1
44	NC	91	SDA	136	VDDQ	183	SA2
45	NC	92	SCL	137	CK0	184	VDDSPD
46	VDD			138	$\overline{\text{CK0}}$		
47	NC			139	VSS		



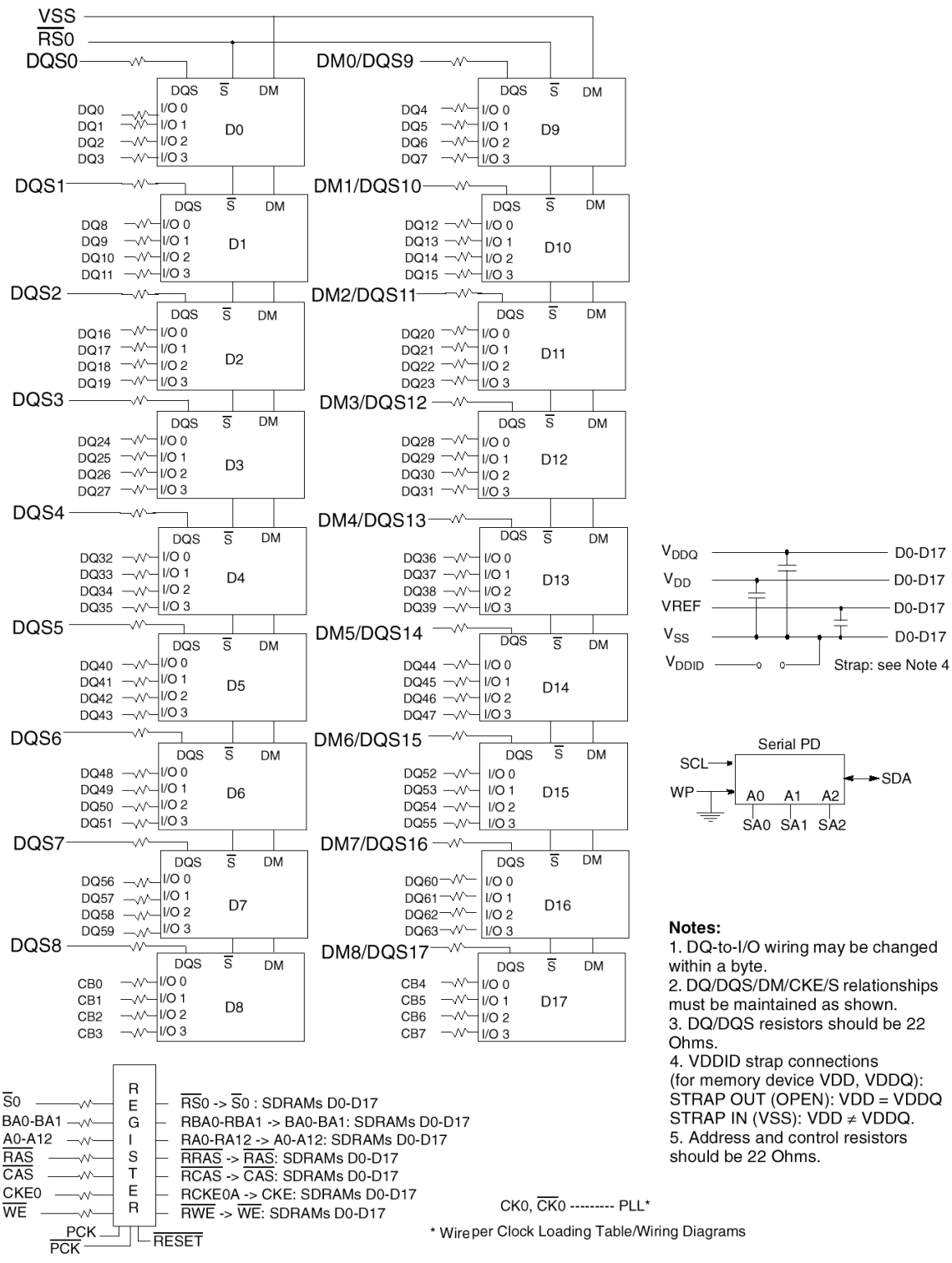
Block Diagram: One Bank 32M × 72 DDR-I SDRAM DIMM Module
HYS72D32000GR using x8 organized SDRAMs on Raw Card Version A



Notes:

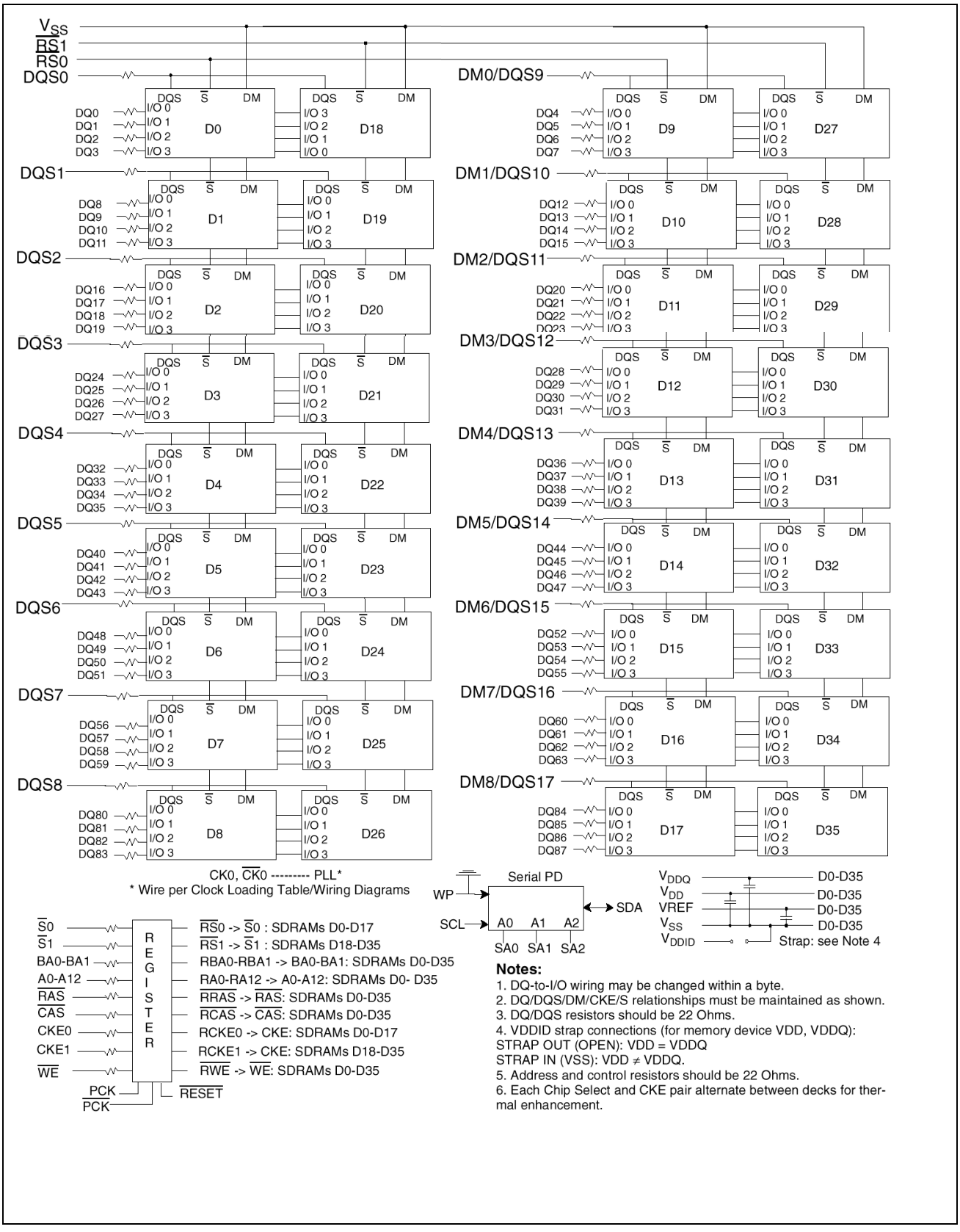
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
   STRAP OUT (OPEN): VDD = VDDQ
   STRAP IN (VSS): VDD ≠ VDDQ.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.

Block Diagram: Two Bank 64M × 72 DDR-I SDRAM DIMM Modules
HYS 72D64020GR Using x8 Organized SDRAMs on Raw Card Version A



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD = VDDQ STRAP IN (VSS): VDD ≠ VDDQ.
5. Address and control resistors should be 22 Ohms.

Block Diagram: One Bank 64M × 72 DDR-I SDRAM DIMM Modules
HYS 72D64000GR Using x8 Organized SDRAMs on Raw Card Version B



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

Block Diagram: Two Bank 128M × 72 DDR-I SDRAM DIMM Modules
HYS 72D128020GR Using x8 Organized SDRAMs on Raw Card Version C

Capacitance (target, not verified)
T_A = 0 to 70 °C; V_{DD} = 2.5 V ± 0.2 V, f = 1 MHz

Parameter	Symbol	Limit Values (max.)		Unit
		One Bank modules	Two Bank Modules	
Input Capacitance (all inputs except CLK,$\overline{\text{CLK}}$ & CKE)	C_{IN}	10	20	pF
Input Capacitance (CLK, $\overline{\text{CLK}}$)	C_{CLK}	30	30	pF
Input Capacitance (CKE)	C_{CKE}	17	30	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	17	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	8	8	pF

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	–
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	1.15	1.25	1.35	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

3) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)
(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.18	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.18	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	2)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V.

Operating, Standby and Refresh Currents (for reference only)
(values apply to one SDRAM component and do not include register and PLL)

(T_A = 0 to +70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter	Symbol	Test Condition	Speed			Unit	Notes
			– 7	– 7.5	– 8		
Operating Current $t_{RC} = t_{RC(min)}$, t_{CK} = min. Active-Precharge command without burst operation	I_{CC1}	1 bank operation $\overline{CS}$ Latency = 2	100	90	70	mA	1), 2), 3)
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ $V_{IL(max)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH(min)}$	20	20	20	mA	1)
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ $V_{IH(min)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH\ (min)}$	50	45	40	mA	1), 3)
No Operating Current (Active state: 4 bank)	I_{CC3P}	CKE ≤ $V_{IL(max)}$, t_{CK} = min.	30	30	30	mA	1)
	I_{CC3N}	CKE ≥ $V_{IH(min)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH\ (min)}$	65	60	55	mA	1), 3)
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min., Read/Write command cycling, Multiple banks active, gapless data, BL = 4	140	120	100	mA	1), 2), 3)
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min., $t_{RC} = t_{RFC(min)}$ CBR command cycling	155	135	110	mA	1), 4), 5)
Self Refresh Current	I_{CC6}	CKE ≤ 0.2 V	1	1	1	mA	1), 4)

1) These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}.
2) The specified values are obtained with the output open.
3) Input signals are changed once during three clock cycles.
4) 8192 refresh cycles in 64 ms.
5) Minimum cycle time during Auto Refresh operation (t_{REF}) is greater than minimum cycle time for Read/Write operation.

AC Characteristics (for reference only)
(values apply to the SDRAM component and do not include register, PLL, or card wiring)

(T_A = 0 to + 70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter		Symbol	-7 PC266A		-7.5 PC266B		-8 PC200		Unit	Notes
			min.	max.	min.	max.	min.	max.		
DQ Output Access Time from CK/$\overline{CK}$		t_{AC}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
DQS Output access Time from CK/$\overline{CK}$		t_{DQSCK}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
CLK High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	*tCK	–
CLK Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	*tCK	–
Clock Period	CL = 2	t_{CK}	7.5	20	10	20	10	20	ns	1)
	CL = 2.5		7	20	7.5	20	8	20	ns	–
	CL = 3		7	20	7.5	20	8	20	ns	–
DQ and DM Input Hold Time		t_{DH}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Setup Time		t_{DS}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Pulse Width (for each input)		t_{DIPW}	1.75	–	1.75	–	2	–	ns	–
Data-Out High-impedance from CK/$\overline{CK}$		t_{HZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
Data-Out Low-impedance from CK/$\overline{CK}$		t_{LZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
DQS-DQ Skew		t_{DQSQ}	–	+ 0.5	–	+ 0.5	–	+ 0.6	ns	–
QH Data-Out Hold Time from DQS		t_{QH}	tHP-0.75	–	tHP-0.75	–	tHP-1.0	–	ns	2)
Write Command to First DQS Latching Transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	*t_{CK}	–
DQS Input Valid Time		$t_{DSL,H}$	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Mode Register/Extended Mode Register Set Cycle Time		t_{MRD}	15	–	15	–	16	–	ns	–
Write Preamble Setup Time		t_{WPRES}	0	–	0	–	0	–	ns	–
DQS Hold Time from CK/$\overline{CK}$		t_{WPREH}	0.25	–	0.25	–	0.25	–	*t_{CK}	–
Write Postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Input Setup Time (LVTTL inputs)		t_{IS}	0.9	–	0.9	–	1.2	–	ns	3)
Input Hold Time (LVTTL inputs)		t_{IH}	0.9	–	0.9	–	1.2	–	ns	3)
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	*t_{CK}	–
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Row Active Time		t_{RAS}	45	120K	45	120k	50	120K	ns	–
Row Cycle Time	R/W Operation	t_{RC}	65	–	65	–	70	–	ns	–
	Auto Refresh	t_{RFC}	75	–	75	–	80	–	ns	1)
$\overline{RAS}$ to $\overline{CAS}$ Delay		t_{RCD}	20	–	20	–	20	–	ns	–
Row Precharge Time		t_{RP}	20	–	20	–	20	–	ns	–
Row Activate to Row Activate Delay		t_{RRD}	15	–	15	–	15	–	ns	–
Write Recovery Time		t_{WR}	15	–	15	–	15	–	ns	–

AC Characteristics (cont'd)(for reference only)
(values apply to the SDRAM component and do not include register, PLL, or card wiring)

(T_A = 0 to + 70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter	Symbol	-7 PC266A		-7.5 PC266B		-8 PC200		Unit	Notes
		min.	max.	min.	max.	min.	max.		
Auto Precharge Write Recovery + Precharge Time	t_{DAL}	35	–	35	–	35	–	ns	–
Internal Write to Read Command Delay	t_{WTR}	1	–	1	–	1	–	*t_{CK}	–
Power Down Entry Time	t_{PDENT}	t_{IS} + 1 CLK	2 CLK + t_{IS}	–	–	t_{IS} + 1 CLK	2 CLK + t_{IS}	ns	–
Power Down Exit Time	t_{PDEX}	t_{IS} + 1 CLK	2 CLK + t_{IS}	–	–	t_{IS} + 1 CLK	2 CLK + t_{IS}	ns	–
Self Refresh Exit Time	t_{SREX}	200	–	200	–	200	–	Cycles	–
Average Periodic Refresh Intercal	t_{REF}	–	7.8	–	7.8	–	7.8	µs	–
CLK Transition Time	t_T	0.5	–	–	–	0.5	–	ns	–

1) Minimum Auto Refresh cycle time is greater than minimum cycle time during normal Read or Write operation.

2) t_{HP} is the lesser of t_{CL} and T_{CH}

3) These parameters guarantee device timing, but they are not necessarily tested on each device
they may be guaranteed by design or tester correlation
t_{IS} / t_{IH} =0.9ns for PC266 are measured with command / address input slew rate of ≥ 1.0V/ns
for command / address input slew rate of ≥ 0.5V/ns and < 1.0V/ns t_{IS} / t_{IH} = 1.0ns should be guaranteed by design
for PC200 t_{IS} / t_{IH} = 1.2ns command / address input slew rate of 1.0V/ns is assumed
slew rate is measured between V_{OH}(AC) and V_{OL}(AC)
CK / CK slew rates are assumed to be ≥ 1.0V/ns
Pulse width for command / address signals to be properly sampled at rising edges of clock shall be a minimum of 2.2ns

Environmental Parameters

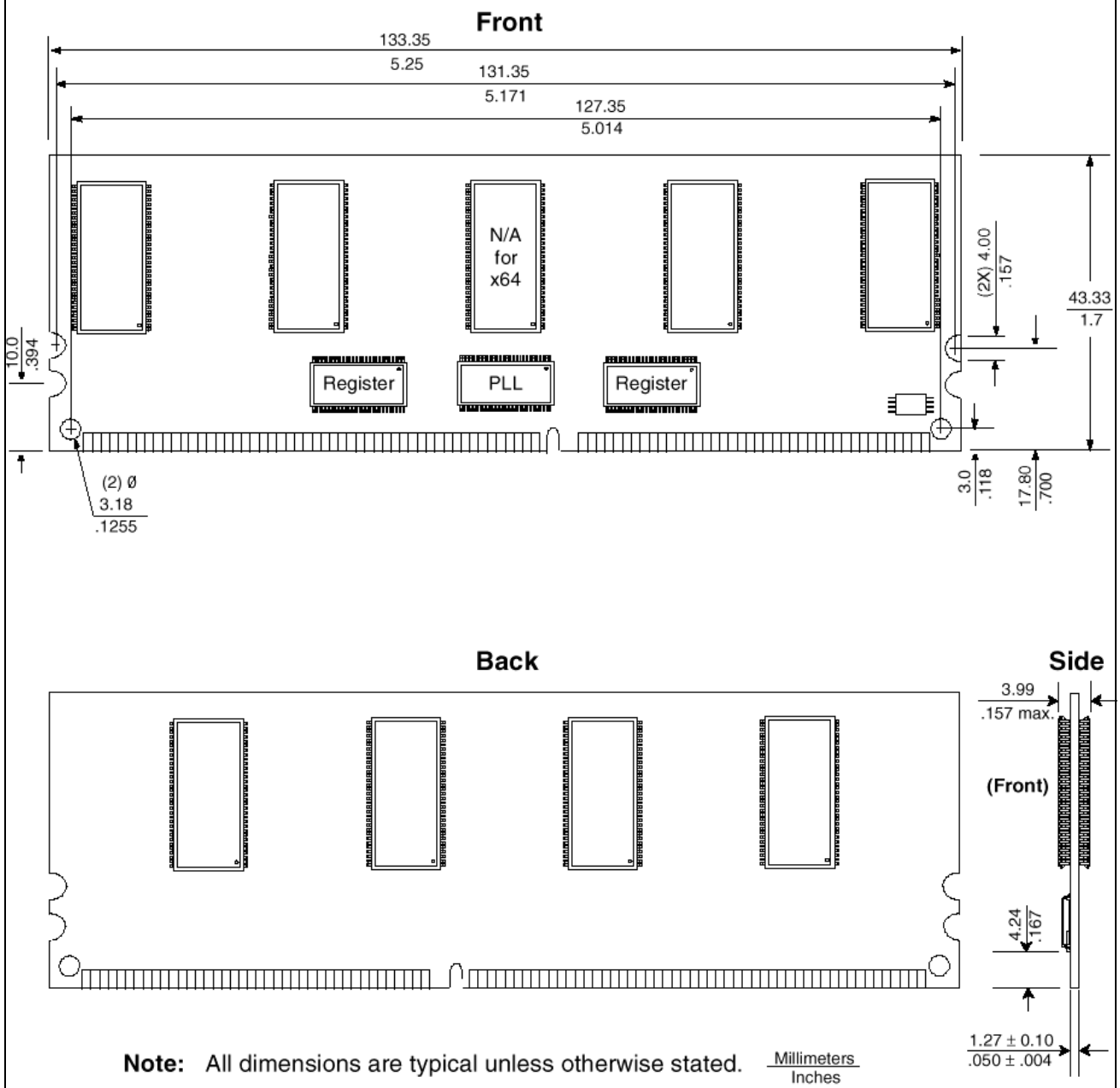
Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1)
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1)
	Barometric Pressure (operating and storage)	105 to 69	K Pascal	2)

1) stresses greater than those listed may cause permanent damage to the device. Device functional operation at or above these conditions is not implied.
2) up to 3000 m (9850 ft)

Package Outlines

Module Package
JEDEC MO-161
DDR-I Registered DIMM Modules Raw Card A

256MByte Modules (one physical bank)

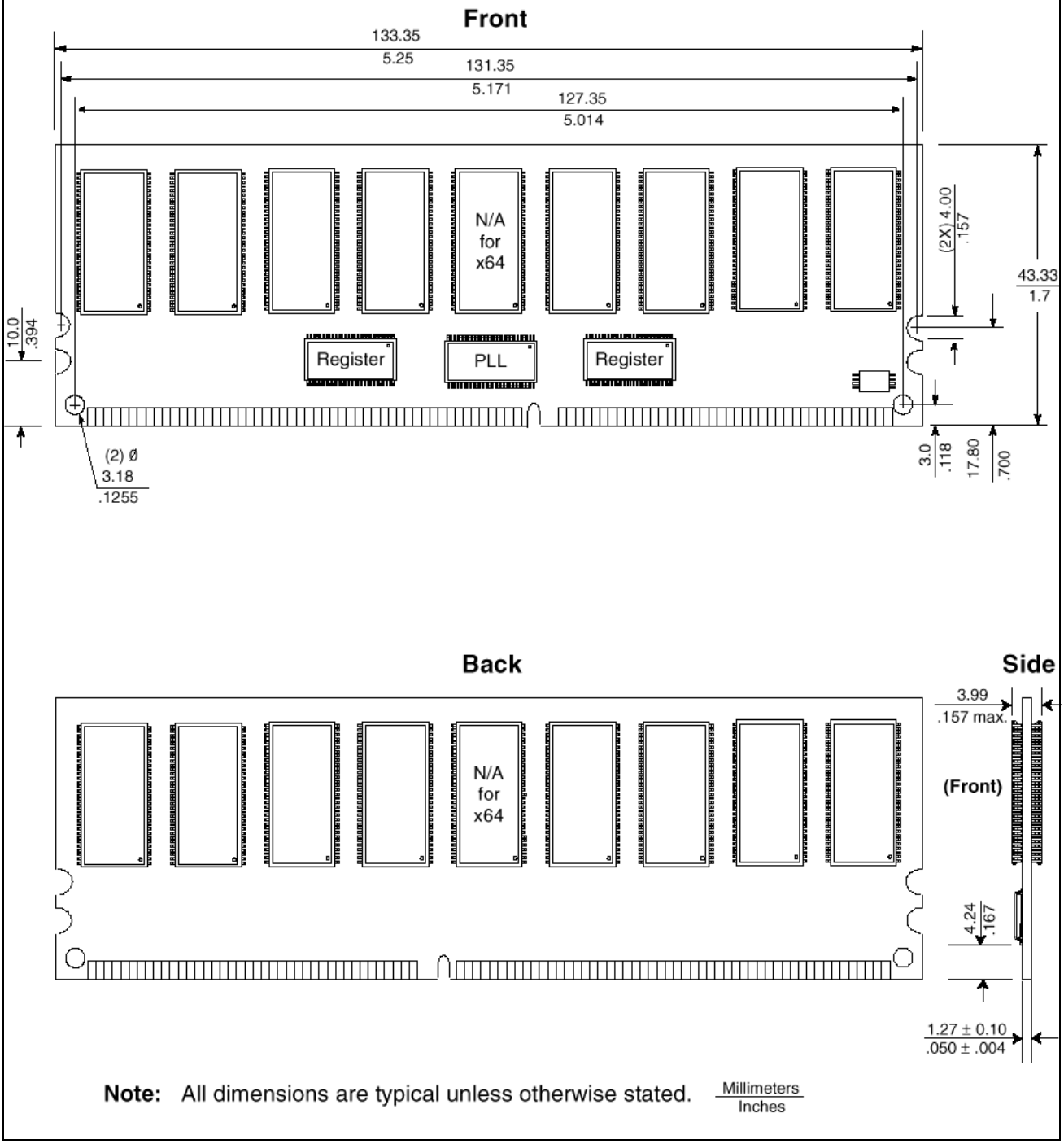


Package Outlines

Module Package

DDR-I Registered DIMM Modules Raw Card A

512MByte Module with two physical banks

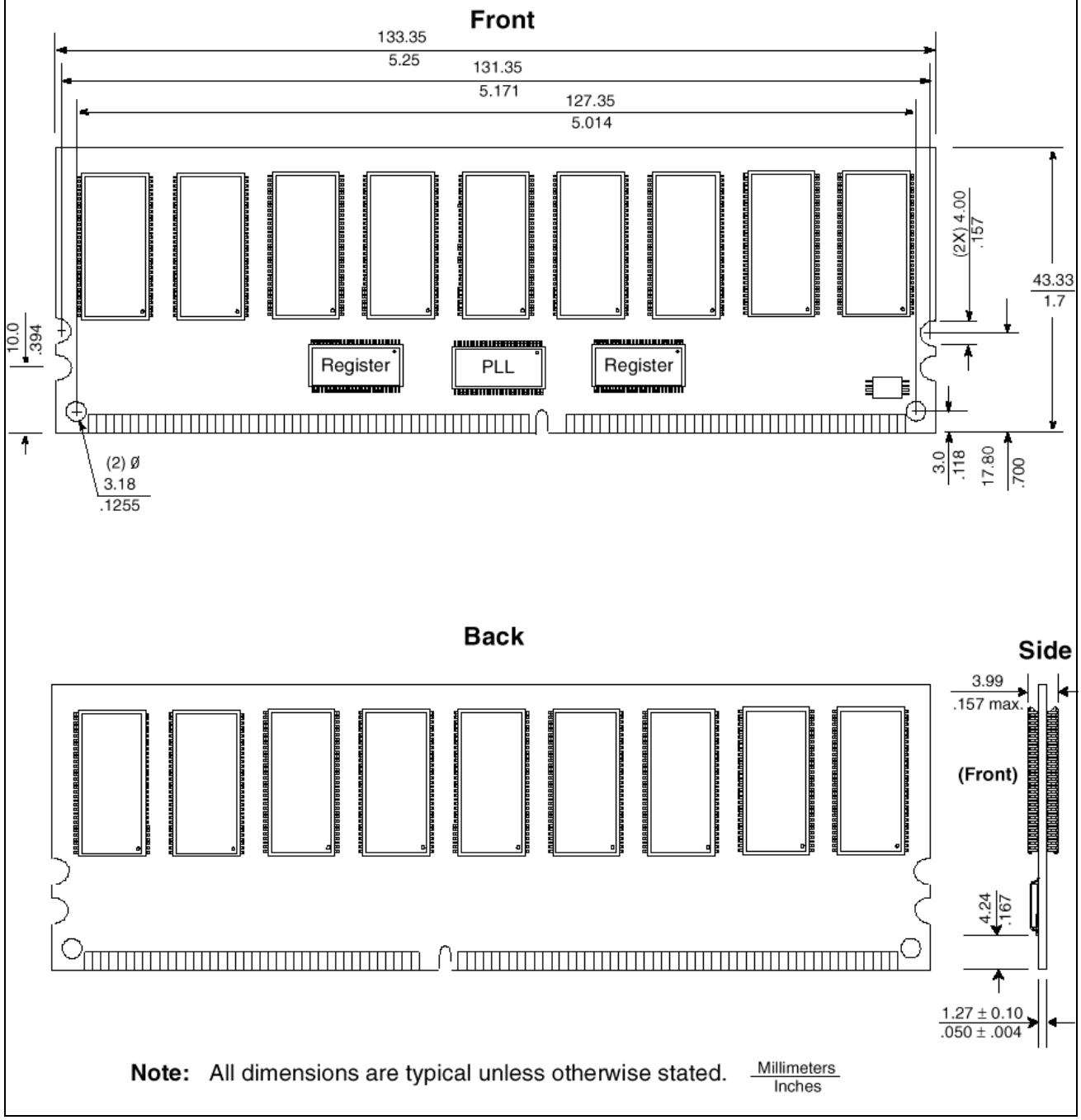


Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Package Outlines

Module Package

DDR-I Registered DIMM Modules Raw Card B
512MByte Module with one physical bank

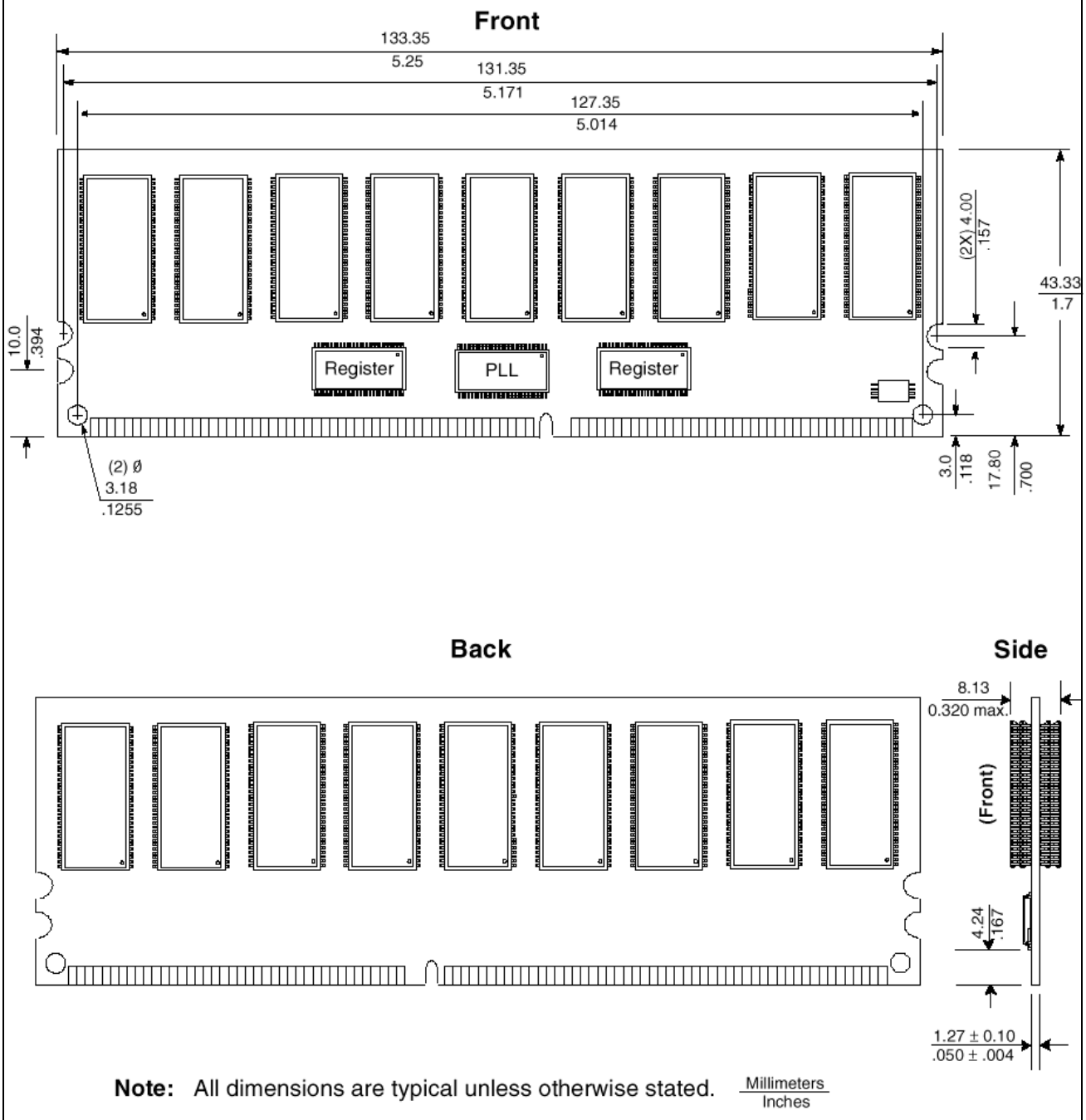


Package Outlines

Module Package

DDR-I Registered DIMM Modules Raw Card C

1 GByte Module with two physical banks



Change List

11.99	Rev.0.2	First target revision 0.2
1.00	Rev.0.3	Rev. 0.3
4.00	Rev.0.9	Rev. 0.9