

# MC10ELT24, MC100ELT24

## 5V TTL to Differential ECL Translator

The MC10ELT/100ELT24 is a TTL to differential ECL translator. Because ECL levels are used a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT24 makes it ideal for those applications where space, performance and low power are at a premium.

The 100 Series contains temperature compensation.

- 0.8 ns TPHL, 0.95 ns TPLH Typical Propagation Delay
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- ESD Protection: > 4 KV HBM, > 200 V MM
- Operating Range:  $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ ;  $V_{EE} = -4.2 \text{ V to } -5.5 \text{ V}$  with  $GND = 0 \text{ V}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 51 devices

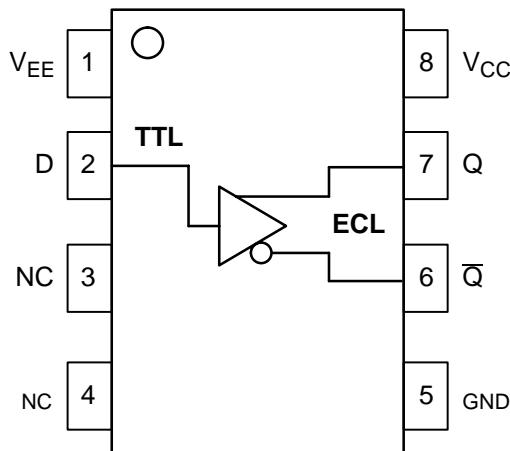


Figure 1. Logic Diagram and Pinout Assignment

### PIN DESCRIPTION

PIN	FUNCTION
Q, $\bar{Q}$	ECL Differential Outputs*
D	TTL Input
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
GND	Ground
NC	No Connect

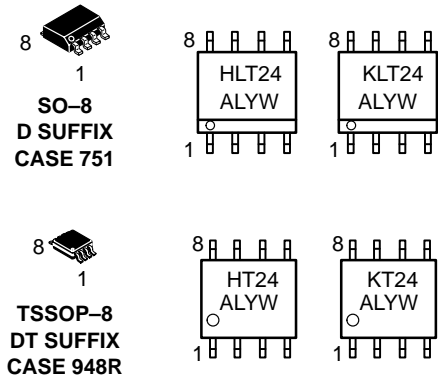
\* Output state undetermined when inputs are open.



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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
K = MC100                    Y = Year  
A = Assembly Location      W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	GND = 0 V	V <sub>EE</sub> = -5.0 V	7	V
V <sub>EE</sub>	Negative Power Supply	GND = 0 V	V <sub>CC</sub> = +5.0 V	-8	V
V <sub>IN</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to V <sub>CC</sub>	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## 10ELT SERIES NECL DC CHARACTERISTICS V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = -5.0 V; GND = 0 V (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>CC</sub>	V <sub>CC</sub> Power Supply Current			7.0		4.5	7.0			7.0	mA
I <sub>EE</sub>	Power Supply Current			18		12.5	18			18	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

2. Output parameters vary 1:1 with GND. V<sub>EE</sub> can vary +0.06 V / -0.5 V.

3. Outputs are terminated through a 50 Ω resistor to GND-2 volts.

## 100ELT SERIES NECL DC CHARACTERISTICS V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = -5.0 V; GND = 0 V (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>CC</sub>	V <sub>CC</sub> Power Supply Current			7.0		4.5	7.0			7.0	mA
I <sub>EE</sub>	Power Supply Current			18		12.5	18			18	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 5)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 5)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

4. Output parameters vary 1:1 with GND. V<sub>EE</sub> can vary +0.8 V / -0.5 V.

5. Outputs are terminated through a 50 Ω resistor to GND-2 volts.

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## TTL INPUT DC CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ; $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

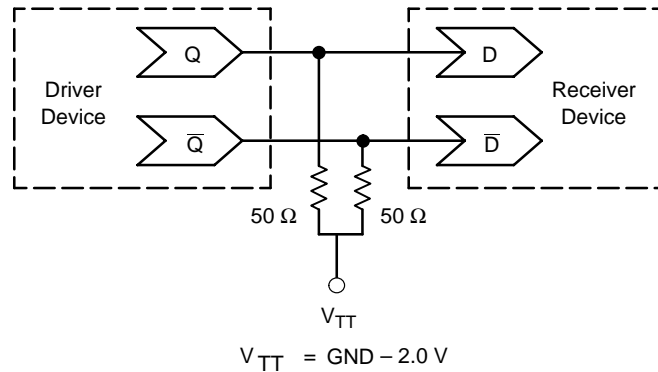
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current	$V_{IN} = 7.0\text{ V}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	$\text{mA}$
$V_{IK}$	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	V
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V

## AC CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ ; $\text{GND} = 0.0\text{ V}$ (Note 6)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{max}}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{\text{PLH}}$	Propagation Delay (Note 7) 1.5 V to 50%	0.7		1.3	0.65	0.95	1.25	0.65		1.25	ns
$t_{\text{PHL}}$	Propagation Delay (Note 7) 1.5 V to 50%	0.4		1.0	0.50	0.80	1.10	0.70		1.30	ns
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r/t_f$	Output Rise/Fall Time (20–80%)	0.25		1.25	0.25		1.25	0.25		1.25	ns

6.  $V_{EE}$  can vary  $+0.06\text{ V} / -0.5\text{ V}$  for 10ELT;  $V_{EE}$  can vary  $+0.8\text{ V} / -0.5\text{ V}$  for 100ELT.

7. Specifications for standard TTL input signal.



**Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

## MC10ELT24, MC100ELT24

### ORDERING INFORMATION

Device	Package Type	Shipping
MC10ELT24D	SO-8	98 Units/Rail
MC10ELT24DR2	SO-8	2500 Tape & Reel
MC100ELT24D	SO-8	98 Units/Rail
MC100ELT24DR2	SO-8	2500 Tape & Reel
MC10ELT24DT	TSSOP-8	98 Units/Rail
MC10ELT24DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT24DT	TSSOP-8	98 Units/Rail
MC100ELT24DTR2	TSSOP-8	2500 Tape & Reel

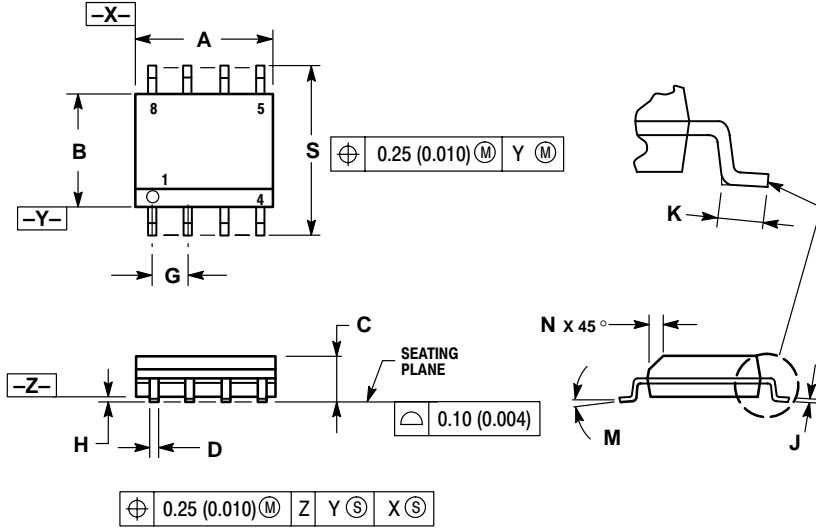
### Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10ELT24, MC100ELT24

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-07  
ISSUE W



### NOTES:

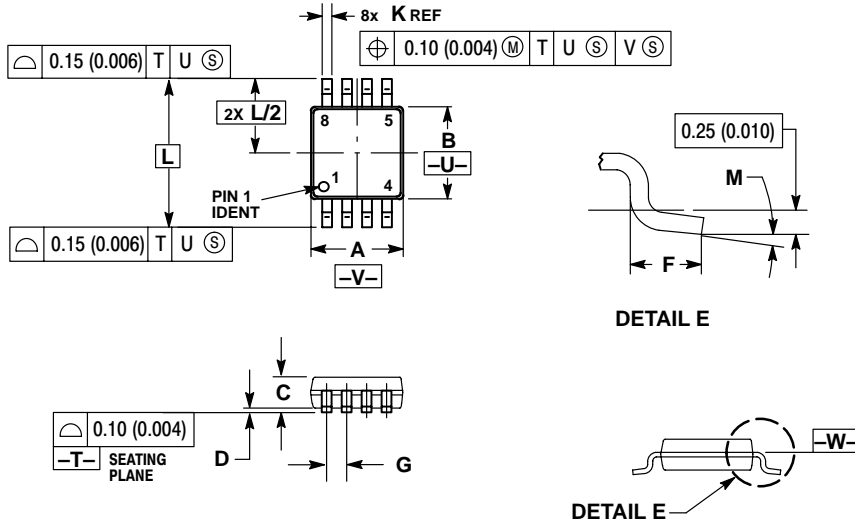
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0° 8°		0° 8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

# MC10ELT24, MC100ELT24

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

## Notes

## MC10ELT24, MC100ELT24

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