1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS dual 12-bit DACPORTs™, each consisting of two 12-bit DACs, output amplifiers and reference. The AD7237A has an (8+4) microprocessor loading structure, while the AD7247A has a parallel loading structure.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7237ATQ/883B, AD7247ATQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
Q-24	24-Pin Cerdip, 0.3" Width

(For volume applications, the AD7237A and AD7247A are available in the LCC package. Contact your local Analog Devices Sales Office.)

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to GND (AD7247A) ..... +0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237A) ..... −0.3 V to +17 V
V_{DD} to V_{SS} ..... −0.3 V to +34 V
AGND to DGND (AD7237A) ..... +0.3 V, V_{DD} +0.3 V
V_{OUTA},[1] V_{OUTB}[1] to AGND (GND) ..... V_{SS} −0.3 V to V_{DD} +0.3 V
REFOUT[1] to AGND (GND) ..... 0 V to V_{DD}
REFIN to AGND (GND) ..... −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) ..... −0.3 V to V_{DD} +0.3 V
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 1000 mW
Derates above +75°C by ..... 10 mW/°C

NOTE
[1]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

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Table 1.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1]	Unit
Resolution	RES	−1		12	1, 2, 3		Bits
Relative Accuracy	RA	−1	−0.5	+0:5	1, 2, 3		LSB
Differential Nonlinearity	DNL	−1	−0.9	+0.9	1, 2, 3	Guaranteed Monotonic	LSB
Unipolar Offset Error	OFS	−1	−3	+3	1, 2, 3	V_{SS} = 0 V or −15 V. DAC Latch Contents All Zeroes	LSB
Bipolar Zero Error	Z_E	−1	−6	+6	1, 2, 3	V_{SS} = −15 V. DAC Latch Contents 1000 0000 0000	LSB
Full-Scale Error[2]	A_E	−1	−6	+6	1, 2, 3		LSB
Reference Output	REF OUT	−1	4.95	5.05	1, 2, 3		V
Reference Load Change	△REF	−1		−1	1, 2, 3	△REFOUT vs. △ I Reference Load Current Change (0–100 mA)	mV
Reference Input Range	REFIN	−1	4.75	5.25	1, 2, 3		V
Input Current	I_{IN}	−1	−5	+5	13, 14, 15		μA
Digital Input High Voltage	V_{INH}	−1	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	−1		0.8	1, 2, 3		V
Digital Input Current[3]	I_{IN}	−1	−10	+10	1, 2, 3	Data Inputs; V_{IN} = 0 V to V_{DD}	μA
	I_{INH}		−10	+10		Control Inputs; V_{IN} = V_{DD}	
	I_{INL}			−150		Control Inputs; V_{IN} = 0 V	
Input Capacitance	C_{IN}	−1		16	13, 14, 15		pF
Output Range Resistors		−1	15	30	1, 2, 3		kΩ
Output Voltage Ranges		−1	+5	+10	1, 2, 3	V_{SS} = 0 V; Pin Strappable	V
Output Voltage Ranges		−1	+5, +10, ±5		1, 2, 3	V_{SS} = −12 V to −15 V; Pin Strappable	V
Voltage Output Settling Time Full-Scale Change	t_{SL}	−1		12	13, 14, 15	V_{DD} = +15 V, V_{SS} = 0 or −12 V to −15 V Settling to ±1/2 LSB	μs
Power Supply Current	I_{DD}	−1		15	1, 2, 3	Outputs Unloaded	mA
	I_{SS}	−1		5	1, 2, 3	Outputs Unloaded (Dual Supplies)	mA
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	−1	0		9, 10, 11	See Note 4	ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	−1	0		9, 10, 11		ns
$\overline{WR}$ Pulse Width	t_3	−1	100		9, 10, 11		ns
Data Valid to Write Setup Time	t_4	−1	80		9, 10, 11		ns
Data Valid to Write Hold Time	t_5	−1	10		9, 10, 11		ns
Address to Write Setup Time	t_6[5]	−1	0		9, 10, 11		ns
Address to Write Hold Time	t_7[5]	−1	0		9, 10, 11		ns
$\overline{LDAC}$ Pulse Width	t_8[5]	−1	100		9, 10, 11		ns

NOTES

[1]V_{DD} = 12 V to 15 V, V_{SS} = 0 V or − 12 V to −15 V; AGND = DGND = 0 V (AD7237A), GND = 0 V (AD7247A); R_L = 2 kΩ, C_L = 100 pF. Subgroups 10, 11, 13, 14, 15 are characterized at initial design are after any design changes and are not production tested.

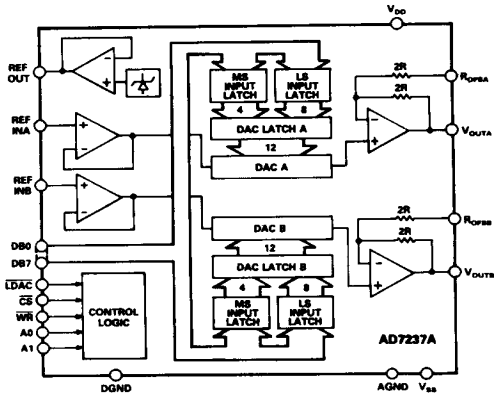
[2]Measured with respect to REFIN and includes unipolar/bipolar offset error.

[3]Control inputs are A0, A1, CS, WR and LDAC for the AD7237A and CSA, CSB and WR for the AD7247A.

[4]All input signals are specified with t_R = t_F = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

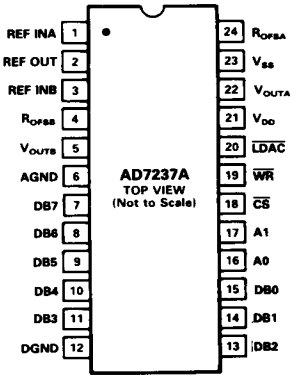
[5]Applies to AD7237A only.

3.2.1 Functional Block Diagram and Terminal Assignments.

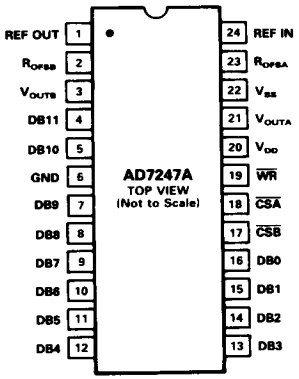


Pin Assignments

DIP



DIP



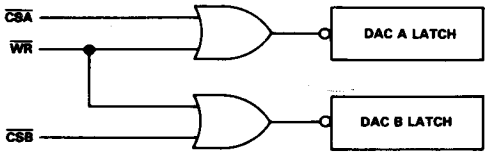


Figure 1. Input Control Logic AD7247A

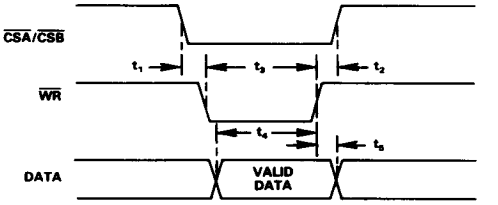


Figure 2. Timing Diagram AD7247A

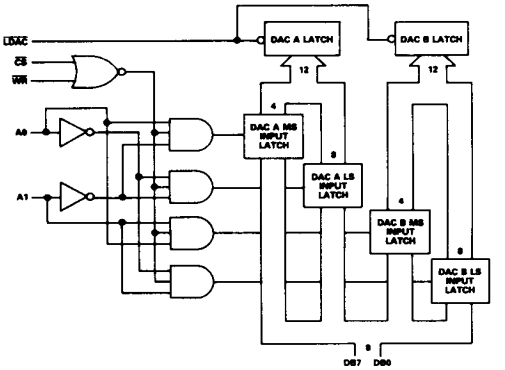


Figure 3. Input Control Logic AD7237A

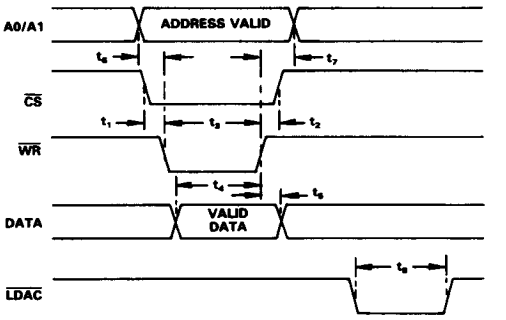


Figure 4. Timing Diagram AD7237A

Table 2. AD7247A Truth Table

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X=Don't Care

Table 3. AD7237A Truth Table

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

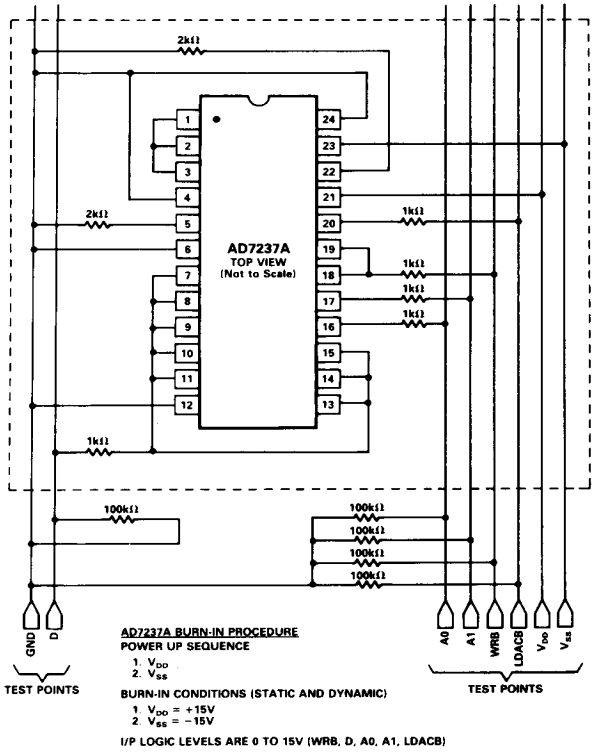
X = Don't Care.

3.2.4 Microcircuit Technology Group.

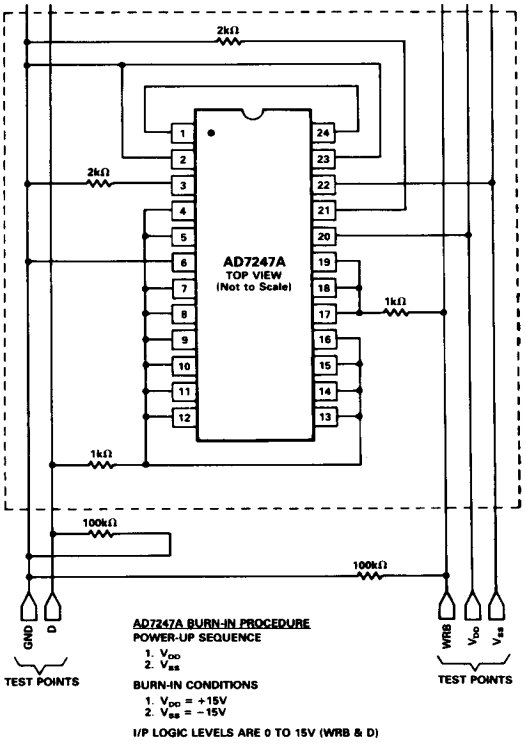
This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7237A Burn-In Diagram



AD7247A Burn-In Diagram