INTERNATIONAL RECTIFIER 26E D ■ 4855452 0010266 7 ■ T-39-90 T-01-05 T-03-05

IGBTs, HEXFET, HEXSENSE and LOGIC LEVEL HEXFET DIE

International Rectifier now support Die and Wafer sales from their European Headquarters at Oxted, England.

COMMERCIAL CHIPS

It is possible to buy any of the IGBT, HEXSense and Logic Level products in die form, for your own custom and hybrid applications. If you are a larger user with needs in excess of 100,000 die per annum then it may be worthwhile discussing the use of wafers instead of the discrete components in waffle packs. Whatever your needs, contact your local Sales Office who will be happy to advise you regarding technical details, pricing and delivery.

INSULATED GATE BIPOLAR TRANSISTORS — IGBTs

International Rectifier can now offer it's new range of Insulated Gate Bipolar Transistors (IGBTs) in chip form. The IGBT combines the best features of Power MOSFETs and Bipolar Transistors. The ease of drive and rugged operation of HEXFETs, coupled with the low forward voltage drop of Bipolar Devices, results in an optimum solution for low to medium frequency power converters up to 20kHz.

IRFCXX '-883, '-ESA, '-LAT and '-VIS MILITARY CHIPS

For users who require more than just commercial components International Rectifier can offer four levels of High-Rel screening on chips. "VIS" provides a 100% visual inspection to Mil-Std 750C method 2072, "LAT" additionally gives a sample from each wafer lot a series of accelerated life test to establish diffusion stability. "ESA" provides screening to the recognised ESA/SCC 20450 specification section 4A. "883" provides screening according to MIL-S-833 method 5008 level B. For more details, request a copy of our Controlling Specification E2931 from your Local Sales Office.

HEXFET GENERATION III

The evolution of the HEXFET has given rise to three HEXFET types, each based on a distinct die design philosophy. The HEXFET III process, detailed in Application Note AN-964, is distinguished by increased and specialised avalanche capability, a high diode-recovery dv/dt rating, an increase in maximum allowable die temperature for devices of 100V and below, and a number of other significant technological advances.

N-channel : All die supplied are now Generation III.

P-channel : 60V and 100V die are Generation III. The 200V die continue to be supplied as Generation I.

As with Generation I and II die the Generation III die are all glass passivated over the active areas with a "Silox" Phosphor/Silicon Dioxide, compound providing mechanical protection and a degree of hermeticity.

THE APPLICATION AND CUSTOM ASSEMBLY OF HEXFET DICE

(FROM APPLICATION NOTES AN931 AND AN964)

INTRODUCTION

This document describes the HEXFET transistors available from International Rectifier in die form. These power MOS field effect transistor dice feature the same high reliability DMOS technology used for the IRF series of packaged HEXFETS. The same advanced MOS processing techniques, silicon gate structure, and efficient hexagonal source pattern are available in die form for hybrid assembly. Use of silicon-gate design and state of the art MOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes. Hybrid packaging of such die results in substantial savings in weight and volume compared to standard packaging.

HEXFET GENERATION I

Only 200V P-channel product continues to be available in Generation I.

HEXFET GENERATION III

HEXFET Generation III are ruggedised and have better silicon utilisation than the other two processes. The HEXFET Generation III process devices are upwardly compatible with the corresponding HEXFET Generation I and II process components. Low voltage, Generation III components will have a Vds of 60V instead of 50V.

The HEXFET Generation III process is distinguished by increased avalanche capability, a much higher diode dv/dt rating, an increase in maximum allowable die temperature of 175°C for devices of 100V and below, and a number of other significant technological advances. Full details of these improvements are given in Application Note AN964.

HEXSense

International Rectifier has introduced a new family of HEXFETs incorporating Current Sensing. This is the HEXSense range of devices. Current Sensing is achieved by isolating a few of the HEXFET cells from the main source metallisation and providing them with a separate bonding pad. The drain current divides between the sense cells and the main body of cells in a manner determined by the ratio of the number of sense cells to the total number of cells on the die. This ratio being known, the drain current can be determined measuring only the sense current. Since the sense current is of the order of a few milliamps the value of the drain current can be determined without incurring significant power losses.

The HEXSense die has two extra bonding pads, besides the gate and source pads. These are the Current-sense pad and the Kelvin-source pad. The current-sense pad connects to the sensing cells. The Kelvin-source pad connects to the main source metallisation and is used as a return path for the sense current. A separate return path for this current is required to prevent voltage drops owing to parasitic resistance in the main source path being included in the sense current path.

Details of the HEXSense range are given in Table 3 and the die dimensions are included in figures 34 to 38.

ELECTRICAL CHARACTERISTICS

Each HEXFET die is individually probed at room ambient temperature to the electrical specifications shown in Tables 1, 2, 3, 4 and 5.

Because of limitations when electrically probing in wafer form, some of the generic specifications of the equivalent packaged devices cannot be tested and guaranteed in die form.

These are Power Dissipation P_D, Safe Operating area SOA, Thermal Resistance $R_{TH(J-C)}$, On-Resistance at rated current

$R_{DS(ON)}$, and Inductive Current I_L and sense ratio r. On-Resistance at I_D = 1A is tested and guaranteed according to Tables 1, 2, 3 and 4.

These above parameters are dependent upon the user's assembly technique. However, the following characteristics are guaranteed by design to meet the specifications of the equivalent part: gfs, C_{iss}, C_{oss}, C_{rss}, and $T_{j(max)}$ for HEXFET Generation I; gfs, Qg, Qgs, Qgd, dv/dt and $T_{j(max)}$ for HEXFET Generation III devices. Consult the appropriate data sheet listed in Tables 1 through 4.

Following electrical probing, the dice are inked for identification and scribed. The dice are mechanically separated visually inspected then waffle packed for shipment.

The relative cell densities of the different generation HEXFET are as follows:

GEN I 500,000 cells/in² (100V-500V)
GEN II 800,000 cells/in² (60V-100V)
GEN III 500,000 cells/in² (100V-600V)

HANDLING AND SHIPPING

HEXFET dice from International Rectifier are shipped in anti-static chip trays and sealed in electrostatic shielding bags for protection during shipment. Once opened, the dice must be stored in a dry, inert atmosphere such as nitrogen prior to assembly. Dice should be handled with DuPont Teflon-tipped vacuum pencils to prevent mechanical damage. Any non-conformance to the electrical or visual inspection specifictions in this guide must be reported in writing to International Rectifier within 30 days of shipment of the lot by International Rectifier. International Rectifier assumes no responsibilities for die which have been subjected to further processing such as mountdown, wire bonding, or encapsulation. In the interest of product improvement, the right is reserved to make design or processing changes without notification.

The anti-static chip trays are designed to avoid the build-up of static charge. International Rectifier HEXFETs have large gate capacitances and thick oxide layers relative to low level MOS devices. Though significantly more rugged than such low level devices, reasonable precautions should be observed during handling and assembly to prevent exceeding the 20V specified maximum gate-source voltage.

VISUAL INSPECTION OF DIE

International Rectifier HEXFET die are designed to be capable of meeting the visual inspection criteria of Mil-Standard 750C, Method 2072. HEXFET dice are visually screened to a 1.0% AQL level prior to shipment. 100% screening can be obtained by specifying -VIS or higher level testing.

DIE MOUNTING

The HEXFET dice have chromium-nickel-silver drain metallisation which is suitable for solder preform mounting using solders such as 95/5 PbSn or 92.5/2.5/5 Pb/Ag/In solder.

Gold backing can be made available as an alternative; please contact the factory or your IR Representative for more information.

Any of the commonly used header or substrate materials such as copper, nickel-plated copper, and gold plated molybdenum, beryllia, and alumina are acceptable to mount HEXFET die onto. The substrate must be freed of oxides prior to assembly either by chemical cleaning or H_2 pre-firing techniques.

The HEXFET dice should be cleaned prior to mountdown in deionised water cascade (one minute) followed by isopropl alcohol agitated bath (twice, one minute each) and then dried in a Nitrogen filled chamber at between 70°C and 125°C. Mounting is generally accomplished in a profiled belt furnace. The furnace zone settings will depend upon hybrid mass density, jigging and belt speed. The HEXFET die temperature must not exceed 400°C, nor be in the range of 350°C to 400°C for greater than one minute. A clean furnace of hydrogen atmosphere is recommended, although nitrogen atmosphere or forming gas (nitrogen-hydrogen 85%-15%) is acceptable.

A variety of conductive plastics have been utilised as alternative means of bonding the HEXFET dice to a variety of substrates.

WIRE BONDING

For electrical connection to the gate and source aluminium bonding pads ultrasonic wire-bonding with Al wire is recommended. The maximum recommended wire diameters are given in Tables 1 to 5 of this shortform. Caution must be exercised during wire bonding to ensure that the bonding footprint remains within the bonding pad area. Likewise, wire bond equipment settings should be optimised and a wire pull test performed (e.g. Method 2037, Mil-Standard 750C) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Rebonding on wire bond rejects can be performed although decreased yield can be expected from such reworks. Using process controls as described above, final assembly yields of 80% to 95% can be achieved.

ENCAPSULATION

Prior to encapsulation, the die assembly must be kept in a moisture-free environment, as I_{GSS} and I_{DSS} particularly are sensitive to surface moisture. If the final package is non-hermetic, a high grade electronic coating such as Dow Corning RTV3140 or equivalent may be applied. If the package is hermetic, the coating is optional. Cleaning of the die in a freon vapour degreaser prior to coating is recommended.

T-01-05

Immediately prior to encapsulation, a 150°C, two hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry nitrogen atmosphere.

T-03-05

CONCLUSION

The use of power MOSFET dice for hybrid assemblies can result in significant reduction in overall package size. In addition, the high gain characteristics of the HEXFET can allow further miniaturisation by eliminating complex drive circuitry. Several HEXFET dice can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The HEXFET operational advantages, thereby, can be realised in very compact, custom package configurations.

TABLE 1: ELECTRICAL PROBE SPECIFICATIONS FOR N-CHANNEL HEXFET POWER MOSFET DIE

HEX size	Part Number	V_{DS} V	$R_{DS(on)}$ Ω	Figure	Recommended Bond Wire Size Source in/mm	Recommended Bond Wire Size Gate in/mm	Closest Part Number	Bulletin
Z	IRFC1Z0R	100	3.200	1	0.005/0.127	0.005/0.127	IRFS1Z0	PD-9.438
1	IRFC014R	60	0.200	2	0.005/0.127	0.005/0.127	IRFZ14	PD-9.507
	IRFC110R	100	0.540	3	0.005/0.127	0.005/0.127	IRF510	PD-9.325
	IRFC210R	200	1.500	4	0.005/0.127	0.005/0.127	IRF610	PD-9.326
	IRFC214R	250	2.000	4	0.005/0.127	0.005/0.127	IRF614	PD-9.475
	IRFC310R	400	3.600	5	0.005/0.127	0.005/0.127	IRF710	PD-9.327
2	IRFC024R	60	0.100	6	0.008/0.203	0.005/0.127	IRFZ24	PD-9.058
	IRFC120R	100	0.270	7	0.008/0.203	0.005/0.127	IRF520	PD-9.313
	IRFC220R	200	0.800	8	0.008/0.203	0.005/0.127	IRF620	PD-9.317
	IRFC224R	250	1.100	8	0.008/0.203	0.005/0.127	IRF624	PD-9.472
	IRFC320R	400	1.800	9	0.008/0.203	0.005/0.127	IRF720	PD-9.315
	IRFC420R	500	3.000	9	0.008/0.203	0.005/0.127	IRF820	PD-9.324
	IRFCC20R	600	4.400	9	0.008/0.203	0.005/0.127	IRFBC20	—
3	IRFC034R	60	0.050	10	0.010/0.254	0.005/0.127	IRFZ34	PD-9.509
	IRFC130R	100	0.160	11	0.010/0.254	0.005/0.127	IRF530	PD-9.307
	IRFC234R	200	0.400	12	0.008/0.203	0.005/0.127	IRF630	PD-9.309
	IRFC234R	250	0.450	12	0.008/0.203	0.005/0.127	IRF634	PD-9.476
	IRFC330R	400	1.000	13	0.008/0.203	0.005/0.127	IRF730	PD-9.308
	IRFC430R	500	1.500	13	0.008/0.203	0.005/0.127	IRF830	PD-9.311
	IRFCC30R	600	2.200	13	0.008/0.203	0.005/0.127	IRFBC30	PD-9.482
4	IRFC044R *	60	0.028	14	0.015/0.381	0.005/0.127	IRFZ44	PD-9.510
	IRFC140R *	100	0.077	15	0.015/0.381	0.005/0.127	IRF540	PD-9.373
	IRFC240R *	200	0.180	16	0.012/0.305	0.005/0.127	IRF640	PD-9.374
	IRFC244R *	250	0.280	16	0.012/0.305	0.005/0.127	IRF644	PD-9.527
	IRFC340R *	400	0.550	17	0.012/0.305	0.005/0.127	IRF740	PD-9.375
	IRFC440R *	500	0.850	17	0.012/0.305	0.005/0.127	IRF840	PD-9.376
	IRFC448R *	500	0.600	18	0.012/0.305	0.005/0.127	IRFP448	PD-9.376
	IRFCC40R *	600	1.200	17	0.012/0.305	0.005/0.127	IRFBC40	PD-9.506
5	IRFC054R *	60	0.020	18	0.020/0.508	0.005/0.127	IRFP054	PD-9.544
	IRFC150R *	100	0.055	19	0.020/0.508	0.005/0.127	IRFP150	PD-9.411
	IRFC250R *	200	0.085	20	0.012/0.305	0.005/0.127	IRFP250	PD-9.443
	IRFC254R *	250	0.140	20	0.012/0.305	0.005/0.127	IRFP254	PD-9.540
	IRFC350R *	400	0.300	21	0.012/0.305	0.005/0.127	IRFP350	PD-9.445
	IRFC450R *	500	0.400	21	0.012/0.305	0.005/0.127	IRFP450	PD-9.458
	IRFCC50R *	600	0.580	21	0.012/0.305	0.005/0.127	IRFPC50	—
6	IRFC260R *	200	0.070	22	0.015/0.381	0.005/0.127	IRFP260	—
	IRFC360R *	400	0.200	22	0.015/0.381	0.005/0.127	IRFP360	PD-9.518
	IRFC460R *	500	0.270	22	0.015/0.381	0.005/0.127	IRFP460	PD-9.465

TABLE 2: ELECTRICAL PROBE SPECIFICATIONS FOR P-CHANNEL HEXFET POWER MOSFET DIE

HEX size	Part Number	V_{DS} V	$R_{DS(on)}$ Ω	Figure	Recommended Bond Wire Size Source in/mm	Recommended Bond Wire Size Gate in/mm	Closest Part Number	Bulletin
1	IRFC9014R	−60	0.500	23	0.004/0.102	0.004/0.102	IRF9Z14	—
	IRFC9110R	−100	1.200	24	0.004/0.102	0.004/0.102	IRF9510	PD-9.390
	IRFC9210	−200	3.000	25	0.004/0.102	0.004/0.102	IRF9610	PD-9.350
2	IRFC9204R	−60	0.280	26	0.008/0.203	0.008/0.203	IRF9Z24	—
	IRFC9120R	−100	0.600	27	0.008/0.203	0.008/0.203	IRF9520	PD-9.319
	IRFC9220	−200	1.500	28	0.008/0.203	0.008/0.203	IRF9620	PD-9.351
3	IRFC9034R *	−60	0.140	29	0.010/0.254	0.010/0.254	IRF9Z34	—
	IRFC9130R *	−100	0.300	30	0.010/0.254	0.010/0.254	IRF9530	PD-9.320
	IRFC9230 *	−200	0.800	31	0.010/0.254	0.010/0.254	IRF9630	PD-9.352
4	IRFC9140R *	−100	0.250	32	0.020/0.508	0.020/0.508	IRF9540	PD-9.421
	IRFC9240 *	−200	0.500	33	0.020/0.508	0.020/0.508	IRF9640	PD-9.422

Common Characteristics

$R_{DS(on)}$: V_{GS} = 10V.

I_{DSS} @ V_{DS} : N-CHANNEL — 250μA : P-CHANNEL — −250μA.

I_{GSS} : N-CHANNEL — 500nA : P-CHANNEL — −100nA.

$V_{GS(th)}$: N-CHANNEL — min. 2V max. 4V @ $V_{DS} = V_{GS}$, I_D = 250μA.
P-CHANNEL — min. −2V max. −4V @ $V_{DS} = V_{GS}$, I_D = 250μA.

* These die are available screened to '883', 'ESA', 'LAT' and 'VIS'. For further details contact your local sales office.

TABLE 3: ELECTRICAL PROBE SPECIFICATIONS FOR N-CHANNEL HEXSense POWER MOSFET DIE

HEX size	Part Number	V_{DS} V	$R_{DS(on)}$ Ω	Nominal Sense Ratio	Figure	Recommended Bond Wire Size Source in/mm	Gate in/mm	Closest Part Number	Bulletin
2	IRCC024	60	0.100	780	34	0.010/0.254	0.003/0.076 to 0.005/0.127	IRCZ24	PD-9.564
3	IRCC034	60	0.050	1512	35			IRCZ34	PD-9.545
	IRCC130	100	0.160	1500	36			IRC530	PD-9.454
	IRCC230	200	0.400	1490	36			IRC630	PD-9.565
	IRCC234	250	0.450	1500	36			IRC634	PD-9.565
	IRCC330	400	1.000	1410	36			IRC730	PD-9.567
	IRCC430	500	1.500	1500	36			IRC830	PD-9.455
4	IRCC044	60	0.028	2820	37			IRCZ44	PD-9.529
	IRCC140	100	0.077	2670	38			IRC540	PD-9.498
	IRCC240	200	0.180	2670	38			IRC640	PD-9.568
	IRCC244	250	0.280	2670	38			IRC644	PD-9.569
	IRCC340	400	0.550	2670	38			IRC740	PD-9.570
	IRCC440	500	0.850	2670	38			IRC840	PD-9.501

TABLE 4: ELECTRICAL PROBE SPECIFICATIONS FOR P-CHANNEL LOGIC LEVEL MOSFET DIE

HEX size	Part Number	V_{DS} V	$R_{DS(on)}$ Ω	Figure	Recommended Bond Wire Size Source in/mm	Gate in/mm	Closest Part Number	Bulletin
1	IRLC014	60	0.300	2	0.005/0.127	0.005/0.127	IRLZ14	PD-9.556
	IRLC110	100	0.750	3	0.005/0.127	0.005/0.127	IRL510	PD-9.560
2	IRLC024	60	0.150	6	0.008/0.203	0.005/0.127	IRLZ24	PD-9.557
	IRLC120	100	0.400	7	0.008/0.203	0.005/0.127	IRL520	PD-9.561
3	IRLC034	60	0.070	10	0.010/0.254	0.005/0.127	IRLZ34	PD-9.558
	IRLC130	100	0.220	11	0.010/0.254	0.005/0.127	IRL530	PD-9.562
4	IRLC044	60	0.040	14	0.015/0.381	0.005/0.271	IRLZ44	PD-9.559
	IRLC140	100	0.110	15	0.015/0.381	0.005/0.271	IRL540	PD-9.563

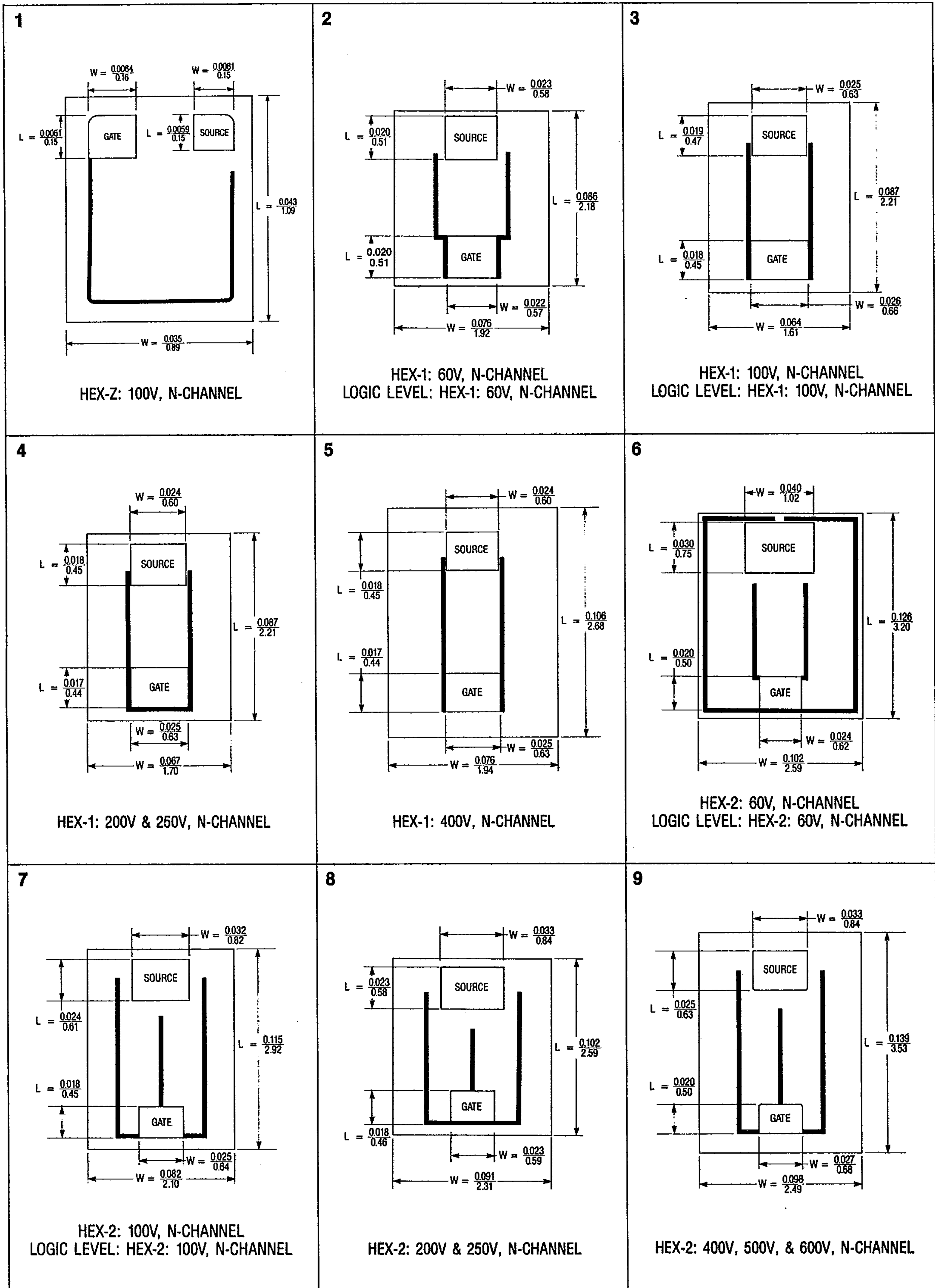
TABLE 5: ELECTRICAL PROBE SPECIFICATIONS FOR INSULATED GATE BIPOLAR TRANSISTOR DIE

HEX size	Part Number	V_{DS} V	$R_{DS(on)}$ Ω	Figure	Recommended Bond Wire Size Emitter in/mm	Gate in/mm	Closest Part Number	Bulletin
2	IRGCC20	600	4.0	39	0.012/0.305	0.005/0.127	IRGBC20	PD-9.626
	IRGCC26	600	2.5	39	0.012/0.305	0.005/0.127	IRGBC26	PD-9.669
3	IRGCC30	600	3.8	40	0.015/0.381	0.005/0.127	IRGBC30	PD-9.619
	IRGCC36	600	2.3	40	0.015/0.381	0.005/0.127	IRGBC36	PD-9.668
4	IRGCC40	600	3.6	41	0.020/0.508	0.005/0.127	IRGBC40	PD-9.627
	IRGCC46	600	1.8	41	0.020/0.508	0.005/0.127	IRGBC46	PD-9.667
5	IRGCC50	600	3.1	42	0.020/0.508	0.005/0.127	IRGPC50	PD-9.664
	IRGCC56	600	1.6	42	0.020/0.508	0.005/0.127	IRGPC56	PD-9.662

Common Characteristics

$R_{DS(on)}$: HEXSense — V_{GS} = 10V. Logic Level — V_{GS} = 4V.
I_{DSS} @ V_{DS} : HEXSense — 250μA : Logic Level — 250μA.
I_{GSS} : HEXSense — 500nA : Logic Level — 500nA.
$V_{GS(th)}$: HEXSense — min. 2V max. 4V @ V_{DS} = V_{GS}, I_D = 250μA.
Logic Level — min. 2V max. 4V @ V_{DS} = V_{DS} = V_{GS}, I_D = 250μA.
$V_{GE(th)}$: IGBT — min. 2.5V max. 5V @ V_{DS} = V_{GS}, I_D = 250μA.
I_{CES} @ V_{CE} : IGBT — 250μA max. V_{GEO} = 0V.
I_{GES} : IGBT — ±500na max. V_{GE} = ±20V.

DIE AND BONDING PAD DIMENSIONS



All dimensions in millimetres (inches)

DIE AND BONDING PAD DIMENSIONS cont'd.

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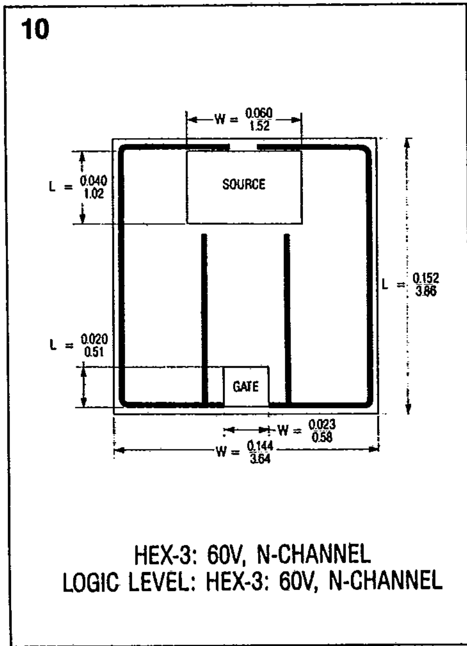

HEX-3: 60V, N-CHANNEL
LOGIC LEVEL: HEX-3: 60V, N-CHANNEL

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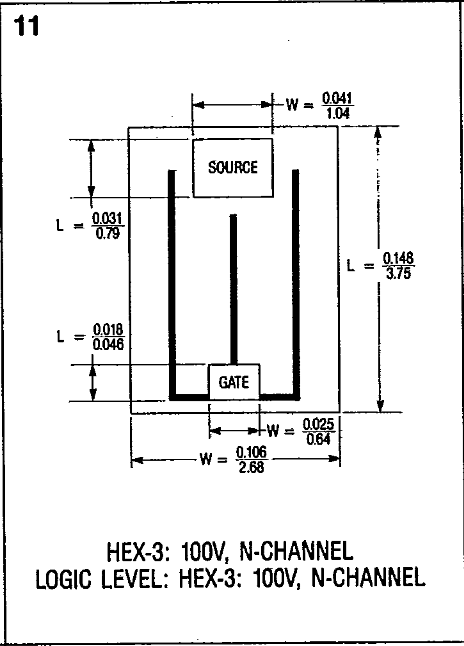

HEX-3: 100V, N-CHANNEL
LOGIC LEVEL: HEX-3: 100V, N-CHANNEL

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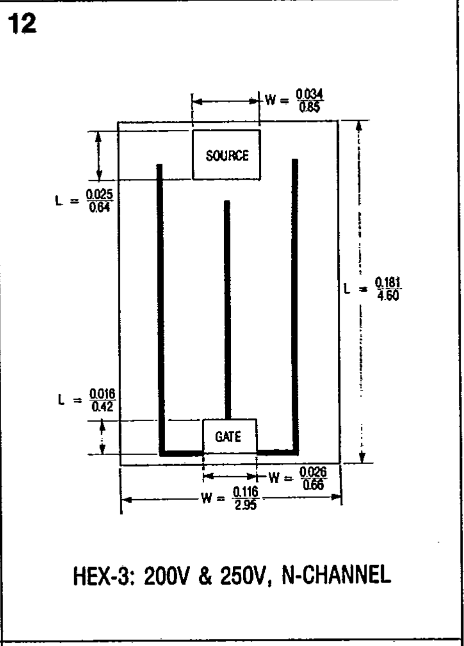

HEX-3: 200V & 250V, N-CHANNEL

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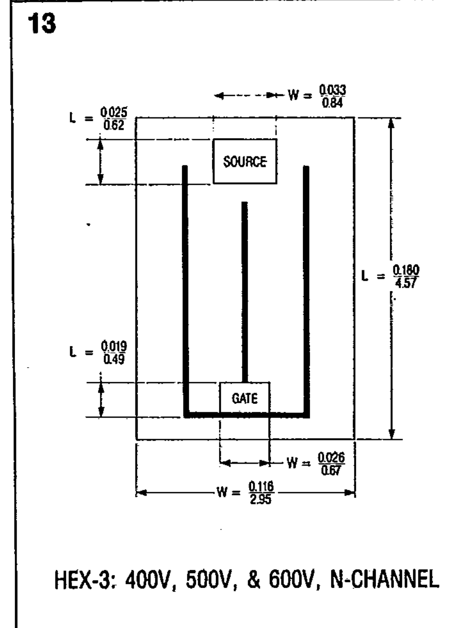

HEX-3: 400V, 500V, & 600V, N-CHANNEL

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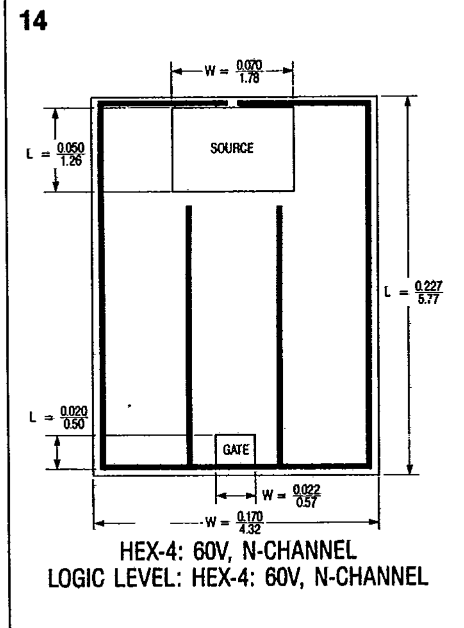

HEX-4: 60V, N-CHANNEL
LOGIC LEVEL: HEX-4: 60V, N-CHANNEL

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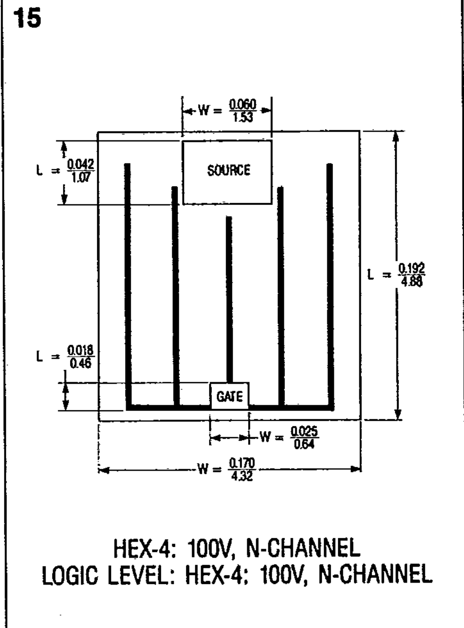

HEX-4: 100V, N-CHANNEL
LOGIC LEVEL: HEX-4: 100V, N-CHANNEL

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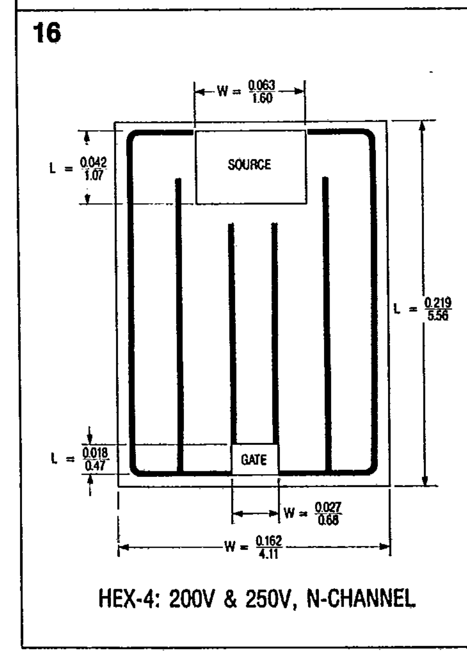

HEX-4: 200V & 250V, N-CHANNEL

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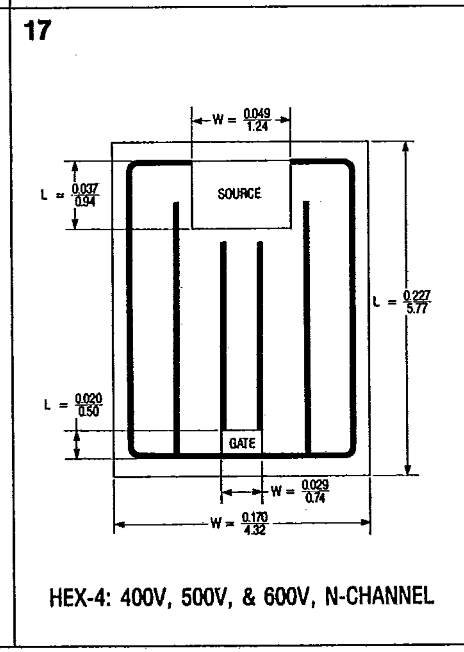

HEX-4: 400V, 500V, & 600V, N-CHANNEL

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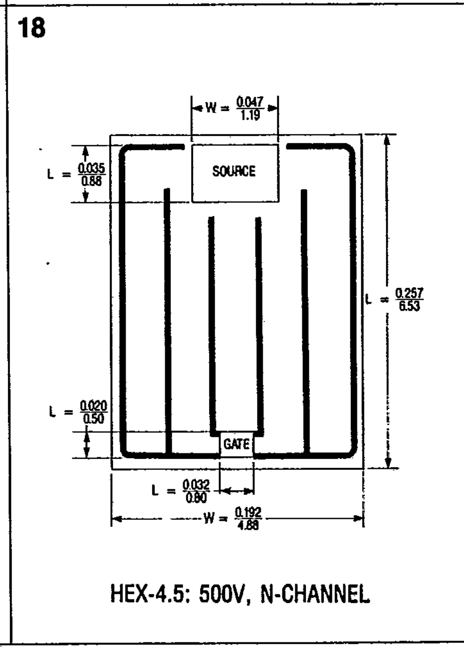
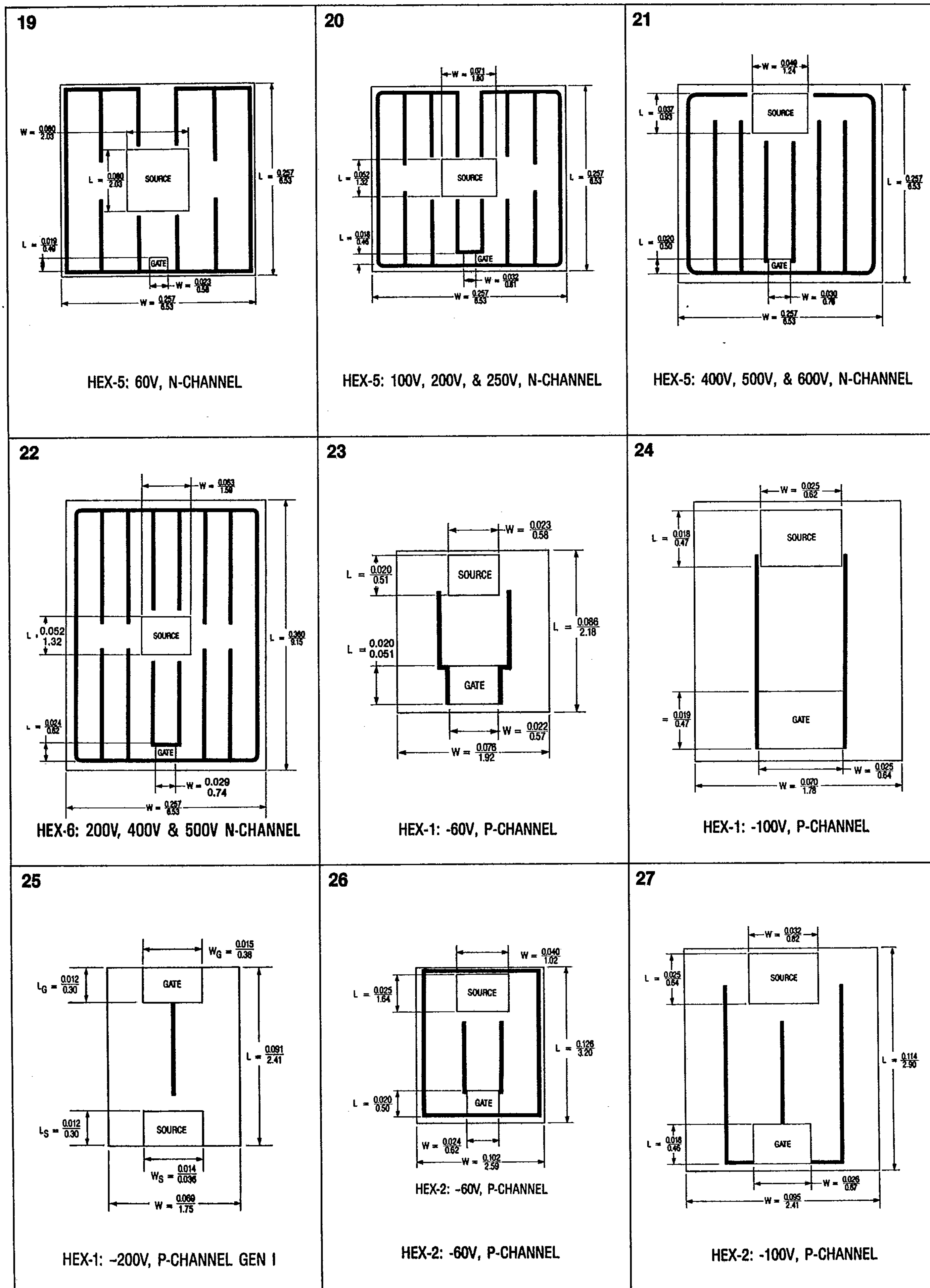


HEX-4.5: 500V, N-CHANNEL

All dimensions in millimetres (inches)

DIE AND BONDING PAD DIMENSIONS cont'd.



DIE AND BONDING PAD DIMENSIONS cont'd.

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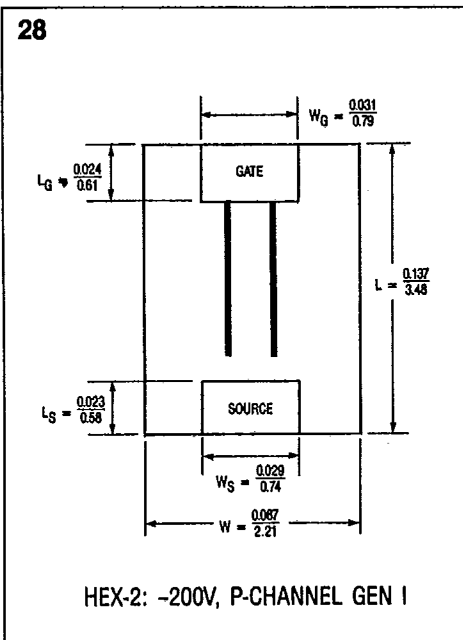
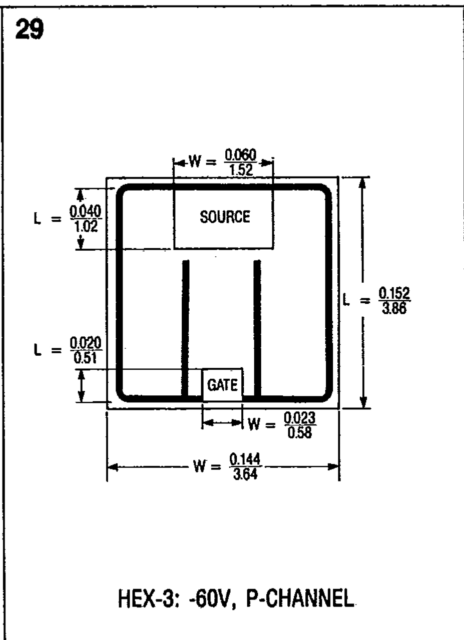


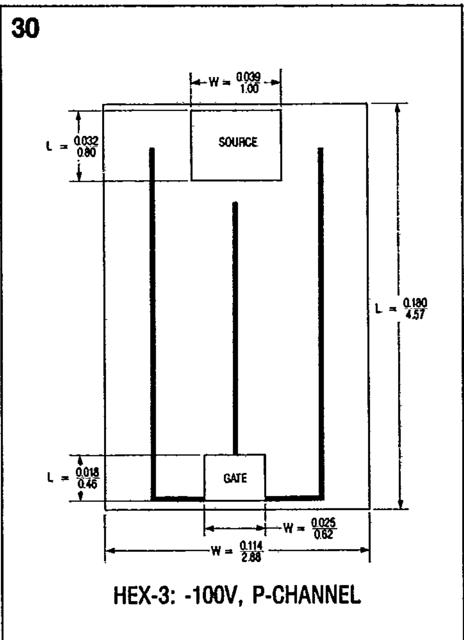
HEX-2: -200V, P-CHANNEL GEN I

29



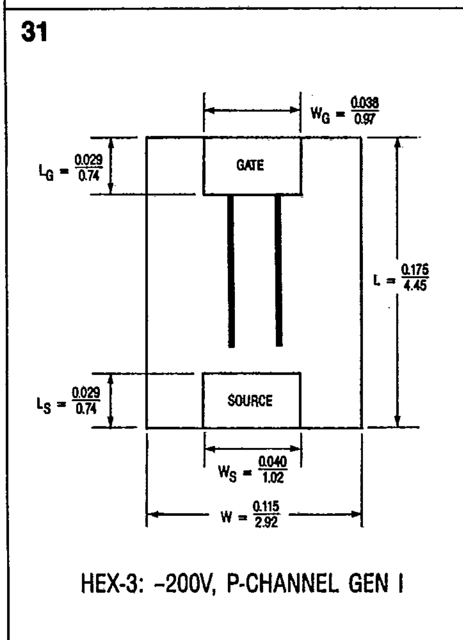
HEX-3: -60V, P-CHANNEL

30



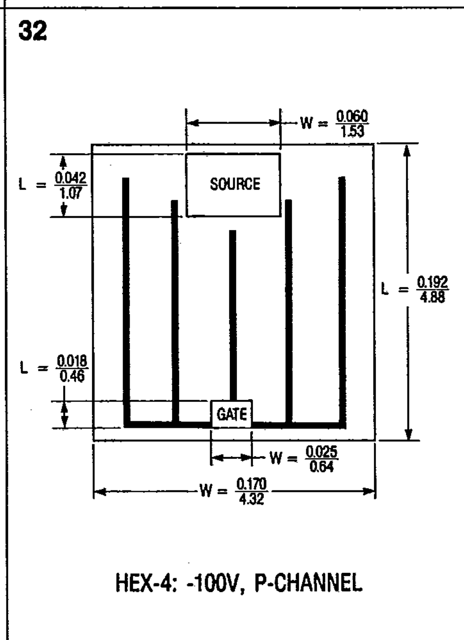
HEX-3: -100V, P-CHANNEL

31



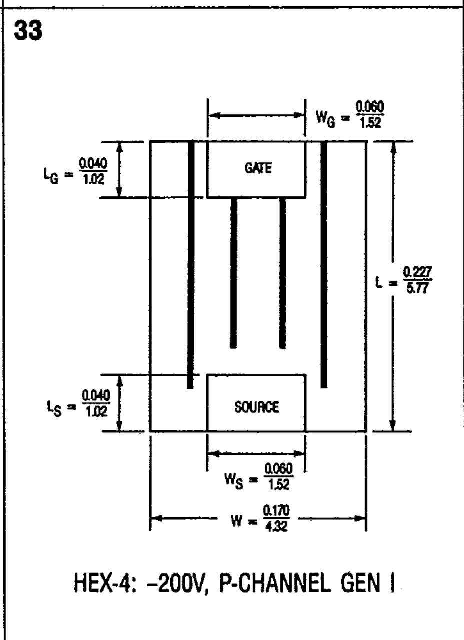
HEX-3: -200V, P-CHANNEL GEN I

32



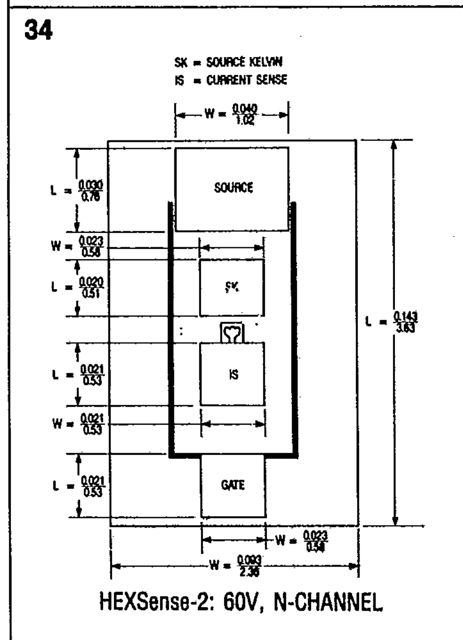
HEX-4: -100V, P-CHANNEL

33



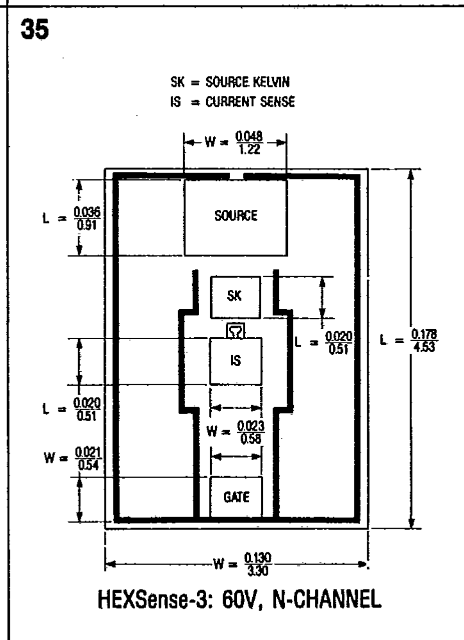
HEX-4: -200V, P-CHANNEL GEN I

34



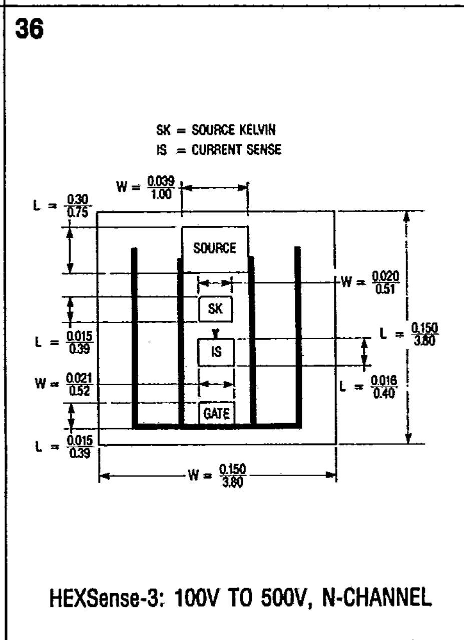
HEXSense-2: 60V, N-CHANNEL

35



HEXSense-3: 60V, N-CHANNEL

36



HEXSense-3: 100V TO 500V, N-CHANNEL

All dimensions in millimetres (inches)

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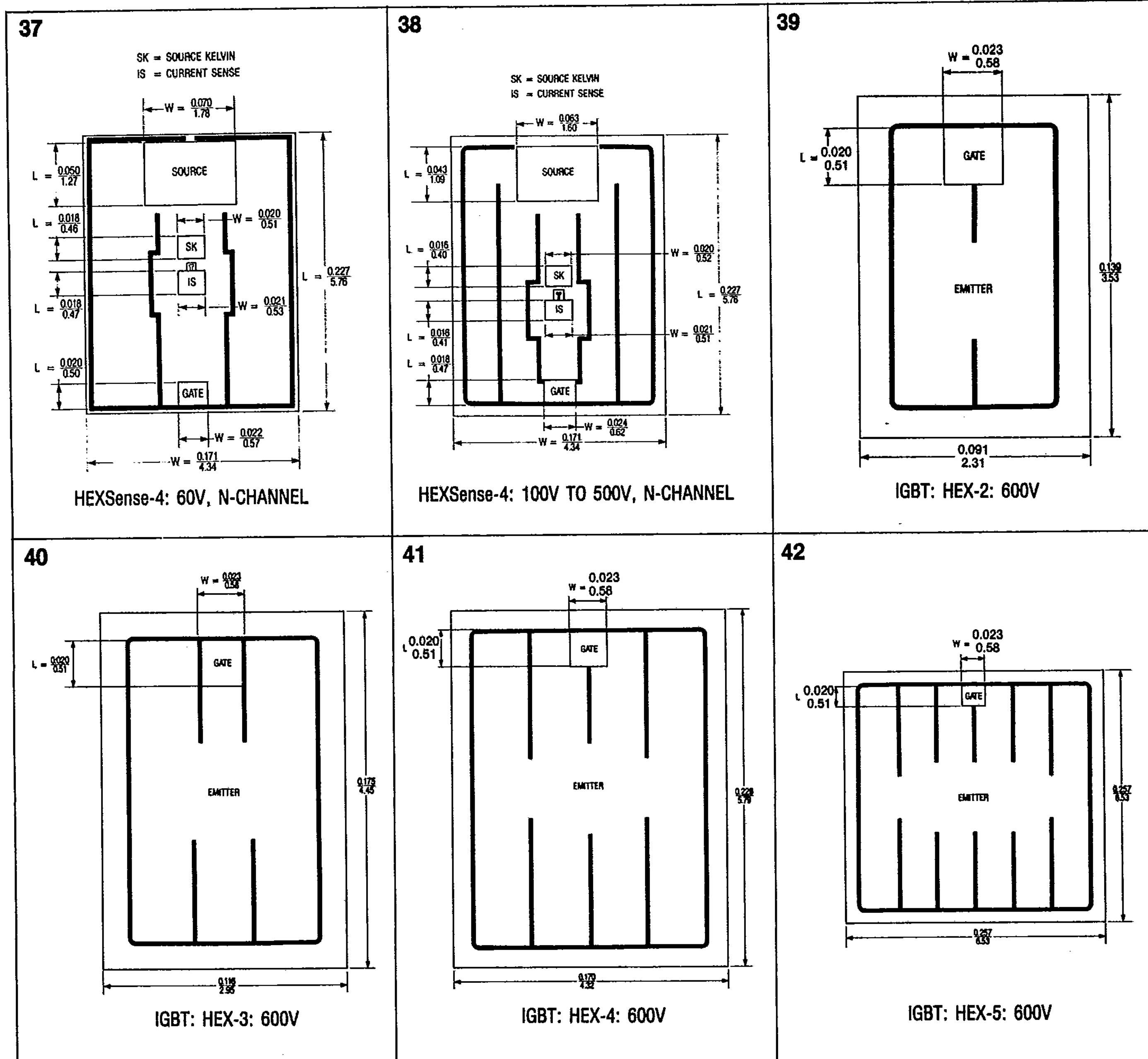
DIE AND BONDING PAD DIMENSIONS cont'd.



Chip Tray Capacity by Die Size

HEXFET DIE	HEX-Z	HEX-1	HEX-2	HEX-3	HEX-4	HEX-4.5	HEX-5	HEX-6
Chip Tray Capacity	400	140	96	45*	35	16	16	15

*35 for Generation I.
Please note that chips are only sold in multiples of the trays shown above.

Dimensional Tolerances

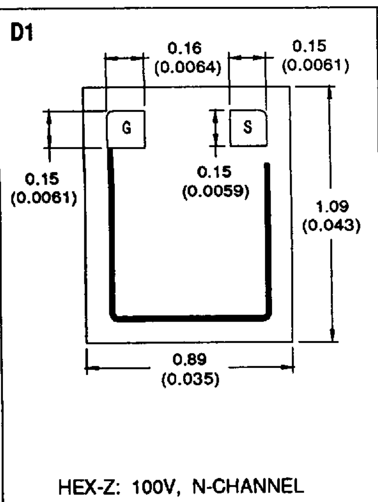
Bonding Pad L or W:
< 0.025 in., Tolerance = ±0.0005 in.
> 0.025 in., Tolerance = ±0.001 in.

Overall Die L or W:
< 0.050 in., Tolerance = ±0.004 in.
> 0.050 in., Tolerance = ±0.008 in.

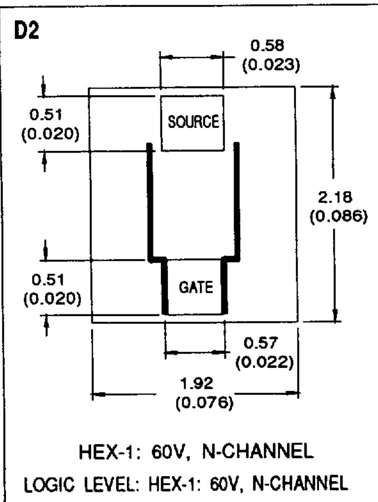
Die Thickness
0.0187 ± 0.001 in. / 0.475 ± 0.02 mm.

Appendix F

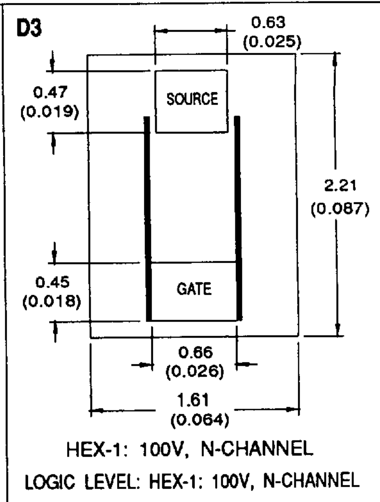
HEXFET Die Outlines



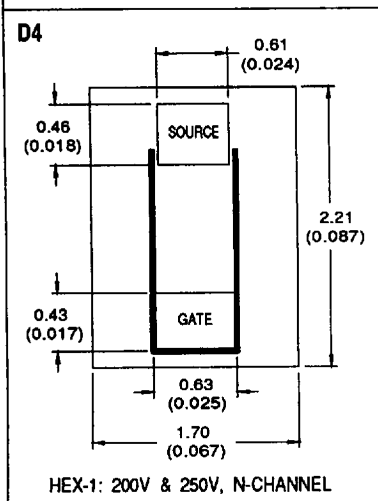
HEX-Z: 100V, N-CHANNEL



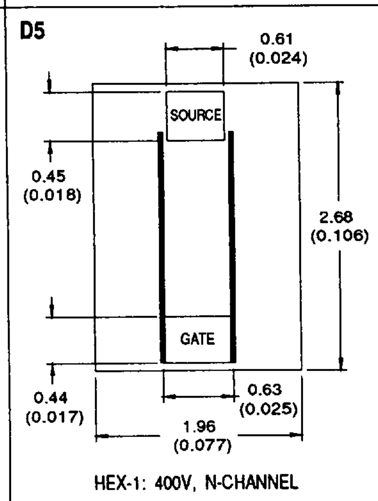
HEX-1: 60V, N-CHANNEL
LOGIC LEVEL: HEX-1: 60V, N-CHANNEL



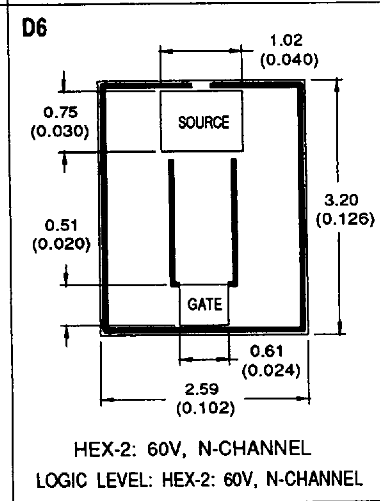
HEX-1: 100V, N-CHANNEL
LOGIC LEVEL: HEX-1: 100V, N-CHANNEL



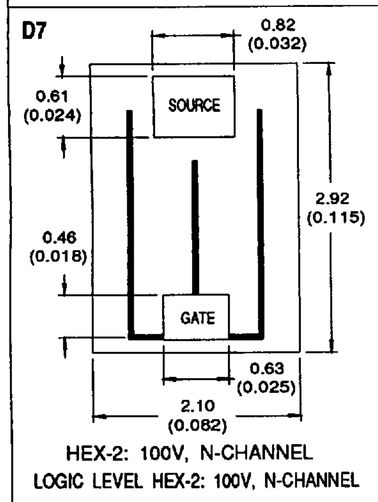
HEX-1: 200V & 250V, N-CHANNEL



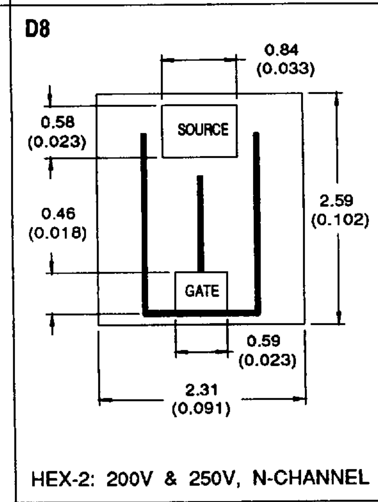
HEX-1: 400V, N-CHANNEL



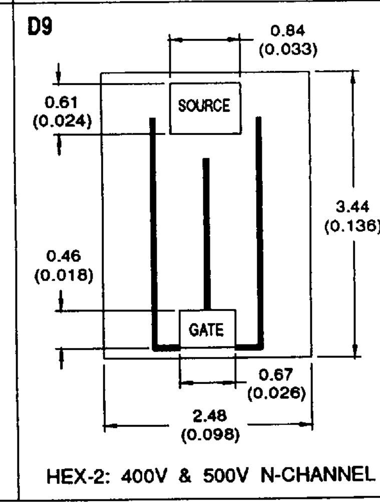
HEX-2: 60V, N-CHANNEL
LOGIC LEVEL: HEX-2: 60V, N-CHANNEL



HEX-2: 100V, N-CHANNEL
LOGIC LEVEL HEX-2: 100V, N-CHANNEL



HEX-2: 200V & 250V, N-CHANNEL



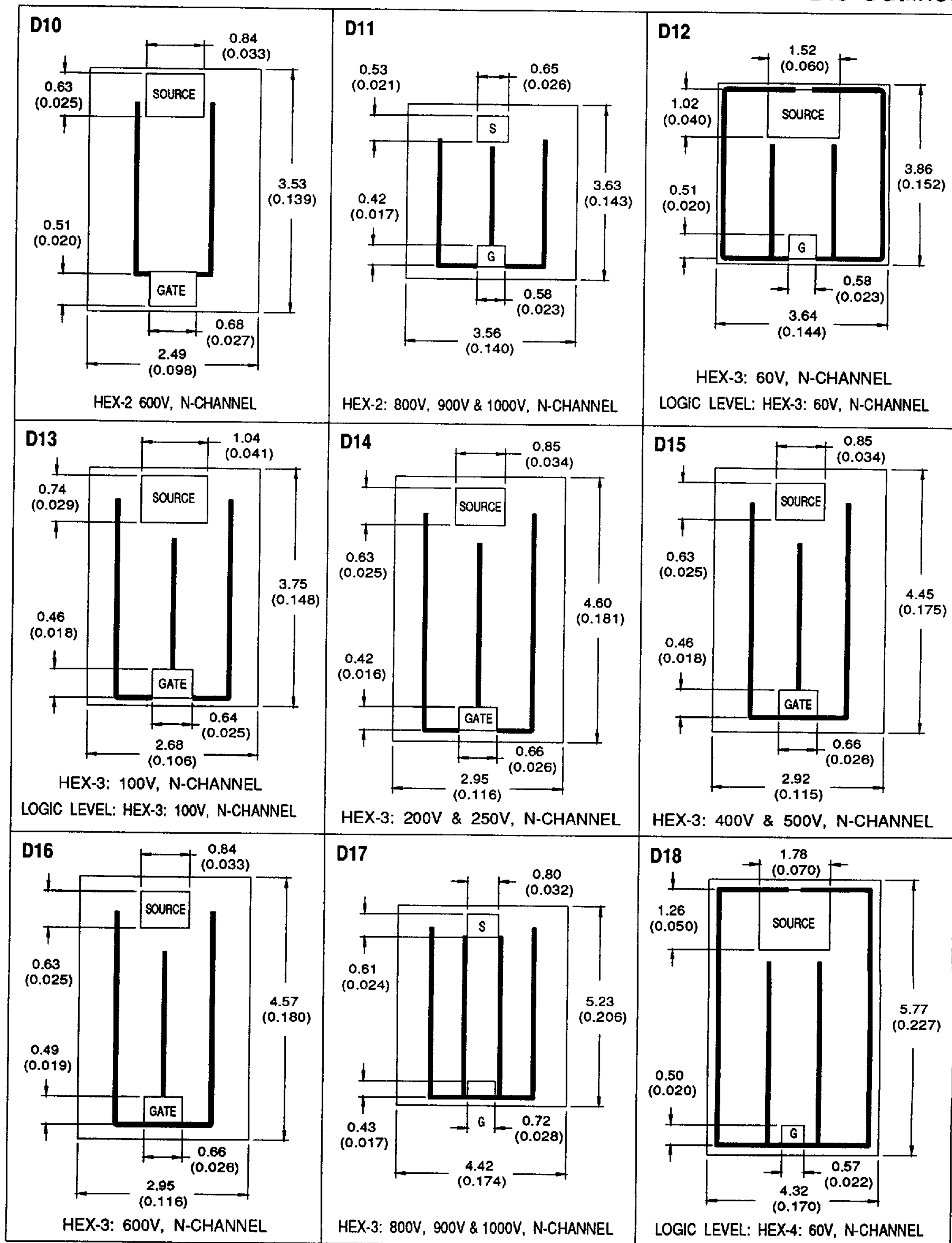
HEX-2: 400V & 500V N-CHANNEL

SEE NOTES FOR TOLERANCES AND ALL OTHER INFORMATION PAGE 1534

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)

Appendix F

HEXFET Die Outlines

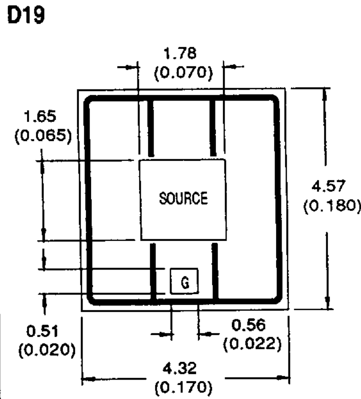


SEE NOTES FOR TOLERANCES AND ALL OTHER INFORMATION PAGE 1534

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)

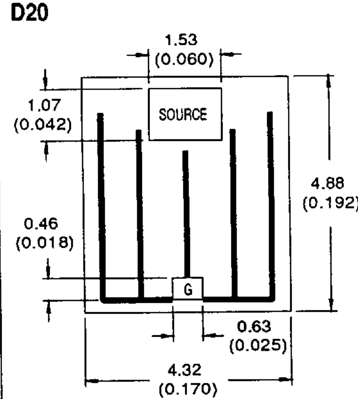
HEXFET Die Outlines

D19



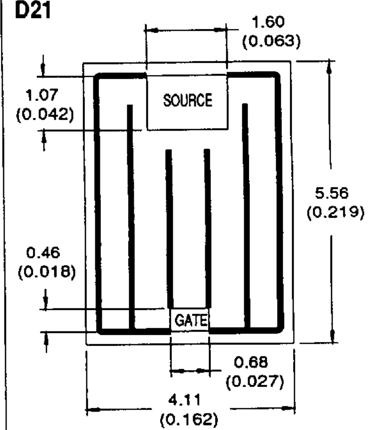
HEX-4: 50V & 60V, N-CHANNEL

D20



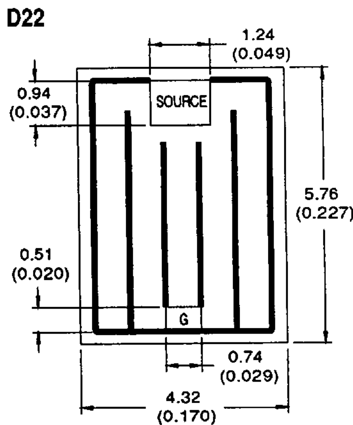
HEX-4: 100V, N-CHANNEL
LOGIC LEVEL: HEX-4: 100V, N-CHANNEL

D21



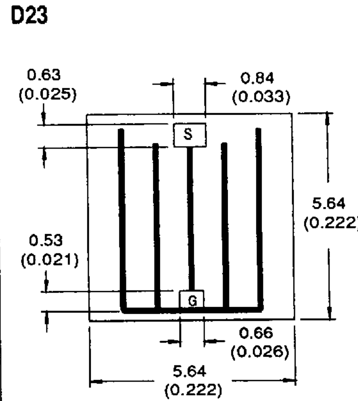
HEX-4: 200V & 250V, N-CHANNEL

D22



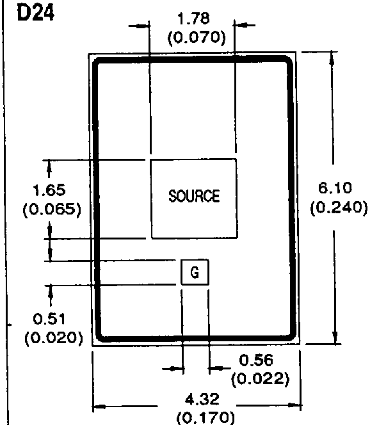
HEX-4: 400V, 500V & 600V, N-CHANNEL

D23



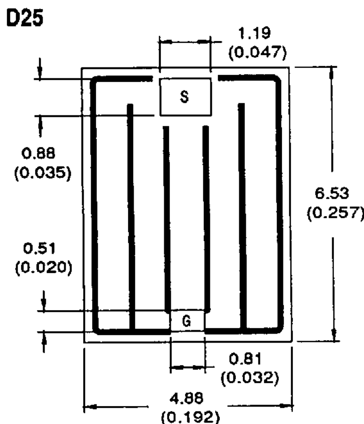
HEX-4: 800V, 900V & 1000V, N-CHANNEL

D24



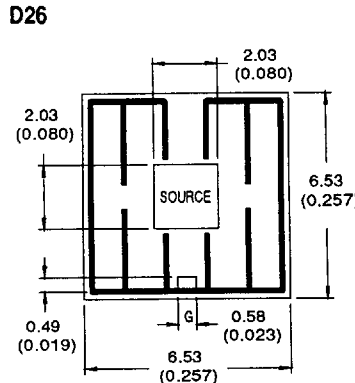
HEX-4.1: 60V, N-CHANNEL

D25



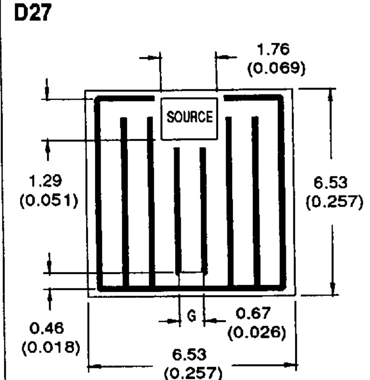
HEX-4.5: 500V, N-CHANNEL

D26



HEX-5: 60V, N-CHANNEL

D27



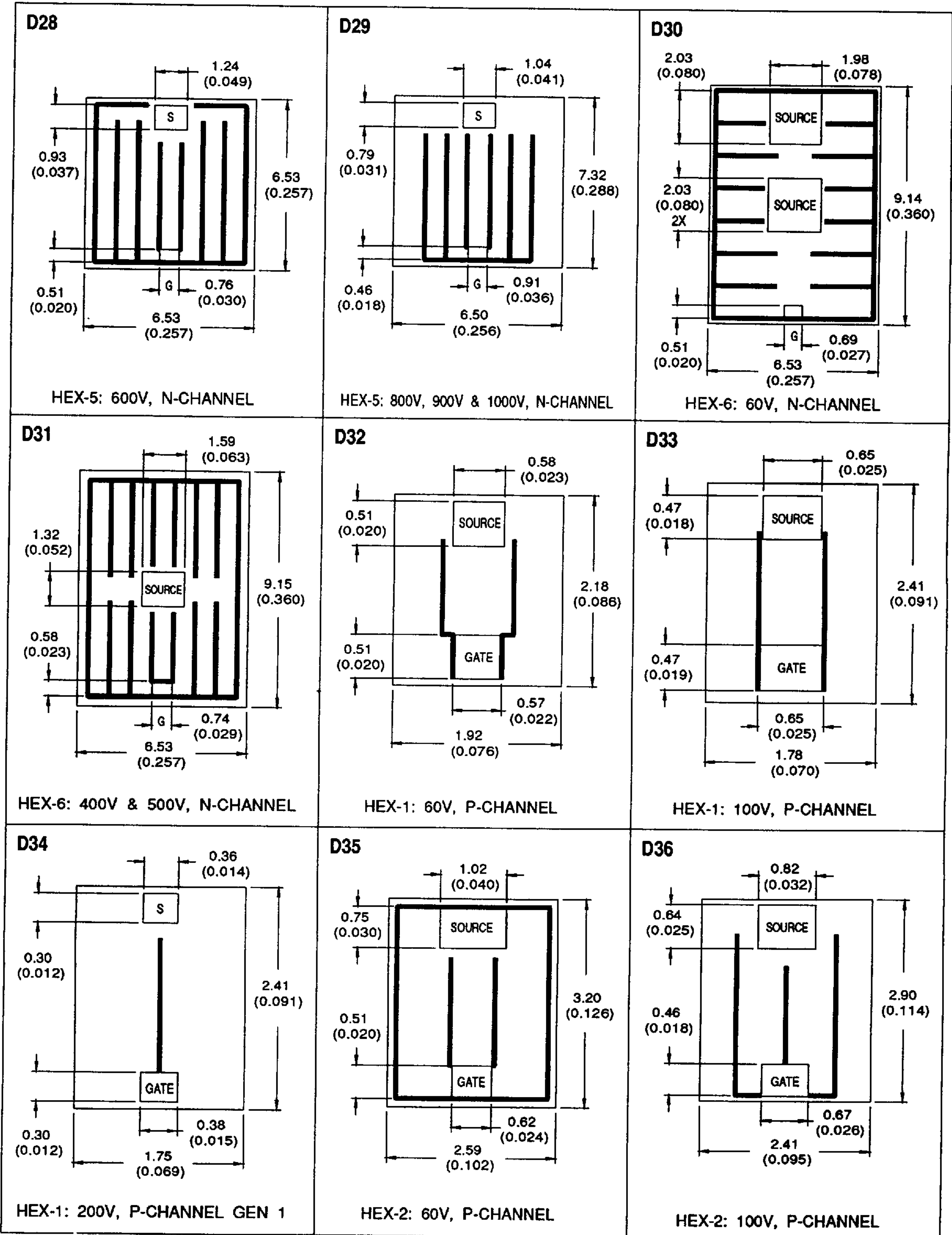
HEX-5: 100V, 200V, 250V, 400V & 500V N-CHANNEL

SEE NOTES FOR TOLERANCES AND ALL OTHER INFORMATION PAGE 1534

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)

Appendix F

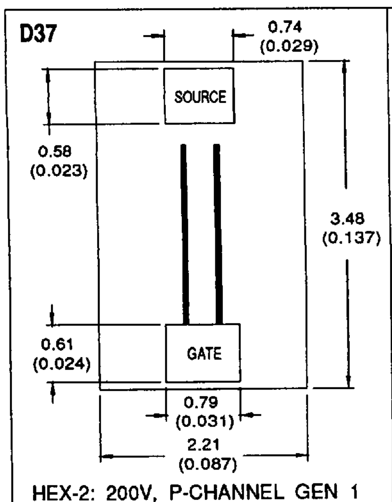
HEXFET Die Outlines



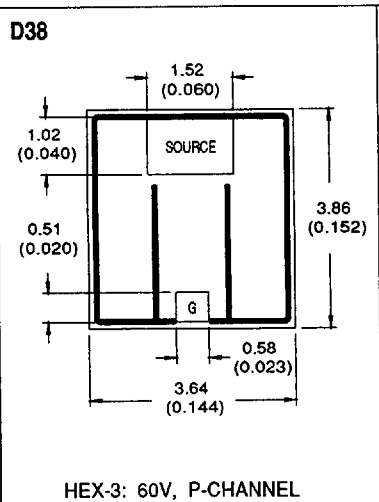
SEE NOTES FOR TOLERANCES AND ALL OTHER INFORMATION PAGE 1534

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)

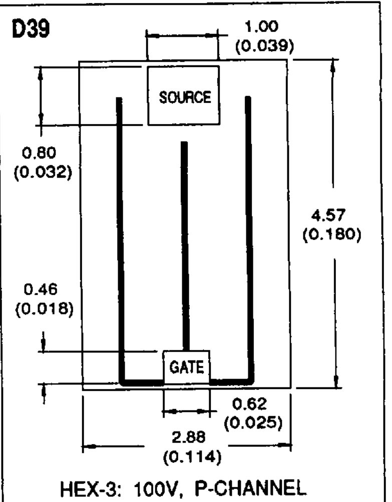
HEXFET Die Outlines



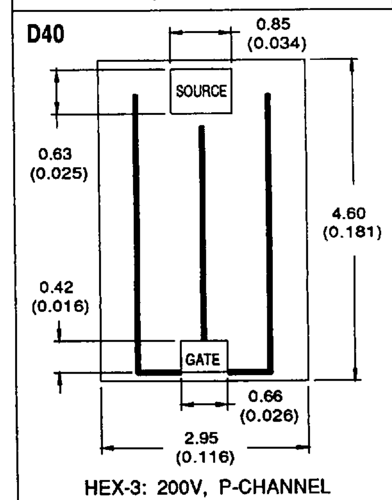
HEX-2: 200V, P-CHANNEL GEN 1



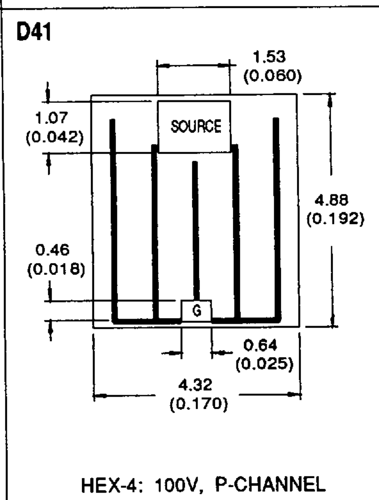
HEX-3: 60V, P-CHANNEL



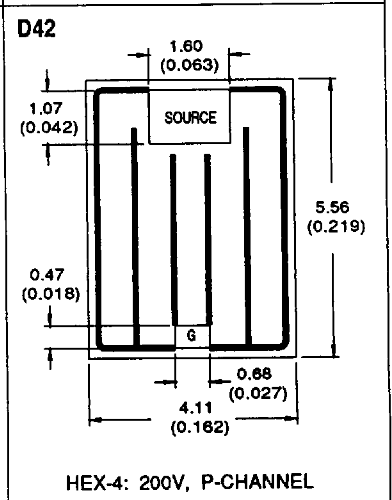
HEX-3: 100V, P-CHANNEL



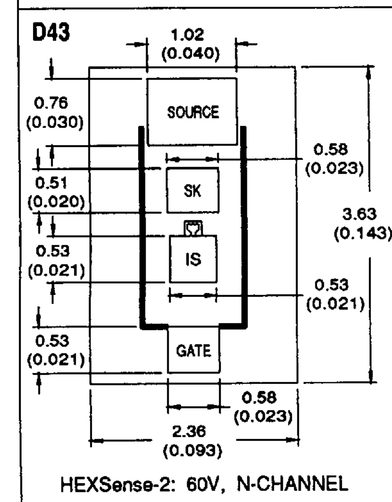
HEX-3: 200V, P-CHANNEL



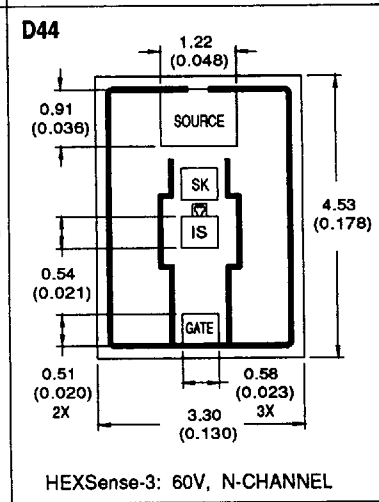
HEX-4: 100V, P-CHANNEL



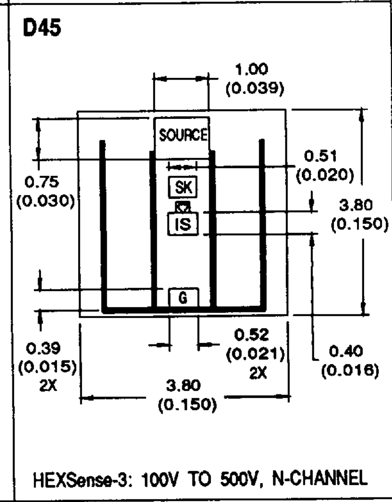
HEX-4: 200V, P-CHANNEL



HEXSense-2: 60V, N-CHANNEL



HEXSense-3: 60V, N-CHANNEL



HEXSense-3: 100V TO 500V, N-CHANNEL

SEE NOTES FOR TOLERANCES AND ALL OTHER INFORMATION PAGE 1534

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)

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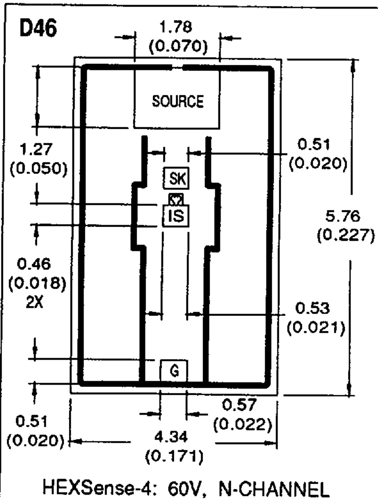
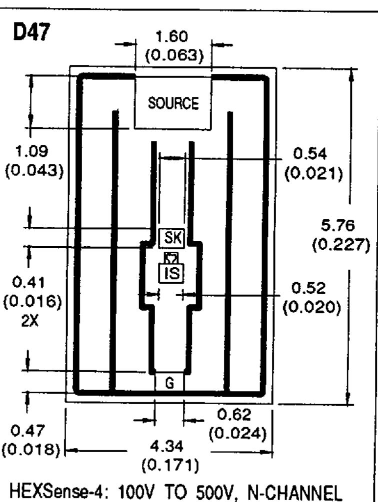
D46



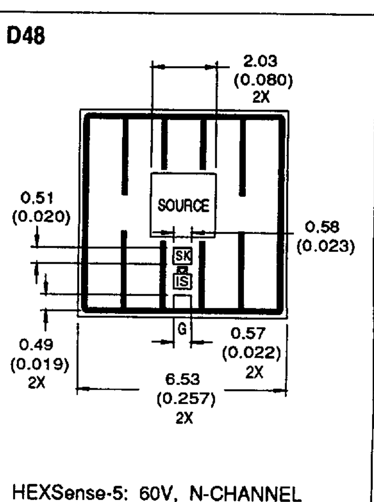
HEXSense-4: 60V, N-CHANNEL

D47



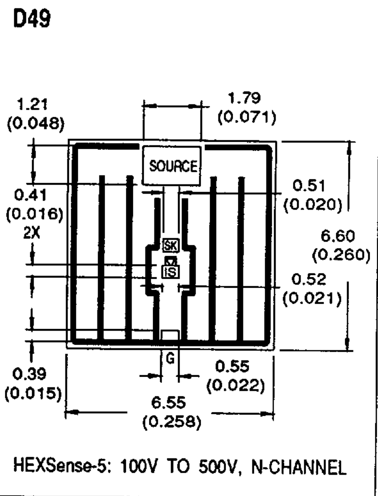
HEXSense-4: 100V TO 500V, N-CHANNEL

D48



HEXSense-5: 60V, N-CHANNEL

D49



HEXSense-5: 100V TO 500V, N-CHANNEL

D50

D51

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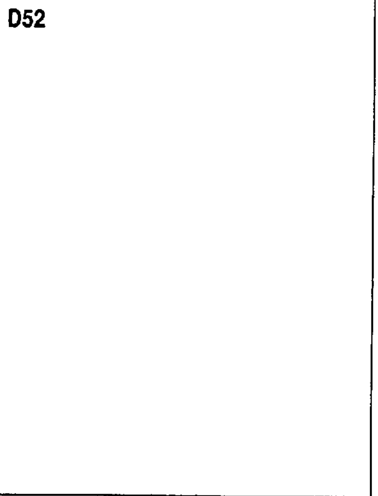
D52



NOTES:

1 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)

2 CONTROLLING DIMENSION: (INCH).

3. LETTER DESIGNATION:
   - S = SOURCE SK = SOURCE KELVIN
   - G = GATE IS = CURRENT SENSE

4. DIMENSIONAL TOLERANCES:

BONDING PADS: WIDTH & LENGTH	< 0.635 TOLERANCE	= +/- 0.013
	< (0.0250) TOLERANCE	= +/- (0.0005)
	> 0.635 TOLERANCE	= +/- 0.025
	> (0.0250) TOLERANCE	= +/- (0.0010)
OVERALL DIE: WIDTH & LENGTH	< 1.270 TOLERANCE	= +/- 0.102
	< (0.050) TOLERANCE	= +/- (0.004)
	> 0.635 TOLERANCE	= +/- 0.203
	> (0.050) TOLERANCE	= +/- (0.008)

5. UNLESS OTHERWISE NOTED ALL DIE ARE GEN III

FOR ADDITIONAL INFORMATION, SEE TABLE 1 SELECTION GUIDE ON PAGE xxi

ALL DIMENSIONS SHOWN IN MILLIMETERS (INCHES)