REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
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REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Kenneth Rice

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APPROVED BY: [signature]

DRAWING APPROVAL DATE: 26 MAY 1989

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS
64K X 16 UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86805
A	67268	

SHEET 1 OF 14

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1319

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86805	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27C1024	64K x 16-bit UVEPROM	300 ns
02	27C1024	64K x 16-bit UVEPROM	250 ns
03	27C1024	64K x 16-bit UVEPROM	200 ns
04	27C1024	64K x 16-bit UVEPROM	170 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package 1/
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package 1/

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Input voltages with respect to ground	-0.6 V dc to V_{CC} +0.5 V dc
Voltage on pin A_9 with respect to ground	-0.6 V dc to +13.5 V dc
V_{PP} supply voltage with respect to ground	-0.6 V dc to +13.5 V dc
Power dissipation (P_D) 2/	330 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J) 3/	+150°C
Data retention	10 years, minimum
Endurance	50 cycles/byte, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage range (V_{CC})	+4.5 V dc to 5.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.
3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{IN} = 0 V to 5.5 V	1, 2, 3	All	-5	+5	µA
Output leakage current	I_{LO} 1/	V_{OUT} = 0 V to 5.5 V	1, 2, 3	All	-10	+10	µA
Operating current	I_{CC1}	$V_{CC} = V_{PP}$ = 5.5 V $\overline{CE} = \overline{OE} = V_{IL}$ O_{0-15} = 0 mA $f = 1/t_{AVQV}$ (maximum)	1, 2, 3	All		60	mA
Standby current (TTL inputs)	I_{CC2}	V_{CC} = 5.5 V $\overline{CE} = V_{IH}$	1, 2, 3	All		1.0	mA
Standby current (CMOS inputs)	I_{CC3}	V_{CC} = 5.5 V $\overline{CE} = V_{CC} \pm 0.3$ V	1, 2, 3	All		120	µA
V_{PP} supply current (read)	I_{PP}	V_{PP} = 5.5 V	1, 2, 3	All		100	µA
Input low voltage (TTL)	V_{IL} 2/		1, 2, 3	All	-0.1 3/	0.8	V
Input high voltage (TTL)	V_{IH} 2/		1, 2, 3	All	2.0	V_{CC} +0.5 3/	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output short-circuit	I_{OS} 3/	V_O = 0 V	1, 2, 3	All	-200	+200	mA
Input capacitance	C_{IN} 4/ 5/	V_{IN} = 0 V, T_C = +25°C f = 1 MHz See 4.3.1c	4	All		25	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0\ V$; $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output capacitance	C_{OUT} 4/ 5/	V_{OUT} = 0 V, T_C = +25°C f = 1 MHz See 4.3.1c	4	All		25	pF
Functional tests		See 4.3.1e	7, 8	All			
Address to output delay	t_{AVQV}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 6/ See figures 3 and 4 as applicable	9, 10, 11	01		300	ns
				02		250	
				03		200	
				04		170	
$\overline{CE}$ to output delay	t_{ELQV}	$\overline{OE}$ = V_{IL} 6/ See figures 3 and 4 as applicable	9, 10, 11	01		300	ns
				02		250	
				03		200	
				04		170	
$\overline{OE}$ to output delay	t_{OLQV}	$\overline{CE}$ = V_{IL} 6/ See figures 3 and 4 as applicable	9, 10, 11	01		120	ns
				02		100	
				03		75	
				04		65	
$\overline{CE}$ and $\overline{OE}$ high to output float	t_{EHQZ} t_{OHQZ} 4/	See figures 3 and 4 as applicable	9, 10, 11	01			ns
				02		60	
				03			
				04		50	
Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occurred first	t_{AXQX} 3/		9, 10, 11	All	0		ns

See footnotes at top of next page.

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1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{LO} with the output under test connected to V_{OUT}.
2/ Test for all input and control pins.
3/ May not be tested, but shall be guaranteed to the limits specified in table I.
4/ Tested initially and after any design changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested shall be grounded.
6/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load = 1 TTL gate and C_L = 100 pF.
Input rise and fall times < 20 ns.
Input pulse levels: 0.45 V and 2.4 V.
Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V
Outputs = 0.8 V and 2.0 V

3.5 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.4 herein.

3.5.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.5.3 Verification of erasure and/or programmability of EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

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Device types	01 through 04		Device types	01 through 04	
Case outlines	Q	X	Case outlines	Q	X
Terminal number	Terminal Symbol		Terminal number	Terminal Symbol	
1	V_{PP}	NC	23	A_2	NC
2	$\overline{CE}$	V_{PP}	24	A_3	A_0
3	I/O_{15}	$\overline{CE}$	25	A_4	A_1
4	I/O_{14}	I/O_{15}	26	A_5	A_2
5	I/O_{13}	I/O_{14}	27	A_6	A_3
6	I/O_{12}	I/O_{13}	28	A_7	A_4
7	I/O_{11}	I/O_{12}	29	A_8	A_5
8	I/O_{10}	I/O_{11}	30	V_{SS}	A_6
9	I/O_{09}	I/O_{10}	31	A_9	A_7
10	I/O_{08}	I/O_{09}	32	A_{10}	A_8
11	V_{SS}	I/O_{08}	33	A_{11}	NC
12	I/O_{07}	V_{SS}	34	A_{12}	V_{SS}
13	I/O_{06}	NC	35	A_{13}	A_9
14	I/O_{05}	I/O_{07}	36	A_{14}	A_{10}
15	I/O_{04}	I/O_{06}	37	A_{15}	A_{11}
16	I/O_{03}	I/O_{05}	38	NC	A_{12}
17	I/O_{02}	I/O_{04}	39	$\overline{PGM}$	A_{13}
18	I/O_{01}	I/O_{03}	40	V_{CC}	A_{14}
19	I/O_0	I/O_{02}	41	---	A_{15}
20	$\overline{OE}$	I/O_{01}	42	---	NC
21	A_0	I/O_0	43	---	$\overline{PGM}$
22	A_1	$\overline{OE}$	44	---	V_{CC}

FIGURE 1. Terminal connections.

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	Pin function					
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ag	Vpp	Outputs
Read	L	L	X	X	X	Data out
Output disable	L	H	X	X	X	High Z
Standby	H	X	X	X	X	High Z
Program	L	X	L	X	Vpp	Data in
Program verify	L	L	H	X	Vpp	Data out
Program inhibit	H	X	X	X	Vpp	High Z
Auto select	L	L	X	V_H	X	Code

H = V_{IH}
L = V_{IL}
X = V_{IH} or V_{IL}
V_H = 12.0 ±0.5 V
Vpp = 12.5 ±0.3 V

FIGURE 2. Truth table.

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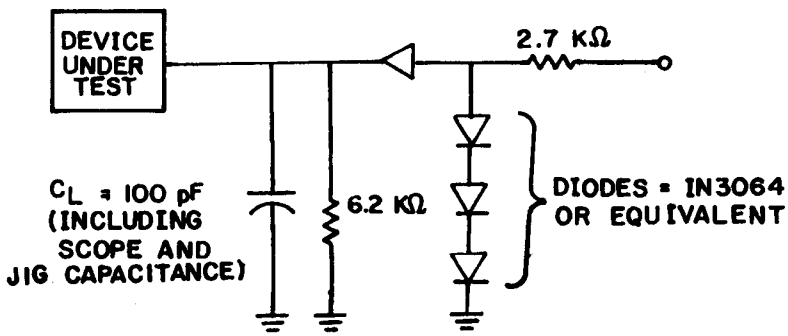

FIGURE 3. Switching times test circuit (or equivalent).

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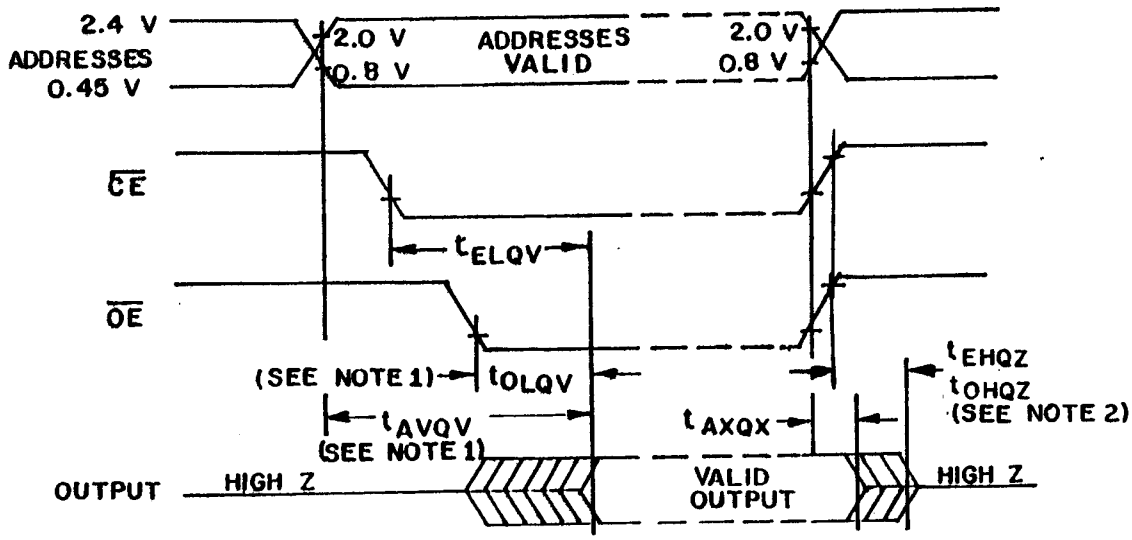

NOTES:
1. $\overline{OE}$ may be delayed up to $t_{AVQV} - t_{OLQV}$ after the falling edge of $\overline{CE}$ without impact on t_{AVQV}.
2. t_{OHQZ} or t_{EHQZ} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 4. Read cycle waveforms.

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4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps performed in the listed sequence.

Margin test method A. 1/

(1) Program at +25°C with a greater than 95 percent pattern (example, diagonal 1's) (see 3.5.2).

(2) Unbiased bake for 24 hours at +175°C.

(3) Test at +75°C (see 3.5.3), including a margin test at V_m = 6.0 V and loose timing (i.e., t_{AVQV} = 1 µs).

(4) Erase (see 3.5.1).

(5) Program at +25°C with a 50 percent pattern (example, checkerboard bar) (see 3.5.2). (Programmed with checkerboard at wafer sort.)

(6) Test at T_C = +130°C (see 3.5.3), including a margin test at V_m = 6.0 V and loose timing (i.e., t_{AVQV} = 1 µs).

(7) Burn-in (see 4.2a).

(8) Test at T_C = +25°C (see 3.5.3), including a margin test at V_m = 6.0 V and loose timing (i.e., t_{AVQV} = 1 µs).

(9) Test at T_C = +130°C (see 3.5.3), including a margin test at V_m = 6.0 V and loose timing (i.e., t_{AVQV} = 1 µs).

(10) Test at T_C = -55°C (see 3.5.3), including a margin test at V_m = 6.0 V and loose timing (i.e., t_{AVQV} = 1 µs).

(11) Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.

(12) Verify erasure at +25°C (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

1/ Steps 1 through 4 may be performed at wafer level.

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4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is 15 devices, all input and output terminals tested and no failures.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.3.2b). The devices to be submitted to the steady-state life testing shall be subjected to the following tests and examinations. Each device in the sample shall be subjected to a minimum 50-program and erase cycles.

(1) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent.

(2) Verify patterns (see 3.5.3).

(3) Erase (see 3.5.1).

(4) Verify pattern erasure (see 3.5.3).

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for exposure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 25 minutes using an ultraviolet lamp with a 12000 uW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 uW/cm^2). Exposure of EPROMs to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

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TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9, 10,11
Group A test requirements (method 5005) 5/	1,2,3,4***,7,8, 9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ (***) see 4.3.1c.
3/ Any subgroups at the same temperature may be combined when using a multifunction tester.
4/ (**) indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
5/ Subgroups 7 and 8 shall consist of verifying the applicable data pattern, see 4.3.1e.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8680501QX	34335	AM27C1024-300/BQA	
5962-8680501XX	34335	AM27C1024-300/BUA	
5962-8680502QX	34335	AM27C1024-250/BQA	
5962-8680502XX	34335	AM27C1024-250/BUA	
5962-8680503QX	34335	AM27C1024-200/BQA	
5962-8680503XX	34335	AM27C1024-200/BUA	
5962-8680504QX	34335	AM27C1024-170/BQA	
5962-8680504XX	34335	AM27C1024-170/BUA	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086	A

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