PowerMOS transistor Logic level TOPFET

BUK113-50DL

DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

FEATURES

- Vertical power DMOS output stage
- Overload protected up to 125˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage	-	50	V
I_D	Drain current limiting	4	8	A
P_D	Total power dissipation	-	4	W
T_j	Continuous junction temperature	-	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance	-	200	mΩ

FUNCTIONAL BLOCK DIAGRAM

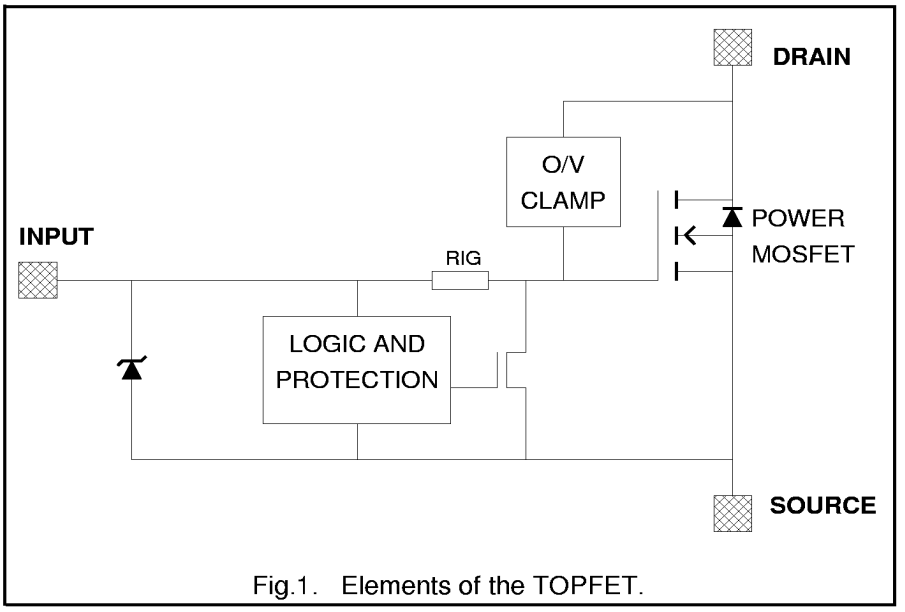
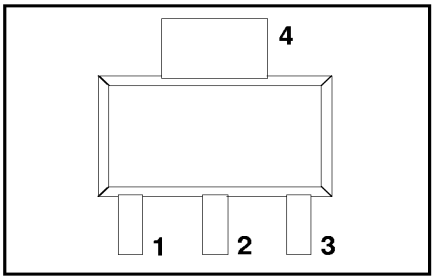


Fig.1. Elements of the TOPFET.

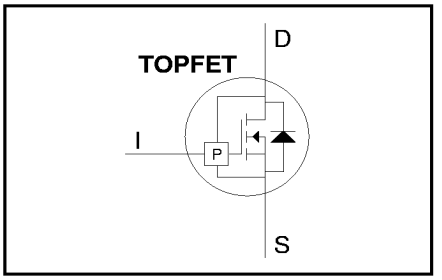
PINNING - SOT223

PIN	DESCRIPTION
1	input
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage[1]	-	-	50	V
I_D	Continuous drain current[2]	-	-	self limiting	A
I_I	Continuous input current	clamping	-	3	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1$ ms	-	10	mA
P_D	Total power dissipation	$T_{sp} = 90$ ˚C	-	4	W
T_{stg}	Storage temperature	-	-55	150	˚C
T_j	Continuous junction temperature	normal operation	-	150	˚C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Non-repetitive clamping energy	$T_b \leq 25$ ˚C; $I_{DM} < I_{D(lim)}$; inductive load	-	100	mJ
E_{DRM}	Repetitive clamping energy	$T_b \leq 75$ ˚C; $I_{DM} = 50$ mA; f = 250 Hz	-	4	mJ

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage[3]	for valid protection	4	-	V
V_{DDP}	Protected drain source supply voltage	$V_{IS} = 5$ V	-	35	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j\text{-}sp}$	Junction to solder point	measured to pin 4 solder point	-	12	15	K/W
	Application information					
$R_{th\ j\text{-}a}$	Junction to ambient	on PCB of fig. 3	-	70	-	K/W
		on minimum footprint PCB	-	100	-	K/W

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 The input voltage for which the overload protection circuits are functional.

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Overload protection					
$I_{D(lim)}$	Drain current limiting	V_{IS} = 5 V	4	6	8	A
	Short circuit load protection					
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 5 V	-	*tbf*	-	J
	Overtemperature protection					
$T_{j(TO)}$	Threshold junction temperature	V_{IS} = 5 V	150	165	-	˚C

STATIC CHARACTERISTICS

T_b = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_D = 10 mA	50	55	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	V_{IS} = 0 V; I_{DM} = 200 mA; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	56	70	V
I_{DSS}	Off-state drain current	V_{DS} = 45 V; V_{IS} = 0 V	-	0.5	2	µA
I_{DSS}	Off-state drain current	V_{DS} = 50 V; V_{IS} = 0 V	-	1	20	µA
I_{DSS}	Off-state drain current	V_{DS} = 40 V; V_{IS} = 0 V; T_j = 100 ˚C	-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance[1]	V_{IS} = 5 V; I_{DM} = 1 A; $t_p \leq 300$ µs; $\delta \leq 0.01$	-	150	200	mΩ

INPUT CHARACTERISTICS

T_b = 25 ˚C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA		1.7	2.2	2.7	V
I_{IS}	Input supply current	normal operation;	V_{IS} = 5 V	-	330	450	µA
			V_{IS} = 4 V	-	170	270	µA
I_{ISL}	Input supply current	protection latched;	V_{IS} = 5 V	-	500	650	µA
			V_{IS} = 3.5 V	-	250	400	µA
V_{ISR}	Protection latch reset voltage[2]			1	2.2	3.5	V
$V_{(CL)IS}$	Input clamping voltage	I_I = 1.5 mA		6	7.5	-	V
R_{IG}	Input series resistance	to gate of power MOSFET		-	33	-	kΩ

SHADED BOXES

Values shown within shaded boxes are estimated for the objective specification.
These will not be fixed until the evaluation of prototype samples.

1 Continuous input voltage. The specified pulse width is for the drain current.

2 The input voltage below which the overload protection circuits will be reset.

MOUNTING INSTRUCTIONS

Dimensions in mm.

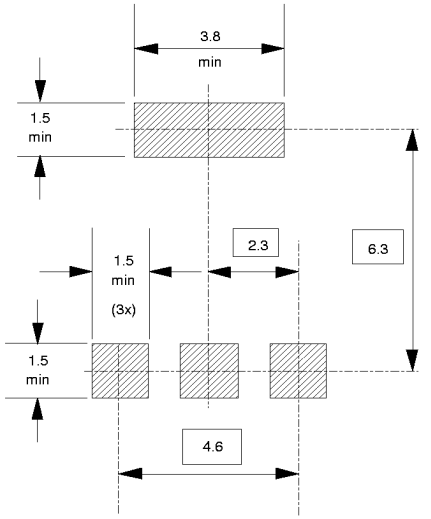


Fig.2. Soldering pattern for surface mounting.

PRINTED CIRCUIT BOARD

Dimensions in mm.

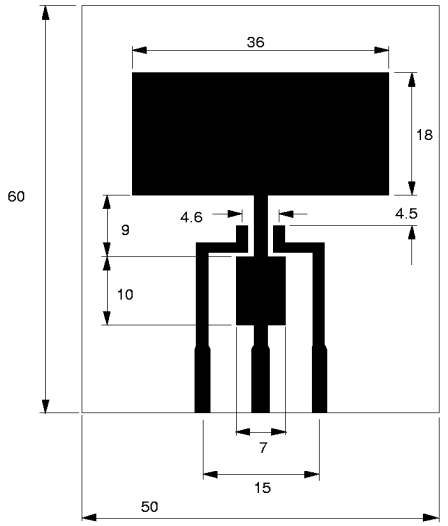


Fig.3. PCB for thermal resistance and power rating. PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

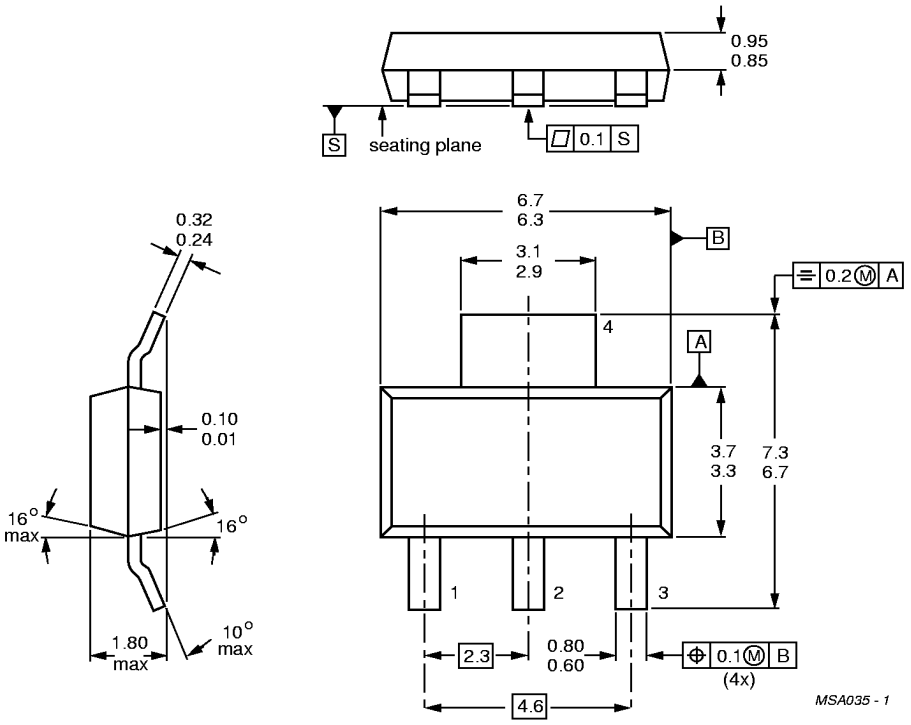


Fig.4. SOT223 surface mounting package[1].

1 For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8".