REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R049-93.	92-12-09	M. A. Frye
B	Updated boilerplate. Added device types 06-10. - glg	98-10-02	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	B	B	B	B	B	B	B	B	B	B	B									
SHEET	35	36	37	38	39	40	41	42	43	44	45									
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Rajesh Pithadia

APPROVED BY
Mike Frye

DRAWING APPROVAL DATE
92-11-09

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS
256K X 4 DYNAMIC RANDOM ACCESS
MEMORY (DRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-90617**

SHEET 1 OF 45

DSCC FORM 2233
APR 97

5962-E532-98

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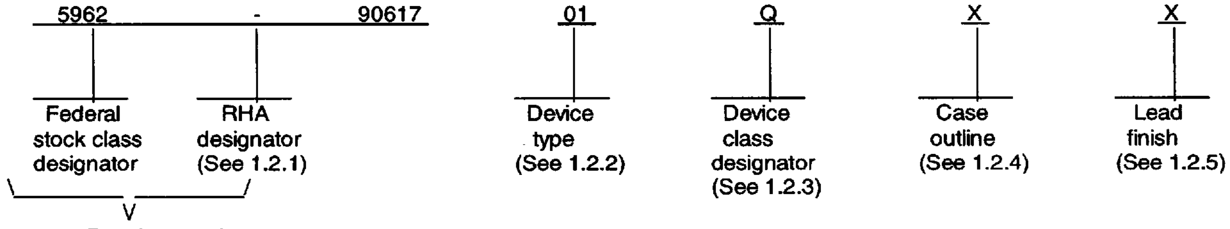
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01,06		256K x 4 dynamic random access memory	150 ns
02,07		256K x 4 dynamic random access memory	120 ns
03,08		256K x 4 dynamic random access memory	100 ns
04,09		256K x 4 dynamic random access memory	80 ns
05,10		256K x 4 dynamic random access memory	70 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
X	See figure 1	20	J-leaded small-outline
Y	See figure 1	20	Rectangular chip carrier
Z	See figure 1	20	Thin rectangular chip carrier
U	See figure 1	20	Flat pack
T	See figure 1	20	Zig-zag-in-line
N	See figure 1	20	Flat pack

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535 (see 6.6.1 and 6.6.2 herein).

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range on any pin	-1.0 V dc to 7.0 V dc
Input voltage range on V_{CC}	0 V dc to 7.0 V dc
Short circuit output current	50 mA
Maximum power dissipation (P_D)	1.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	See MIL-STD-1835
Case X	20°C/W
Case Y	20°C/W
Case Z	20°C/W
Case U	20°C/W
Case T	7.0°C/W
Case N	20°C/W
Junction temperature (T_J) 3/	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) 4/	+4.5 V dc to +5.5 V dc
High level input voltage range (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Low level input voltage range (V_{IL}) 5/	-1.0 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) .... 100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ All voltage values in this drawing are with respect to V_{SS}.
5/ The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this drawing for logic voltage levels only.

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STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

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3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

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4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$V_{CC} = 4.5\ V$, $I_{OH} = -5\ mA$, $V_{IL} = .8\ V$, $V_{IH} = 2.4\ V$	1,2,3	All	2.4		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5\ V$, $I_{OL} = 4.2\ mA$, $V_{IL} = .8\ V$, $V_{IH} = 2.4\ V$	1,2,3	All		0.4	V
Input leakage current	I_I	$V_I = 0\ V$ to $6.5\ V$, $V_{CC} = 5.0\ V$, All other pins = 0 V to V_{CC}	1,2,3	All		±10	µA
Output leakage current	I_O	$V_{CC} = 5.5\ V$, CAS high, $V_O = V_{CC}$ to 0 V	1,2,3	All		±10	µA
Power supply current read or write cycle	I_{CC1}	Minimum cycle, $V_{CC} = 5.5\ V$, Measured for a maximum of one address transition while $RAS = V_{IL}$	1,2,3	01,06		55	mA
				02,07		60	
				03,08		70	
				04,09		80	
				05,10		90	
Power supply current standby	I_{CC2}	After one memory cycle, RAS and CAS high, $V_{IH} = 2.4\ V$	1,2,3	All		4	mA
Power supply current average refresh (RAS-only or CBR)	I_{CC3}	$V_{CC} = 5.5\ V$, minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only) $\overline{RAS}$ low after $\overline{CAS}$ low (CBR), Measured for a maximum of one address transition while $RAS = V_{IL}$	1,2,3	01,06		55	mA
				02,07		60	
				03,08		70	
				04,09		80	
				05,10		90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current average page	I_{CC4}	$\overline{RAS}$ low, $\overline{CAS}$ cycling, t_{PC} = minimum, V_{CC} = 5.5 V, Measured for a maximum of one address transition while CAS = V_{IH}	1,2,3	01,06		35	mA
				02,07		45	
				03,08		50	
				04,09		60	
				05,10		70	
Input capacitance, address inputs	$C_I(A)$	f = 1 MHz see 4.4.1e, Bias on pins under test = 0 V	4	All		10	pF
Input capacitance, strobe inputs	$C_I(S)$		4	All		10	pF
Input capacitance, write-enable inputs	$C_I(W)$		4	All		10	pF
Output capacitance	C_O		4	All		10	pF
Access time from column address	$t_{a(CA)}$	See figures 4 and 5 1/	9,10,11	01,06		70	ns
				02,07		55	
				03,08		45	
				04,09		40	
				05,10		35	
Access time from CAS low	$t_{a(C)}$		9,10,11	01,06		40	ns
				02,07		30	
				03,08		25	
				04,09		20	
				05,10		20	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Access time from column precharge	$t_{a(CP)}$	See figures 4 and 5 1/	9,10,11	01,06		75	ns
				02,07		60	
				03,08		55	
				04,09		45	
				05,10		40	
Access time from RAS low	$t_{a(R)}$		9,10,11	01,06		150	ns
				02,07		120	
				03,08		100	
				04,09		80	
				05,10		70	
Access time from G low	$t_{a(G)}$		9,10,11	01,06		40	ns
				02,07		30	
				03,08		25	
				04,09		20	
				05,10		20	
Output diable time after CAS high 2/	$t_{dis(CH)}$		9,10,11	01,06		35	ns
				02,07		30	
				03,08		25	
				04,09		20	
				05,10		20	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output disable time after G high 2/	$t_{dis(G)}$	See figures 4 and 5 1/	9,10,11	01,06		35	ns
				02,07		30	
				03,08		25	
				04,09		20	
				05,10		20	
Cycle time read or write 3/	$t_{c(rd)}$ $t_{c(W)}$		9,10,11	01,06	260		ns
				02,07	220		
				03,08	190		
				04,09	150		
				05,10	130		
Cycle time read-write/ read-modify-write	$t_{c(rdW)}$		9,10,11	01,06		355	ns
				02,07		305	
				03,08		270	
				04,09		225	
				05,10		205	
Cycle time, pagemode read or write 4/	$t_{c(P)}$		9,10,11	01,06	80		ns
				02,07	65		
				03,08	55		
				04,09	50		
				05,10	45		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Cycle time, pagemode read-modify-write	$t_{c(PM)}$	See figures 4 and 5 4/	9,10,11	01,06	175		ns
				02,07	150		
				03,08	135		
				04,09	100		
				05,10	95		
Pulse duration, $\overline{\text{CAS}}$ low 5/	$t_{w(CL)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	18		
				All		10	µs
Pulse duration, page-mode, $\overline{\text{RAS}}$ low 6/	$t_{w(RL)P}$		9,10,11	01,06	0.15		µs
				02,07	0.12		
				03,08	0.10		
				04,09	0.08		
				05,10	0.07		
				All		100	
Pulse duration, non-page-mode, $\overline{\text{RAS}}$ low 6/	$t_{w(RL)}$		9,10,11	01,06	150		ns
				02,07	120		
				03,08	100		
				04,09	80		
				05,10	70		
				All		10	µs

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pulse duration, CAS high	$t_{w(CH)}$	See figures 4 and 5 1/	9,10,11	01,06	25		ns
				02,07	15		
				03,08	10		
				04,09	10		
				05,10	10		
Pulse duration, RAS high (precharge)	$t_{w(RH)}$		9,10,11	01,06	100		ns
				02,07	90		
				03,08	80		
				04,09	60		
				05,10	50		
Pulse duration, write	$t_{w(WL)}$		9,10,11	01,06	25		ns
				02,07	20		
				03,08	15		
				04,09	15		
				05,10	15		
Setup time, column-, address before CAS low	$t_{su(CA)}$		9,10,11	All	5		ns
Setup time, row-address before RAS low	$t_{su(RA)}$		9,10,11	All	0		ns
Setup time, data before W low 7/	$t_{su(D)}$		9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, read before CAS low	$t_{su(rd)}$	See figures 4 and 5 1/	9,10,11	All	0		ns
Setup time, $\overline{W}$ low before CAS high	$t_{su(WCH)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	18		
Setup time, $\overline{W}$ low before RAS high	$t_{su(WRH)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	18		
Setup time, $\overline{W}$ low before CAS low 8/	$t_{su(WCL)}$		9,10,11	All	0		ns
Setup time, $\overline{W}$ high before RAS low (CAS before RAS refresh) 9/	$t_{su(WRP)}$		9,10,11	06-10	10		ns
Hold time, $\overline{W}$ high from RAS low (CAS before RAS refresh) 9/	$t_{h(WRH)}$		9,10,11	06-10	10		ns
Hold time, column-address after CAS low 7/	$t_{h(CA)}$		9,10,11	01,06	35		ns
				02,07	20		
				03,08	20		
				04,09	20		
				05,10	15		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, data after CAS low 7/	$t_{h(D)}$	See figures 4 and 5 1/	9,10,11	01,06	30		ns
				02,07	25		
				03,08	20		
				04,09	15		
				05,10	15		
Hold time, data after RAS low 10/	$t_{h(RLD)}$		9,10,11	01,06	110		ns
				02,07	85		
				03,08	70		
				04,09	60		
				05,10	55		
Hold time, column address after RAS low 10/	$t_{h(RLCA)}$		9,10,11	01,06	100		ns
				02,07	80		
				03,08	70		
				04,09	60		
				05,10	55		
Hold time, row-address after RAS low	$t_{h(RA)}$		9,10,11	01,06	20		ns
				02,07	15		
				03,08	15		
				04,09	15		
				05,10	15		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time, read after CAS high 11/	$t_{h(CHrd)}$	See figures 4 and 5 1/	9,10,11	All	0		ns
Hold time, read after RAS high 11/	$t_{h(RHrd)}$		9,10,11	All	10		ns
Hold time, write after CAS low (early write operation only) 8/	$t_{h(CLW)}$		9,10,11	01,06	30		ns
				02,07	25		
				03,08	20		
				04,09	15		
				05,10	15		
Hold time, write after RAS low 10/	$t_{h(RLW)}$		9,10,11	01,06	105		ns
				02,07	90		
				03,08	75		
				04,09	70		
				05,10	70		
Delay time, column address to W low (read-write operation only) 12/	$t_{d(CAWL)}$		9,10,11	01,06	120		ns
				02,07	105		
				03,08	95		
				04,09	80		
				05,10	75		
Delay time, $\overline{CAS}$ high to RAS low	$t_{d(CHRL)}$		9,10,11	All	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ low to CAS high	$t_{d(RLCH)}$	See figures 4 and 5 1/	9,10,11	01,06	150		ns
				02,07	120		
				03,08	100		
				04,09	80		
				05,10	70		
Delay time, $\overline{CAS}$ low to RAS low (CAS-before-RAS refresh only) 13/	$t_{d(CLRL)R}$		9,10,11	01,06	15		ns
				02,07	15		
				03,08	10		
				04,09	10		
				05,10	10		
Hold time, $\overline{G}$ after W low	$t_{h(WLGL)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	18		
Delay time, $\overline{CAS}$ low to W low (Read-modify-write operation only)	$t_{d(CLWL)}$		9,10,11	01,06	90		ns
				02,07	80		
				03,08	70		
				04,09	60		
				05,10	50		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{RAS}$ low to column address 14/	$t_{d(RLCA)}$	See figures 4 and 5 1/	9,10,11	01,06	25	80	ns
				02,07	20	65	
				03,08	20	55	
				04,09	20	40	
				05,10	15	35	
Delay time, column address to $\overline{RAS}$ high 15/	$t_{d(CARH)}$		9,10,11	01,06	70		ns
				02,07	55		
				03,08	45		
				04,09	40		
				05,10	35		
Delay time, column address to $\overline{CAS}$ high 15/	$t_{d(CACH)}$		9,10,11	01,06	70		ns
				02,07	55		
				03,08	45		
				04,09	40		
				05,10	35		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low 14/	$t_{d(RLCL)}$		9,10,11	01,06	30	110	ns
				02,07	30	90	
				03,08	30	75	
				04,09	30	60	
				05,10	25	50	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{CAS}$ low to RAS high	$t_{d(CLRH)}$	See figures 4 and 5 1/	9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	25		
				05,10	25		
Delay time, $\overline{RAS}$ high $\overline{CAS}$ low (CAS before RAS refresh only) 13/	$t_{d(RHCL)R}$		9,10,11	All	0		ns
Delay time, $\overline{RAS}$ low to W low (Read-modify-write operation only) 12/	$t_{d(RLWL)}$		9,10,11	01,06	200		ns
				02,07	170		
				03,08	150		
				04,09	130		
				05,10	120		
Delay time, $\overline{G}$ high before data at DQ	$t_{d(GHD)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	20		
Delay time, $\overline{G}$ low to RAS high 15/	$t_{d(GLRH)}$		9,10,11	01,06	40		ns
				02,07	30		
				03,08	25		
				04,09	20		
				05,10	20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, RAS low to CAS high (CAS before RAS refresh only) 13/	$t_{d(RLCH)R}$	See figures 4 and 5 1/	9,10,11	01,06	30		ns
				02,07	25		
				03,08	25		
				04,09	20		
				05,10	15		
Refresh time interval	t_{rf}		9,10,11	All		8	ms

1/ System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.
2/ $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven. The outputs are disabled by bringing either G or CAS high.
3/ All cycle times assume t_T = 5 ns.
4/ To guarantee $t_{c(P)}$ minimum, $t_{su(CA)}$ should be greater than or equal to $t_{w(CH)}$.
5/ In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Additional CAS low time $t_{w(CL)}$ may be required, depending on the user's transition times.
6/ In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Additional RAS low time $t_{w(RL)}$ may be required, depending on the user's transition times.
7/ Referenced to the later of CAS or W in write operations.
8/ Early write operation only.
9/ These tests are applicable to device types 06 - 10 only.
10/ The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ minimum as a reference.
11/ Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
12/ Read-modify-write operation only.
13/ CAS-before-RAS refresh only.
14/ Maximum value specified only to guarantee access time.
15/ This parameter may not be tested, but shall be guaranteed to the limits specified in table I and is included to help with device application.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)		Subgroups (in accordance with MIL-PRF-38535, table III)
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 1, 2,8A,10
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIB). Delta measurements are not required if the manufacturer has provided data and that data has been approved by the qualifying activity.

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TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC2} standby	±400 μA
I_I, I_O	±1.0 μA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

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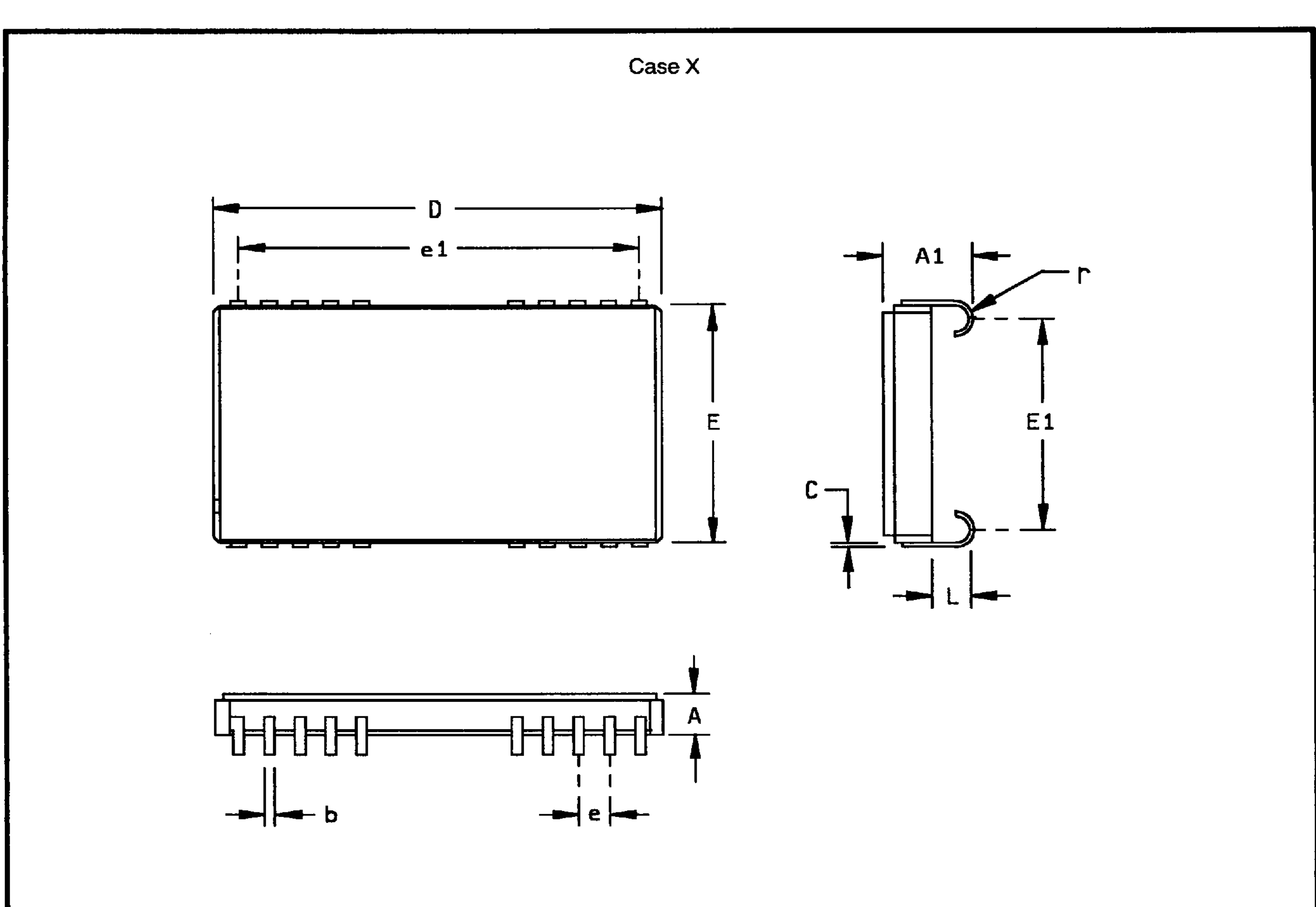
Case X



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Symbol	Inches min.	Inches max.	Millimeters min.	Milimeters max.
A	.080	.100	2.03	2.54	e1	.590	.610	14.99	15.49
A1	.120	.140	3.04	3.56	E	.320	.340	8.13	8.64
b	.016	.023	0.41	0.58	E1	.270	.305	6.86	7.75
C	.006	.012	0.15	0.30	r	.025	.035	0.64	0.89
D	.665	.685	16.89	17.40	L	.035	.045	0.89	1.14
e	.045	.055	1.14	1.40	N	20			

FIGURE 1. Case outlines.

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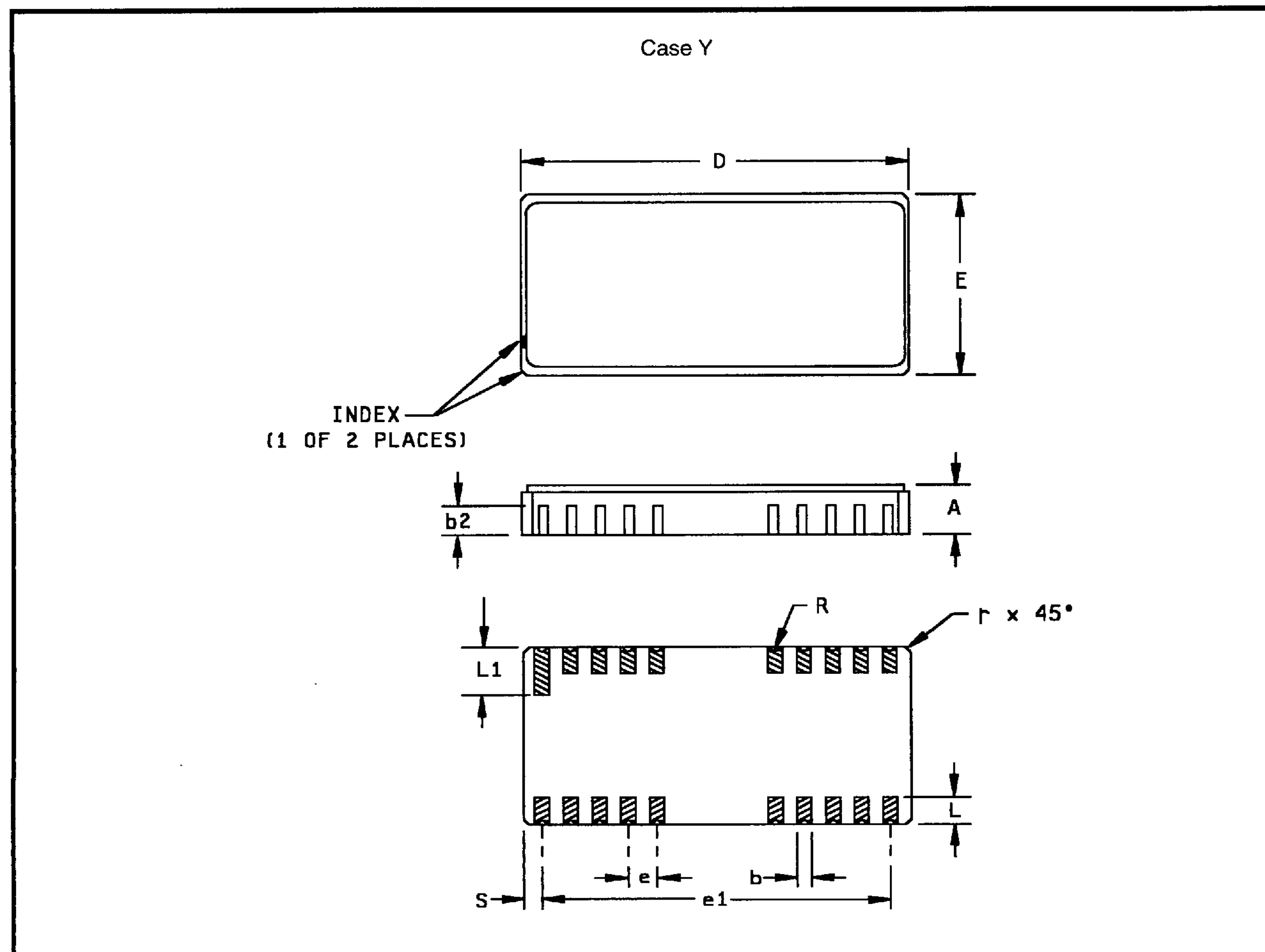
Case Y



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Symbol	Inches min.	Inches max.	Millimeters min.	Milimeters max.
A	.064	.092	2.03	2.54	e1	.590	.610	14.98	15.49
b	.022	.028	3.04	3.56	L	.045	.055	1.14	1.40
b2	.035 ref.		0.89 ref.		L1	.080	.100	2.03	2.54
D	.665	.685	16.89	17.40	r	.010 ref.		0.25 ref.	
E	.343	.357	8.71	9.07	R	.008 typ.		0.20 typ.	
e	.050 typ.		1.27 typ.		S	.028	.048	0.71	1.22

FIGURE 1. Case outlines - Continued.

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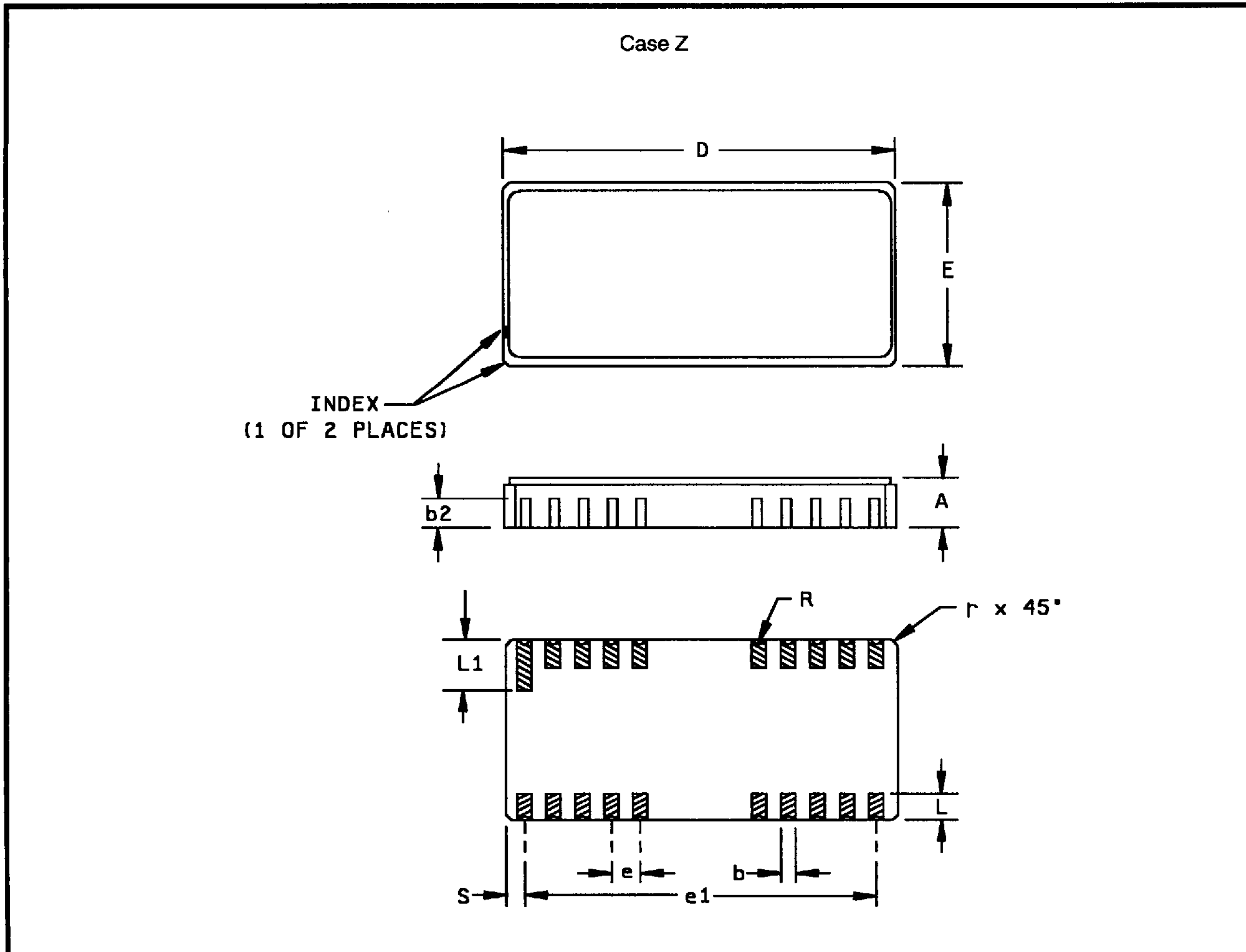
Case Z



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Symbol	Inches min.	Inches max.	Millimeters min.	Milimeters max.
A	.060	.080	1.27	1.52	e1	.590	.610	14.98	15.49
b	.022	.028	3.04	3.56	L	.045	.055	1.14	1.40
b2	.035 ref.		0.89 ref.		L1	.080	.100	2.03	2.54
D	.665	.685	16.89	17.40	r	.010 ref.		0.25 ref.	
E	.343	.357	8.71	9.07	R	.008 typ.		0.20 typ.	
e	.050 typ.		1.27 typ.		S	.028	.048	0.71	1.22

FIGURE 1. Case outlines - Continued.

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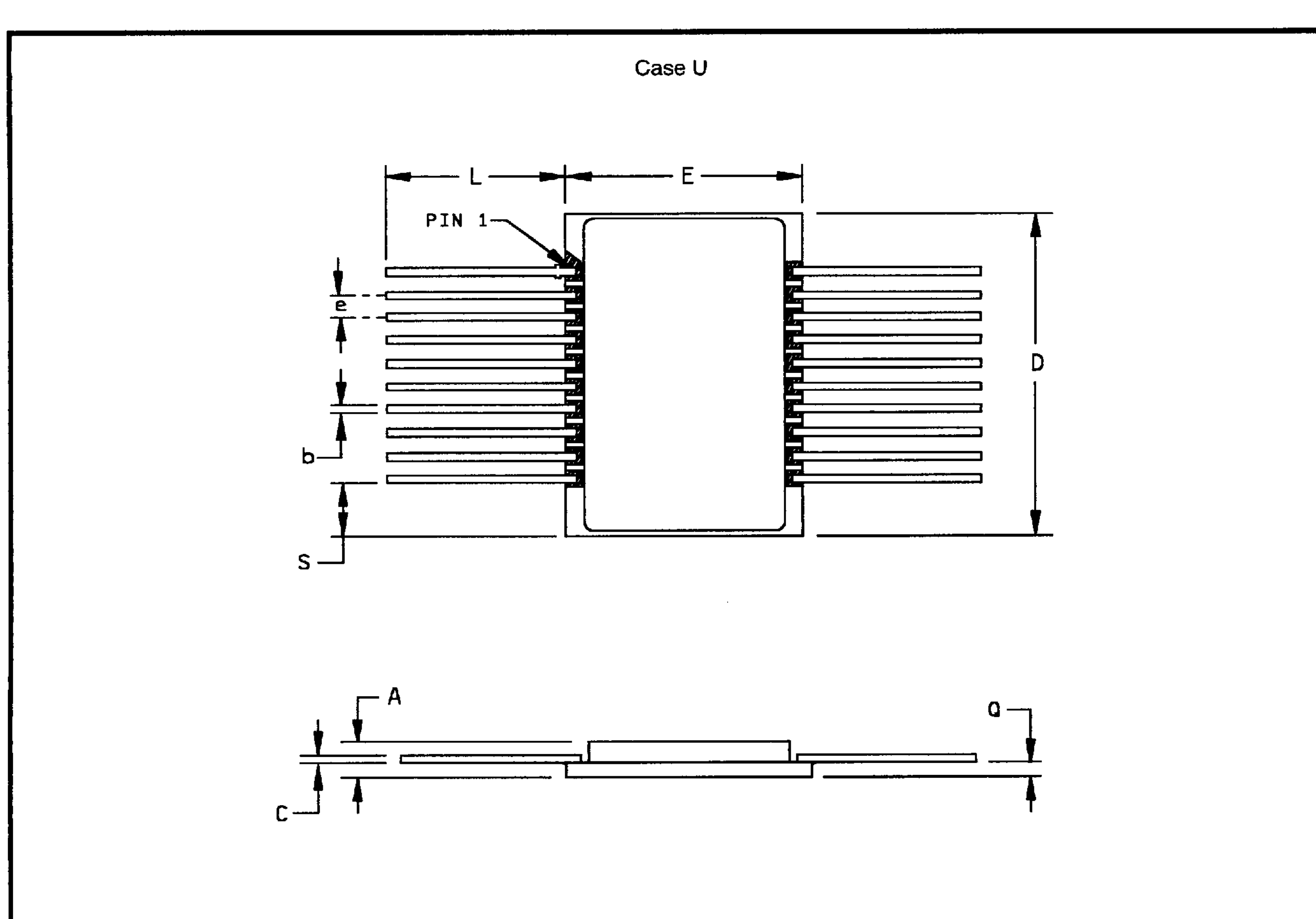
Case U



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Symbol	Inches min.	Inches max.	Millimeters min.	Milimeters max.
A	.075	.095	1.90	2.41	e	.050 typ.		1.27 typ.	
b	.015	.021	0.38	0.53	L	.295	.315	7.49	8.00
C	.004	.010	0.10	0.25	Q	.025	.035	0.64	0.89
D	.660	.680	16.77	17.27	S	.095	.109	2.41	2.77
E	.373	.387	9.47	9.83	N	20			

FIGURE 1. Case outlines - Continued.

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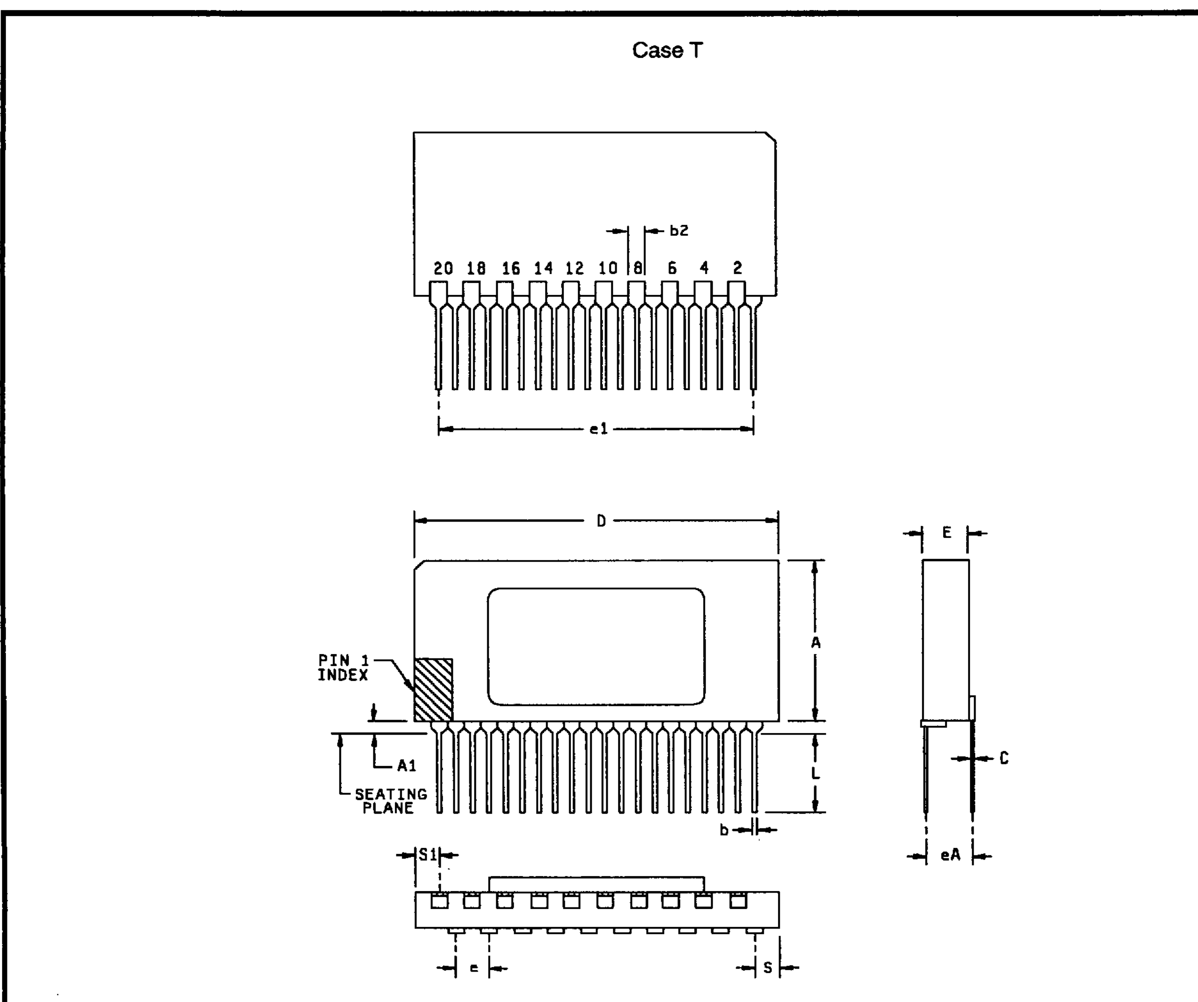
Case T



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Symbol	Inches min.	Inches max.	Millimeters min.	Milimeters max.
A	.355	.405	9.01	10.29	e	.100 typ.		2.54 typ.	
A1	.015	.050	0.38	1.27	e1	.890	.910	22.60	23.11
b	.016	.023	0.41	0.58	eA	.085	.115	2.15	2.92
b2	.035	.070	0.89	1.78	L	.125	.200	3.18	5.08
C	.008	.015	0.20	0.38	S	.040	.060	1.02	1.52
D	1.035	1.065	26.29	27.05	S1	.040	.060	1.02	1.52
E	.100	.120	2.54	3.05	N	20			

FIGURE 1. Case outlines - Continued.

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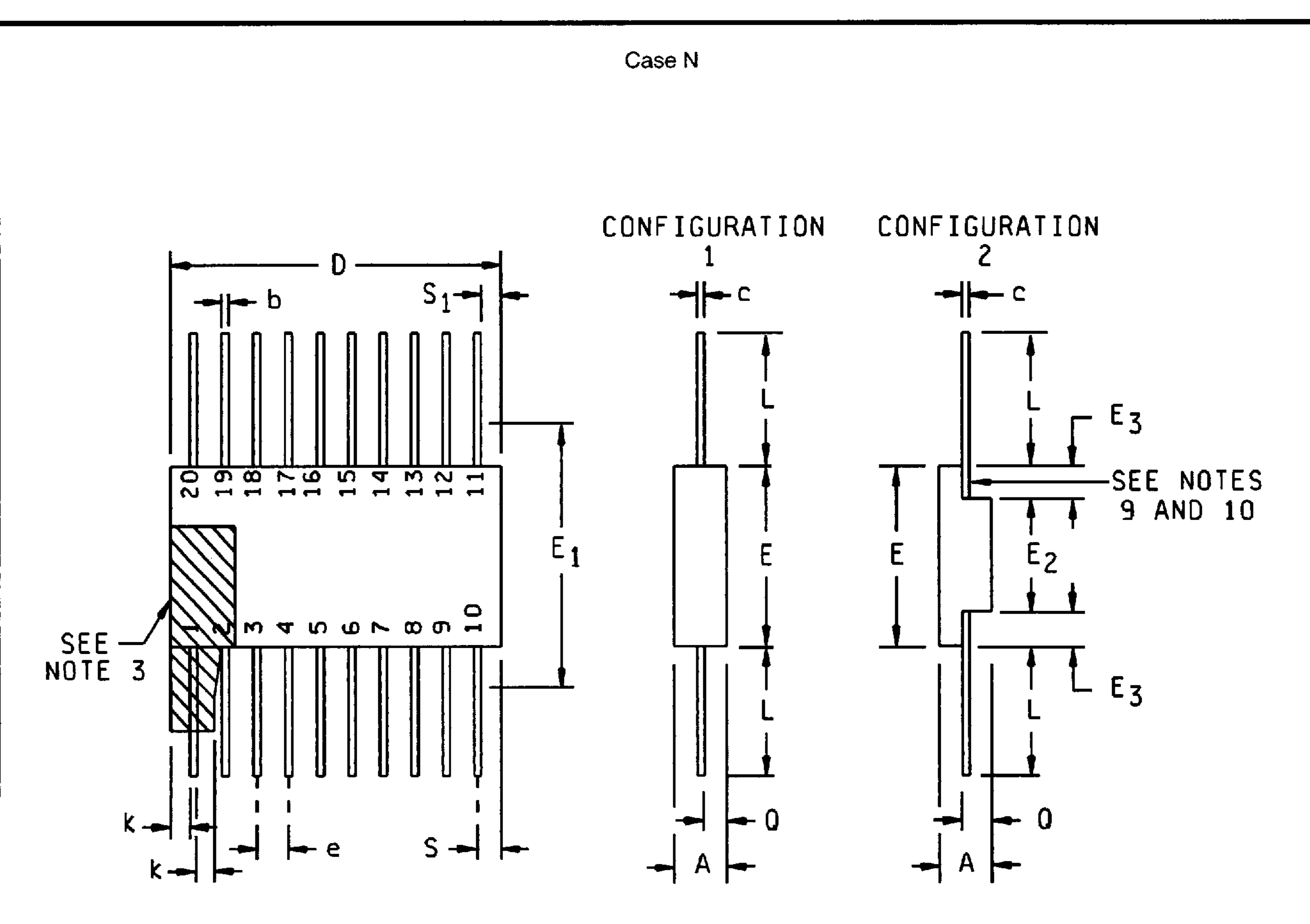
Case N



Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Notes	Symbol	Inches min.	Inches max.	Millimeters min.	Millimeters max.	Notes
A	.045	.105	1.14	2.67	---	E_3	.030	---	0.76	---	---
b	.015	.019	0.38	0.48	7	e	.050 BSC		1.27 BSC		6, 8
c	.003	.006	0.08	0.15	7	k	.008	.015	0.20	0.38	12
D	---	.640	---	16.26	5	L	.250	.370	6.35	9.40	---
D_1	---	.530	---	13.46	5	Q	.026	.040	0.66	1.02	4
E	.360	.420	9.14	10.67	---	S	---	.095	---	2.41	9
E_1	---	.440	---	11.18	5	S_1	.005	---	0.13	---	10
E_2	.180	---	4.57	---	---	α	30°	90°	30°	90°	13

FIGURE 1. Case outlines - Continued.

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Case N

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one. This tab may be located on either side as shown.
4. Dimension Q shall be measured at the point of exit of the lead from the body. Dimension Q shall be .0085 (0.215 mm) minimum when lead finish A is applied.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located with ±.005 (0.13 mm) of its exact longitudinal position relative to pins 1 and 20.
7. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
8. Eighteen spaces.
9. Applies to all four corners (leads number 1, 10, 11, and 20 for configurations 1 and 2 and leads 2, 9, 12, and 19 for configuration 3).
10. Dimension S_1 may be .000 (0.00 mm) if leads number 1, 10, 11, and 20 for configurations 1 and 2 and leads number 2, 9, 12, and 19 for configuration 3 bend toward the cavity of the package within one lead's width from the point of entry of the lead into the body.
11. Optional configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
12. Optional, see note 3. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension K does not apply.
13. Lead configuration is optional within dimension E, except when dimensions B and C apply.

FIGURE 1. Case outlines - Continued.

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Device types	All device types		
Case outlines	R, U, and N	X, Y, and Z	T
Terminal number	Terminal symbol		
1	D/Q_1	D/Q_1	$\overline{G}$
2	D/Q_2	D/Q_2	$\overline{CAS}$
3	$\overline{W}$	$\overline{W}$	D/Q_3
4	$\overline{RAS}$	$\overline{RAS}$	D/Q_4
5	NU	NU	V_{SS}
6	A_0	NP	D/Q_1
7	A_1	NP	D/Q_2
8	A_2	NP	$\overline{W}$
9	A_3	A_0	$\overline{RAS}$
10	V_{CC}	A_1	NU
11	A_4	A_2	A_0
12	A_5	A_3	A_1
13	A_6	V_{CC}	A_2
14	A_7	A_4	A_3
15	A_8	A_5	V_{CC}
16	$\overline{G}$	A_6	A_4
17	$\overline{CAS}$	A_7	A_5
18	D/Q_3	A_8	A_6
19	D/Q_4	NP	A_7
20	V_{SS}	NP	A_8
21	---	NP	---
22	---	$\overline{G}$	---
23	---	$\overline{CAS}$	---
24	---	D/Q_3	---
25	---	D/Q_4	---
26	---	V_{SS}	---

NP = no pin
NU = no external connection is allowed

FIGURE 2. Terminal connections.

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Operation	Inputs					Input		Output
	RAS	CAS	W	G	Row address	Column address	D	Q
Read	ACT	ACT	NAC	ACT	APD	APD	NAC	VLD
Write (early write)	ACT	ACT	ACT	DNC	APD	APD	APD	ILD
Write (late write)	ACT	ACT	ACT	NAC	APD	APD	APD	ILD (see note 1)
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD (see note 1)
RAS-only refresh	ACT	NAC	DNC	DNL	APD (see note 2)	DNC	DNC	HIZ
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	NAC	VLD
CAS before RAS refresh	ACT	ACT	DNC NAC 3/	DNC	DNC	DNC	DNC	HIZ
Standby	NAC	NAC	DNC	DNC	DNC	DNC	DNC	HIZ

ACT = Active
NAC = Nonactive
DNC = Don't care
VLD = Valid
ILD = Invalid
APD = Applied
HIZ = High impedance state

NOTES:

1. Output may go from high impedance to an invalid data state prior to the specified access time as the output is driven when CAS goes low.
2. A10 is a don't care.
3. For device types 06 - 10 only, upon power-up, the user must execute eight (8) RAS-ONLY-REFRESH or eight (8) CBR-REFRESH (W-HIGH) cycles. Either of these RAS cycling methods is mandatory, otherwise proper device operation will not be achieved.

FIGURE 3. Truth table.

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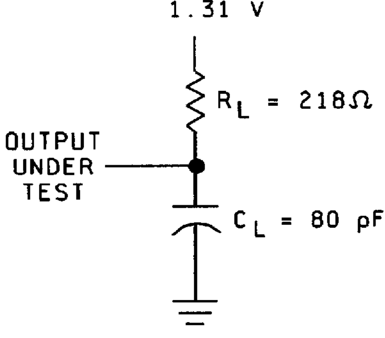
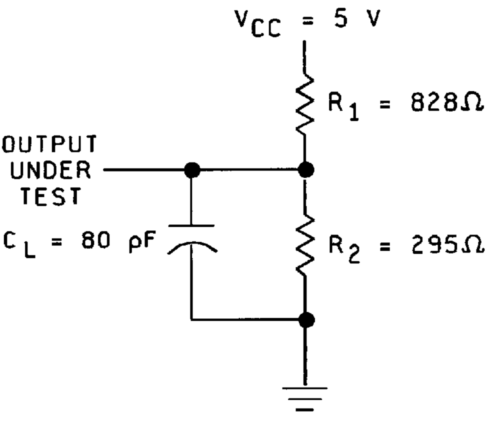


(a) LOAD CIRCUIT



(b) ALTERNATE LOAD CIRCUIT

NOTE: Transition times (t_r, t_F) for $\overline{RAS}$ and $\overline{CAS}$ are 3 through 50 ns.

FIGURE 4. Load circuits.

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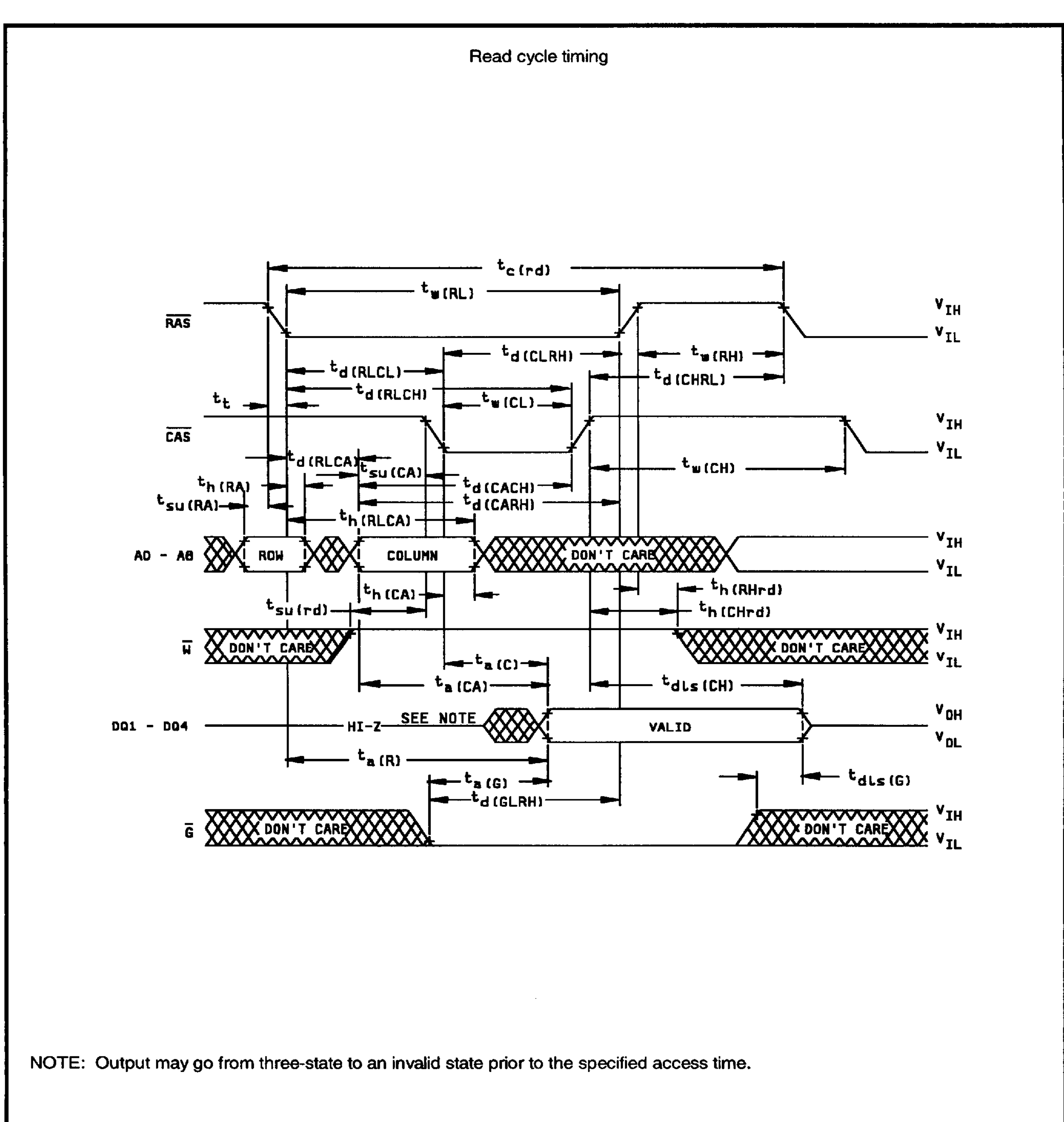
Read cycle timing



NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wavwform diagrams.

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Early write cycle timing

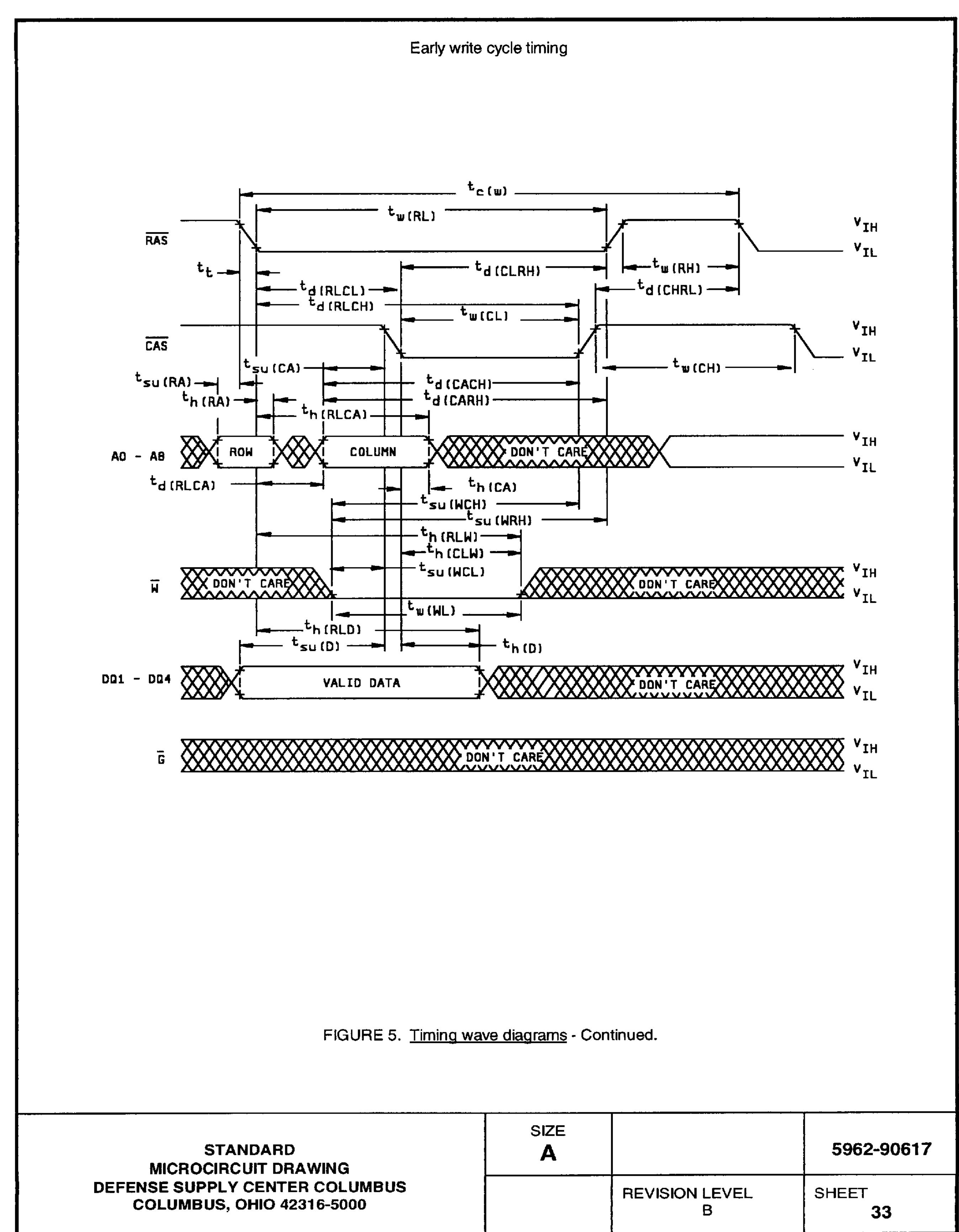

FIGURE 5. Timing wave diagrams - Continued.

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Write cycle timing

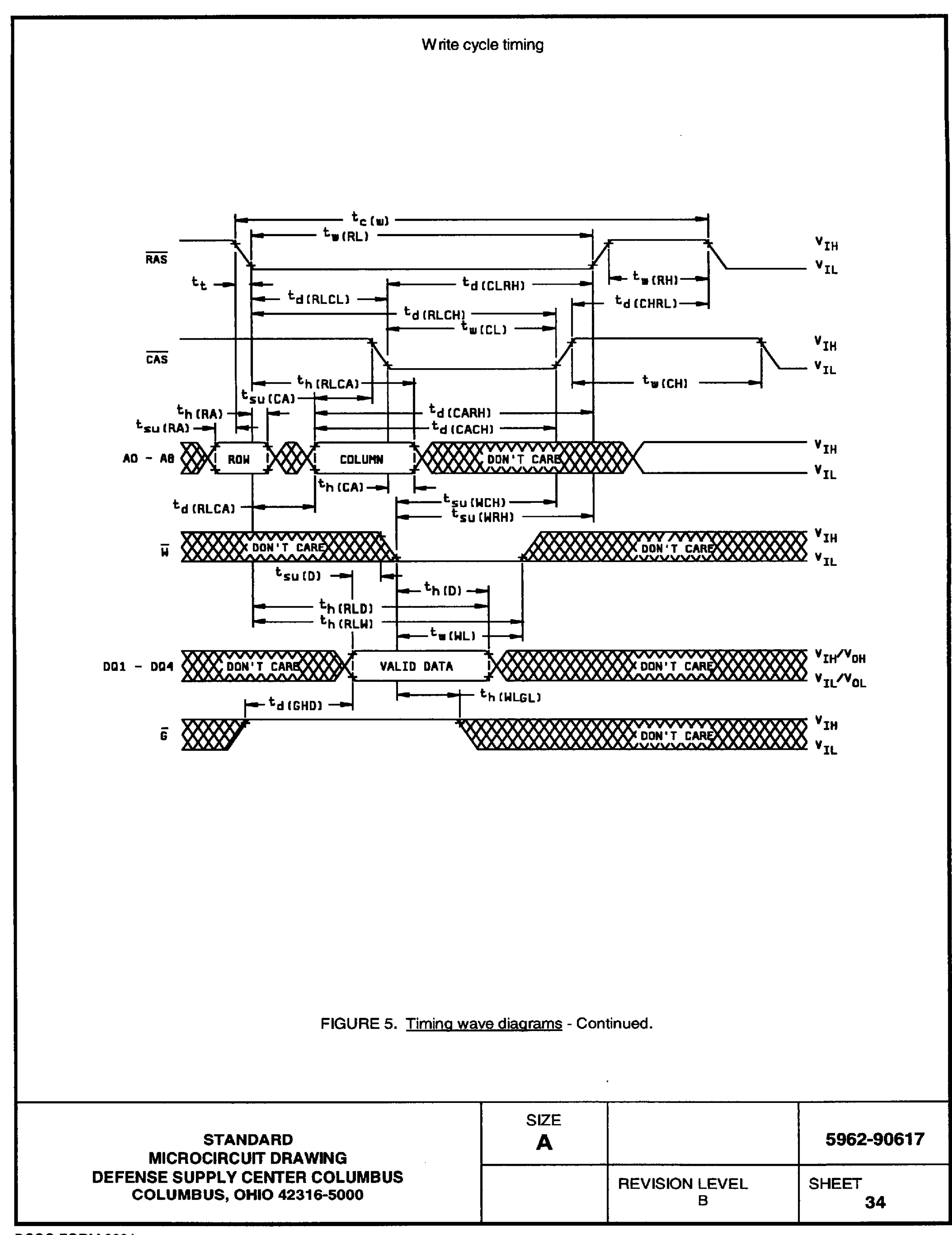

FIGURE 5. Timing wave diagrams - Continued.

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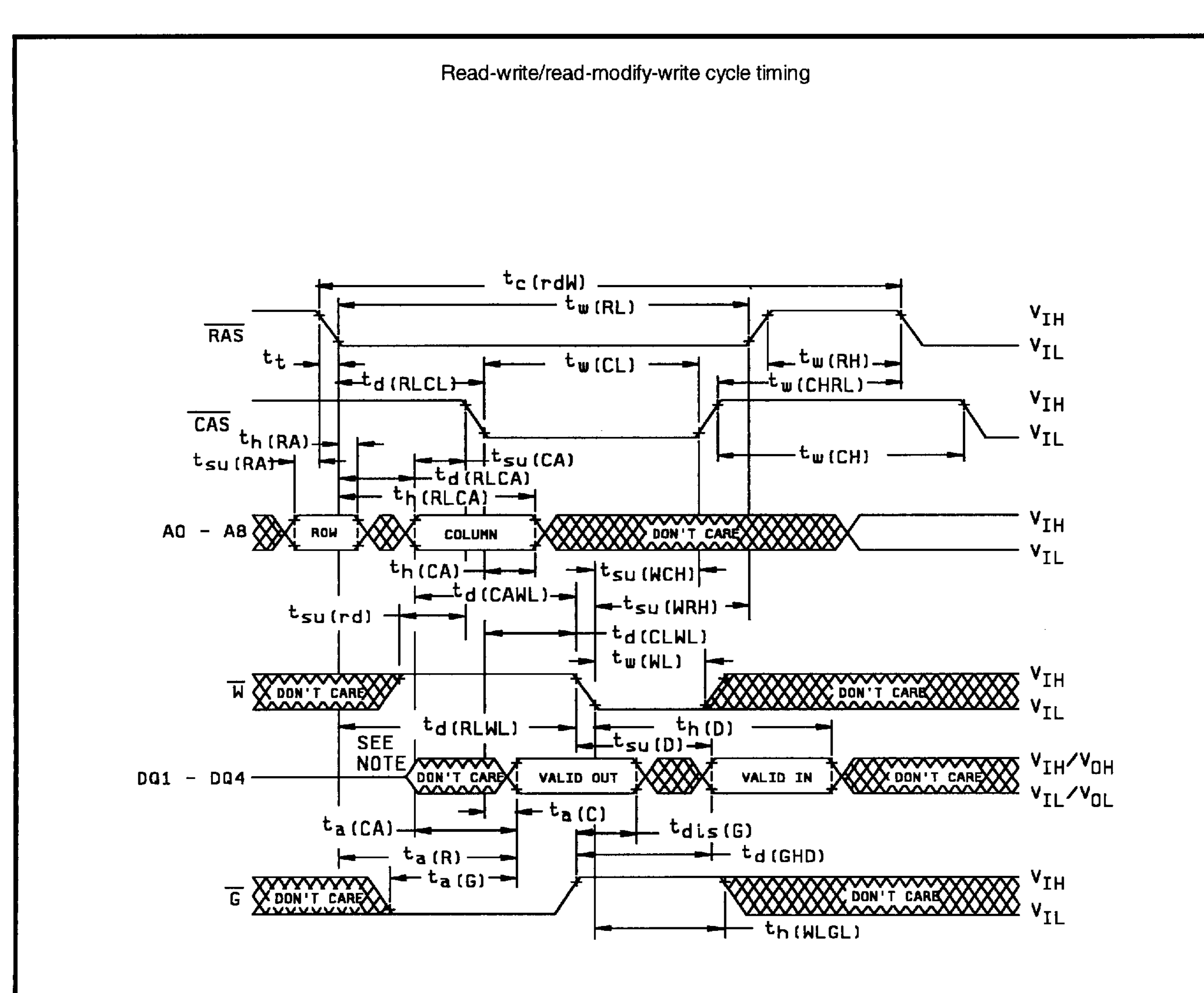
Read-write/read-modify-write cycle timing



NOTE: Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wave diagrams - Continued.

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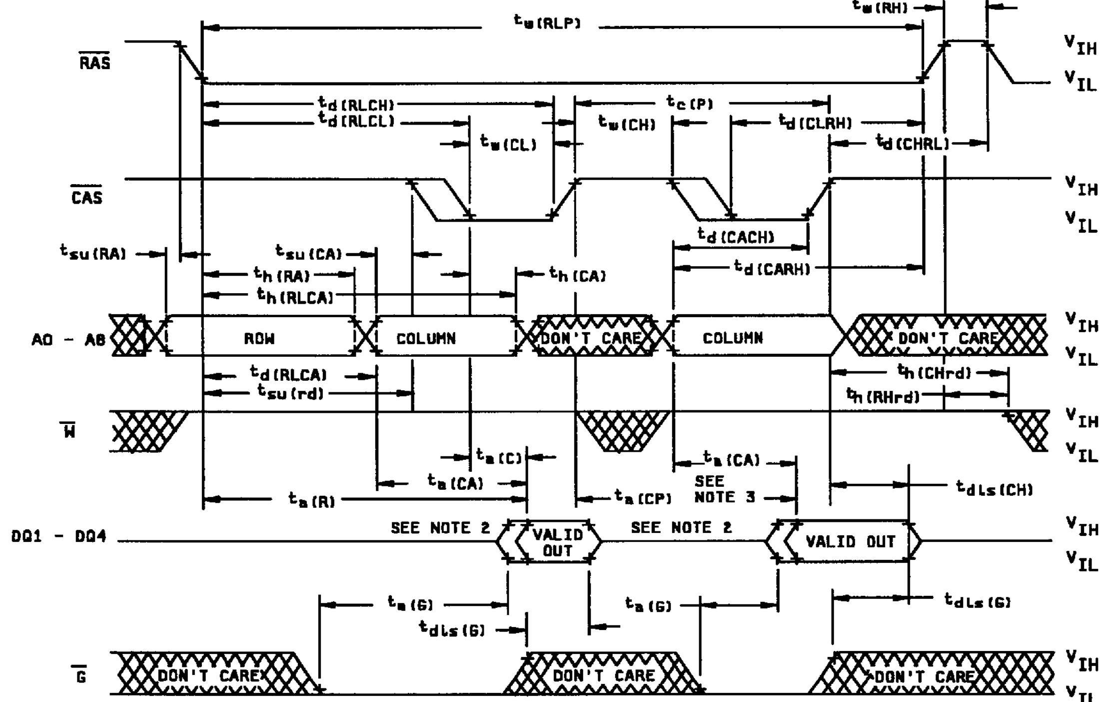
Enhanced page-mode read cycle timing
(see note 1)



NOTES:

1. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
2. Output may go from three-state to an invalid state prior to the specified access time.
3. Access time is $ta_{(CP)}$ or $ta_{(CA)}$ dependent.

FIGURE 5. Timing wave diagrams - Continued.

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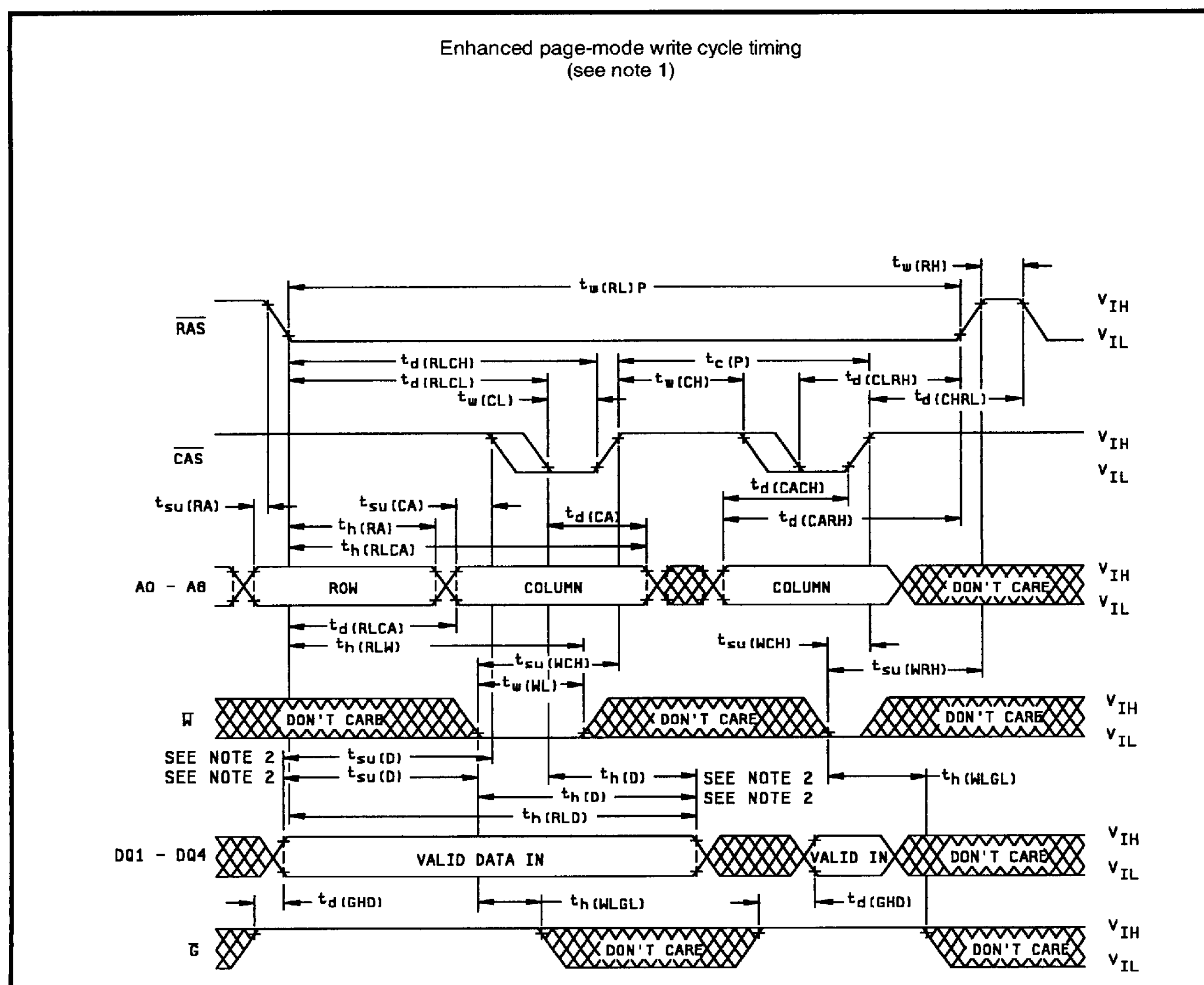
Enhanced page-mode write cycle timing
(see note 1)



NOTES:

1. A read cycle or a read-write cycle can be intermixed with write cycle as long as the read and read-write timing specification are not violated.
2. t_{DS} and t_{DH} are referenced to CAS or W, whichever occurs last.

FIGURE 5. Timing wave diagrams - Continued.

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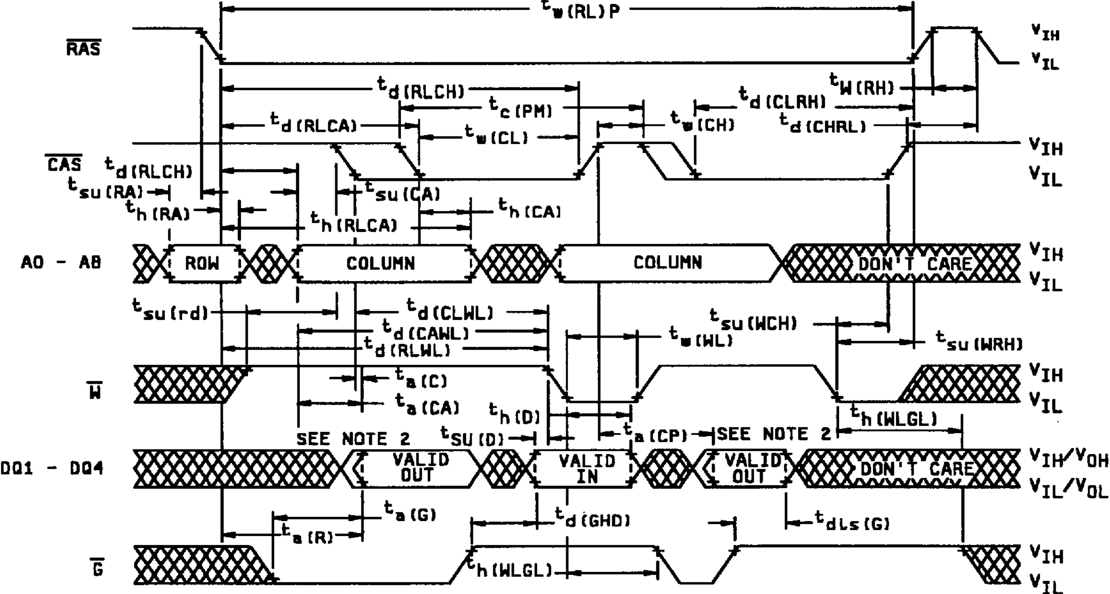
Enhanced page-mode read-write cycle timing
(see note 1)



NOTES:

1. A read or read-write cycle can be intermixed with read-write cycles as long as the read and write timing specification are not violated.
2. Output may go from three-state to an invalid state prior to the specified access time.

FIGURE 5. Timing wave diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE A		5962-90617
		REVISION LEVEL B	SHEET 38

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APR 97

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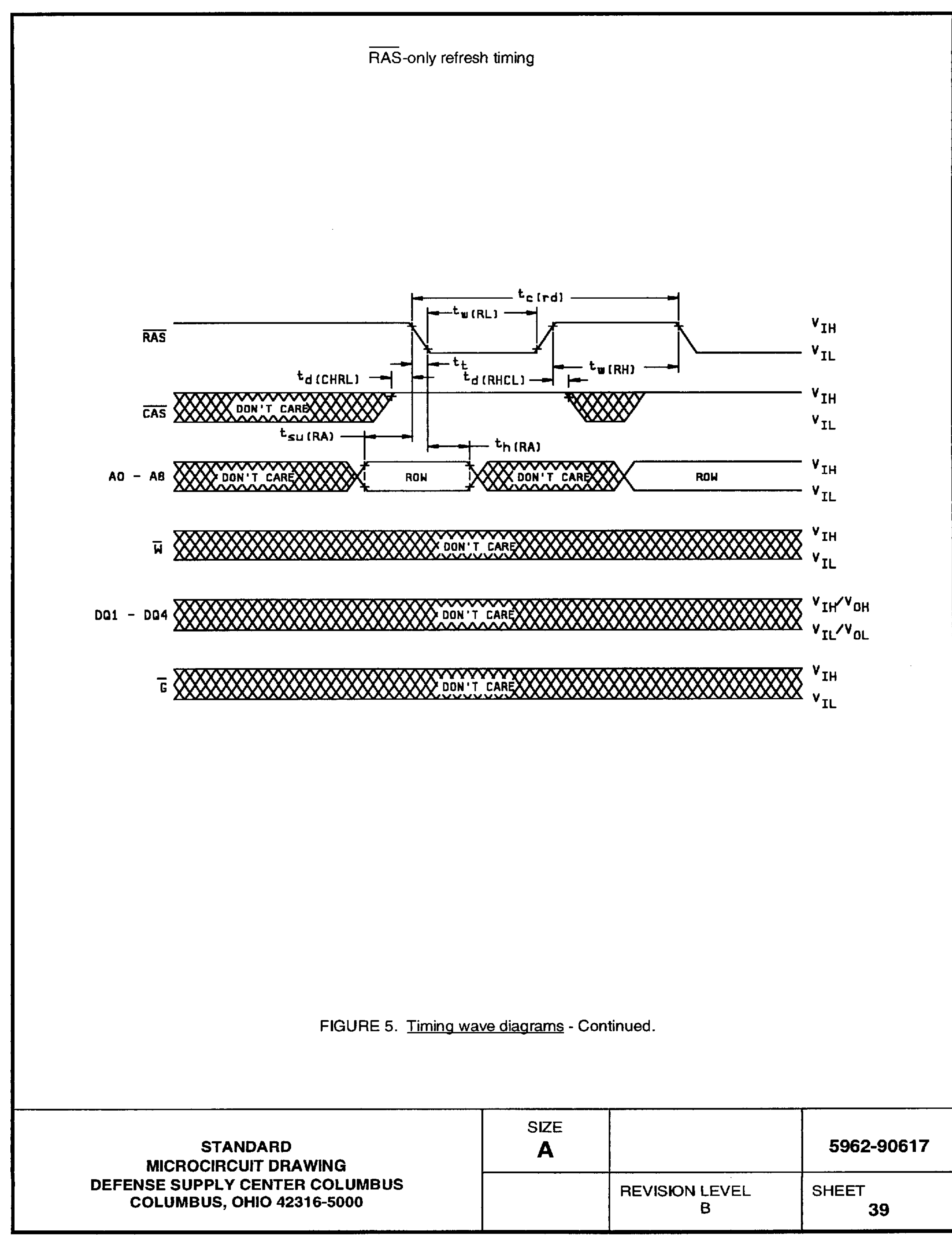

FIGURE 5. Timing wave diagrams - Continued.

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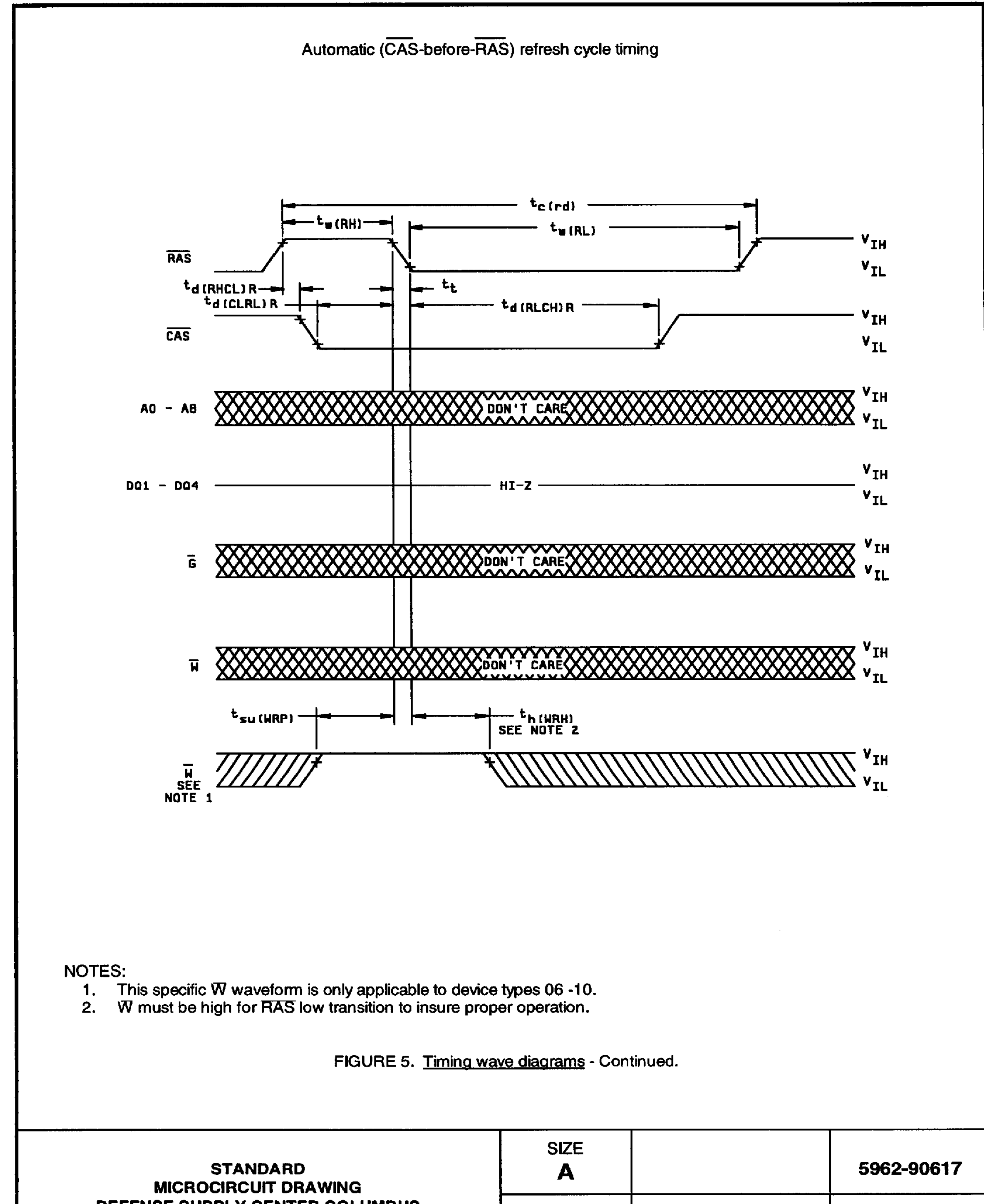
Automatic (CAS-before-RAS) refresh cycle timing



NOTES:
1. This specific W waveform is only applicable to device types 06 -10.
2. W must be high for RAS low transition to insure proper operation.

FIGURE 5. Timing wave diagrams - Continued.

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Hidden refresh cycle (enhanced page mode)

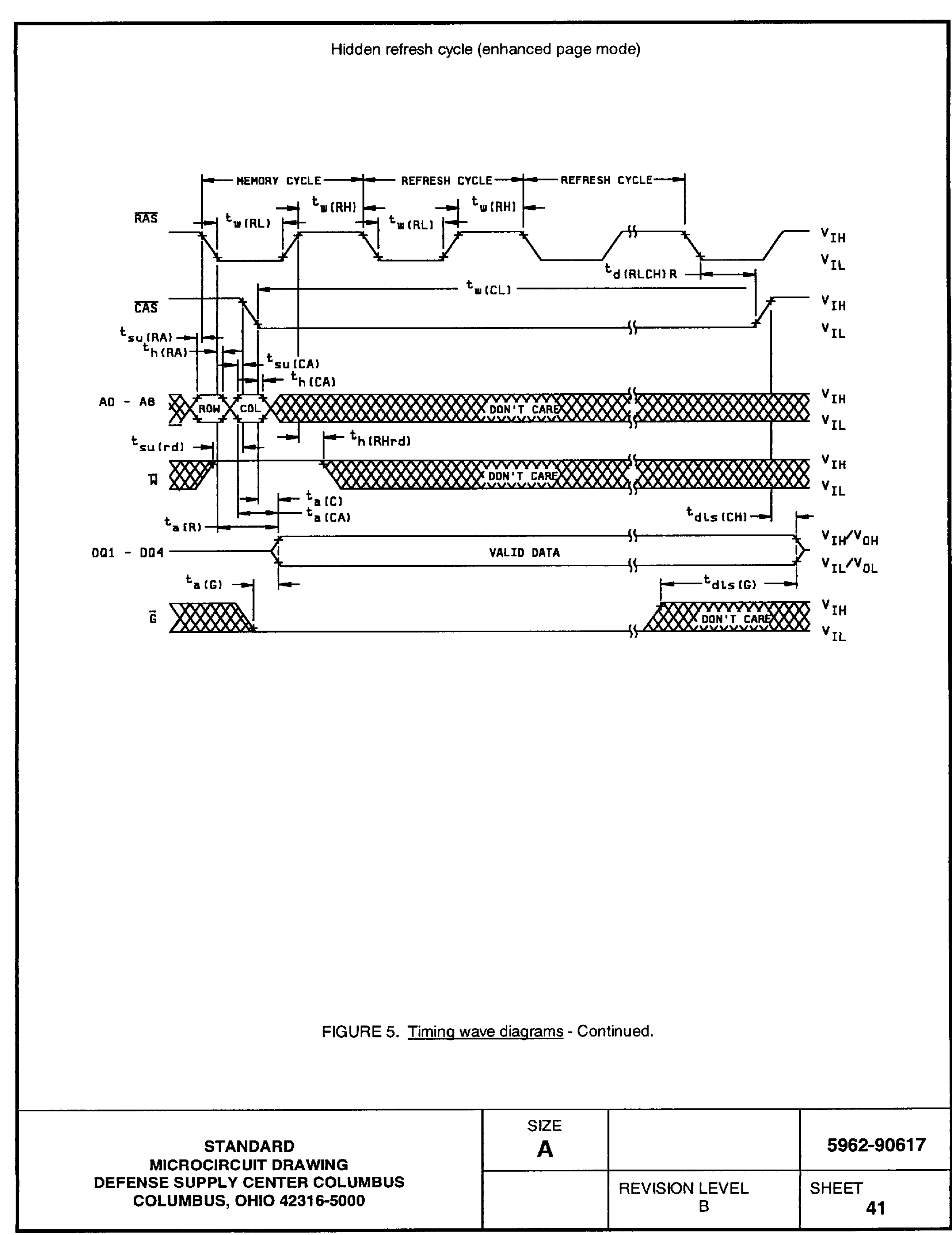

FIGURE 5. Timing wave diagrams - Continued.

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e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_{IN} .... Input terminal capacitance.
C_{OUT} .... Output and bidirectional output terminal capacitance.
GND .... Ground zero voltage potential.
I_{CC} .... Supply current.
I_I .... Input current.
I_O .... Output current.
T_C .... Case temperature.
V_{CC} .... Positive supply voltage.

6.5.1 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
(valid)	MUST BE VALID	WILL BE VALID
(H to L)	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
(L to H)	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
(don't care)	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
(high impedance)		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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APPENDIX

FUNCTIONAL ALGORITHMS 1/

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance (t_{OFF}). This pattern verifies the output buffer switches to high impedence (three-state) within the specified t_{OFF} after the rise of CAS. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise CAS and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after t_{OFF} delay.

30.2 Algorithm B (pattern 2).

30.2.1 V_{CC} slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and $\overline{\text{writing}}$. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with V_{CC} at 5.0 V.
Step 3: Change V_{CC} to 4.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change V_{CC} to 5.5 V.
Step 7: Read memory with background data complement.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat steps 9 and 10 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

1/ For device types 06 - 10 only, a 1MEG x 4 die is used and bonded out to produce a 256K x 4 array. Therefore, it is not possible to apply a true topologically pure algorithm. For details regarding testing to verify proper device operation in lieu of functional algorithms, contact the supplying vendor.

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30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with checkerboard data.
Step 3: Pause T_{REF} (stop all clocks).
Step 4: Read memory with checkerboard data.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 3 and 4 using data complement.
Step 6: Read memory with data for all address locations.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with checkerboard data using Page mode cycle.
Step 3: Read first page of memory with checkerboard data using Page mode cycle.
Step 4: Repeat steps 2 and 3 for remaining memory locations.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load one column of memory with background data.
Step 3: Using CAS before RAS cycle read one column of data and load with data complement using RMW cycle using the internally generated row address.
Step 4: Repeat step 3 using data complement.
Step 5: Read one column of data from memory.

30.8 Algorithm H (pattern 8).

30.8.1 $\overline{\text{RAS}}$-only refresh test. This test is used to verify the functionality of the $\overline{\text{RAS}}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 RAS-only cycles while attempting to modify data.
Step 4: Repeat step 3 for 100 ms.
Step 5: Read memory with background data.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-10-02

Approved sources of supply for SMD 5962-90617 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535 .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9061701MRA	01295	SMJ44C256-15JDM
	3/	MT4C4256C-15883C
5962-9061701MXA	01295	SMJ44C256-15HJM
5962-9061701MYA	01295	SMJ44C256-15FQM
	3/	MT4C4256EC-15883C
5962-9061701MZA	4/	SMJ44C256-15HLM
5962-9061701MUA	4/	SMJ44C256-15HKM
5962-9061701MTA	3/	MT4C4256CZ-15883C
5962-9061701MNA	3/	MT4C4256F-15883C
5962-9061702MRA	01295	SMJ44C256-12JDM
	3/	MT4C4256C-12883C
5962-9061702MXA	01295	SMJ44C256-12HJM
5962-9061702MYA	01295	SMJ44C256-12FQM
	3/	MT4C4256EC-12883C
5962-9061702MZA	4/	SMJ44C256-12HLM
5962-9061702MUA	4/	SMJ44C256-12HKM
5962-9061702MTA	3/	MT4C4256CZ-12883C
5962-9061702MNA	3/	MT4C4256F-12883C
5962-9061703MRA	01295	SMJ44C256-10JDM
	3/	MT4C4256C-10883C
5962-9061703MXA	01295	SMJ44C256-10HJM
5962-9061703MYA	01295	SMJ44C256-10FQM
	3/	MT4C4256EC-10883C
5962-9061703MZA	4/	SMJ44C256-10HLM
5962-9061703MUA	4/	SMJ44C256-10HKM
5962-9061703MTA	3/	MT4C4256CZ-10883C
5962-9061703MNA	3/	MT4C4256F-10883C
5962-9061704MRA	01295	SMJ44C256-80JDM
	3/	MT4C4256C-883C
5962-9061704MXA	3/	SMJ44C256-80HJM
5962-9061704MYA	01295	SMJ44C256-80FQM
	3/	MT4C4256EC-883C
5962-9061704MZA	4/	SMJ44C256-80HLM

See footnote at end of list.

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Standardized military drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9061704MUA	4/	SMJ44C256-80HKM
5962-9061704MTA	3/	MT4C4256CZ-883C
5962-9061704MNA	3/	MT4C4256F-883C
5962-9061705MRA	01295	SMJ44C256-70JDM
	3/	MT4C4256C-70883C
5962-9061705MXA	01295	SMJ44C256-70HJM
5962-9061705MYA	01295	SMJ44C256-70FQM
	3/	MT4C4256EC-70883C
5962-9061705MZA	4/	SMJ44C256-70HLM
5962-9061705MUA	4/	SMJ44C256-70HKM
5962-9061705MTA	3/	MT4C4256CZ-70883C
5962-9061705MNA	3/	MT4C4256F-70883C
5962-9061706MNA	0EU86	MT4C4256F-15883C
5962-9061706MYA	0EU86	MT4C4256EC-15883C
5962-9061706MRA	0EU86	MT4C4256C-15883C
5962-9061707MNA	0EU86	MT4C4256F-12883C
5962-9061707MYA	0EU86	MT4C4256EC-12883C
5962-9061707MRA	0EU86	MT4C4256C-12883C
5962-9061708MNA	0EU86	MT4C4256F-10883C
5962-9061708MYA	0EU86	MT4C4256EC-10883C
5962-9061708MRA	0EU86	MT4C4256C-10883C
5962-9061709MNA	0EU86	MT4C4256F-80883C
5962-9061709MYA	0EU86	MT4C4256EC-80883C
5962-9061709MRA	0EU86	MT4C4256C-80883C
5962-90617010MNA	0EU86	MT4C4256F-70883C
5962-90617010MYA	0EU86	MT4C4256EC-70883C
5962-90617010MRA	0EU86	MT4C4256C-70883C

See footnote at end of list.

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1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Although no longer available from an approved source, these devices have been replaced by device types 06 - 10 using a 1Meg x 4 die bonded out to produce a 256K x 4 array.

4/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448
0EU86	Austin Semiconductor Inc. 8701 Cross Park Drive Austin, TX 78754-4566

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