

Clock signal generator circuit for Desktop Video systems (SCGC)

SAA7197

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- 883 compliant burn-in
- Extended temperature range testing
- ESD protection exceeds ___V Per MIL STD 883 method 3015
- Available in low cost plastic package
- Package qualified per Philips Package Qual

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V _{DDD}	digital supply voltage (pins 8,17)	4.5	5.0	5.5	V
I _{DDA}	analog supply current	5	—	9.9	mA
I _{DDD}	digital supply current	10	—	66	mA
V _{LFCO}	LFCO input voltage (peak to peak value)	1	—	V _{DDA}	V
f _i	input frequency range	6.0	—	7.2	MHz
V _I	input voltage LOW input voltage HIGH	0 2.4	— —	0.8 V _{DDD}	V V
V _O	output voltage LOW output voltage HIGH	0 2.6	— —	0.6 V _{DDD}	V V
T _{amb}	operating ambient temperature range	−40	—	125	°C

ORDERING INFORMATION

Description	Order code
20-Pin Dual Inline Plastic Package	SAA7197/AAA

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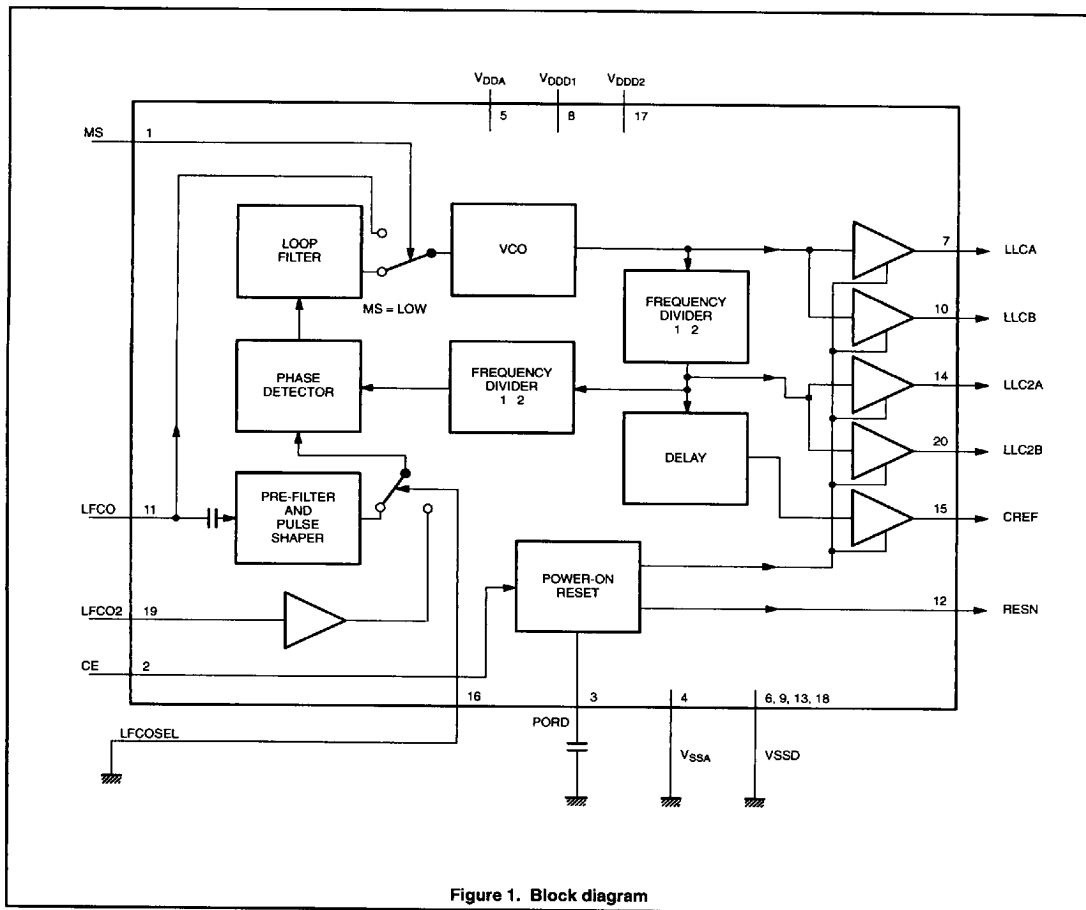


Figure 1. Block diagram

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video color space converter (DCSC) and optional extensions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input LFCO is a digital-to-analog converted signal provided by the DMSD-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = $472 \times f_H$ in 50 Hz systems
6.14 MHz = $360 \times f_H$ in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin 7), LLCB (pin 20). The rectangular output signals have 50% duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available and the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit

operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Figure 4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

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Power-on reset

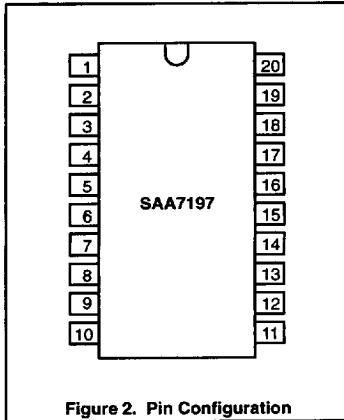
Power-on reset is activated at power-on, when the supply voltage decreases below 3.5V (Figure 4) or when chip enable is done.

The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of

this digital TV system.

The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

PIN CONFIGURATION



PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode) ¹
CE	2	chip enable/reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V _{SSA}	4	analog ground (0V)
V _{DDA}	5	analog supply voltage (+5V)
V _{SSD1}	6	digital ground 1 (0V)
LLCA	7	line-locked clock output signal (4 times f _{LFCO})
V _{DDD1}	8	digital supply voltage 1 (+5V)
V _{SSD2}	9	digital ground 2 (0V)
LLCB	10	line-locked clock output signal (4 times f _{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Figure 4)
V _{SSD3}	13	digital ground 3 (0V)
LLC2A	14	line-locked clock output signal 2A (2 times f _{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f _{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected) ¹
V _{DDD2}	17	digital supply voltage 2 (+5V)
V _{SSD4}	18	digital ground 4 (0V)
LFCO2	19	line-locked frequency control input signal 2 ¹
LLC2B	20	line-locked clock output signal 2B (2 times f _{LFCO})

NOTE:

1. MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins are connected together

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DDA}	analog supply voltage (pin 5)	-0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	-0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	± 100	mV
V_O	output voltage ($I_{OM} = 20\text{ mA}$)	-0.5	V_{DDD}	V
P_{TOT}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	-65	150	°C
T_{amb}	operating ambient temperature range	-40	125	°C
V_{ESD}	electrostatic handling for all pins ¹	-	tbf	V

NOTE:

- Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices".

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CHARACTERISTICS
 $V_{DDA} = 4.5$ to 5.5 V; $V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 5.5$ to 8.0 MHz and $T_{amb} = -40$ to 125 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		5	–	9.9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	Note 1	10	–	66	mA
V_{reset}	power-on reset threshold voltage	Figure 4	–	3.5	–	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	–	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	–	V_{DDA}	V
f_{LFCO}	input frequency range		5.5	–	8.0	MHz
C_{11}	input capacitance		–	–	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19)						
V_{iL}	input voltage LOW		0	–	0.8	V
V_{iH}	input voltage HIGH		2.0	–	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2	Note 3	5.5	–	8.0	MHz
I_{Li}	input leakage current		–	–	10	µA
C_i	input capacitance		–	–	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW		0	–	0.4	V
V_{OH}	output voltage HIGH		2.4	–	V_{DDD}	V
t_d	RESN delay time	$C_g = 0.1$ µF; Figure 4	20	–	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW		0	–	0.6	V
V_{OH}	output voltage HIGH		2.4	–	V_{DDD}	V
f_{CREF}	output frequency CREF	Figure 3	–	$2 f_{LFCO(2)}$	–	Mhz
C_L	output load capacitance		15	–	40	pF
t_{SU}	set-up time	Figure 3; Note 1	12	–	–	ns
t_{HD}	hold time	Figure 3; Note 1	4	–	–	ns
Output signals LLCA, LLCB, LLC2A and LLC2B (pins 7, 10, 14 and 20); note 3						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	–	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA CE = HIGH (pin 2)	2.6 2.6	– –	V_{DDD} V_{DDD}	V V
t_{comp}	composite rise time	Figure 3; Notes 1 and 2	–	–	8	ns
f_{LL}	output frequency LLCA	Figure 3	–	$4 f_{LFCO(2)}$	–	Mhz
	output frequency LLCB		–	$4 f_{LFCO(2)}$	–	Mhz
	output frequency LLC2A		–	$2 f_{LFCO(2)}$	–	Mhz
	output frequency LLC2B		–	$2 f_{LFCO(2)}$	–	Mhz
t_r, t_f	rise and fall times	Figure 3	–	–	5	ns
t_{LL}	duty factor LLCA, LLCB, LLC2A and LLC2B (mean values)	Note 1; Figure 3 at 1.5V level	40	50	60	ns

NOTES:

- $f_{LFCO} = 7.0$ MHz and output load 40 pF (Figure 3).
- t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Figure 3) including rise time, skew and jitter components. Measurements taken between 0.6V and 2.6V. Skew between two LLx clocks will not deviate more than ± 2 ns if output loads are matched within 20%.
- LFCO2 functions not tested.

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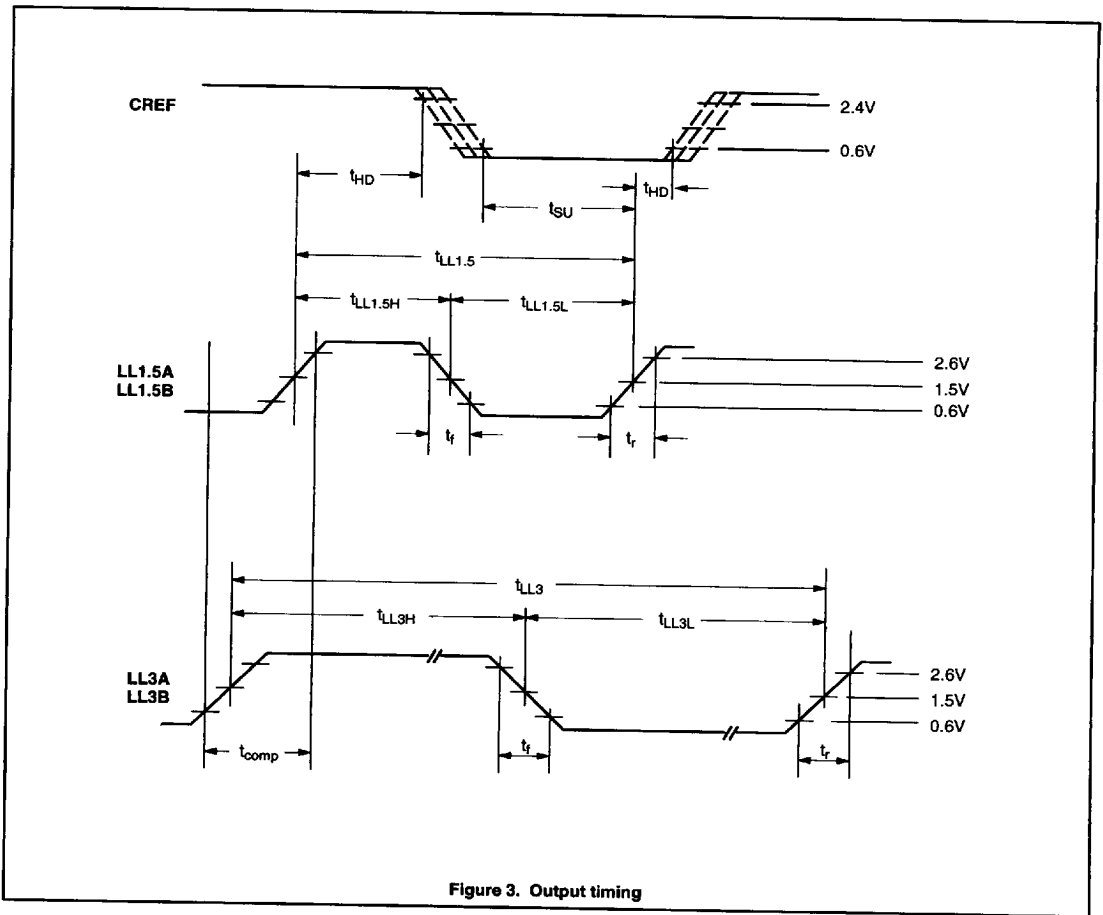


Figure 3. Output timing

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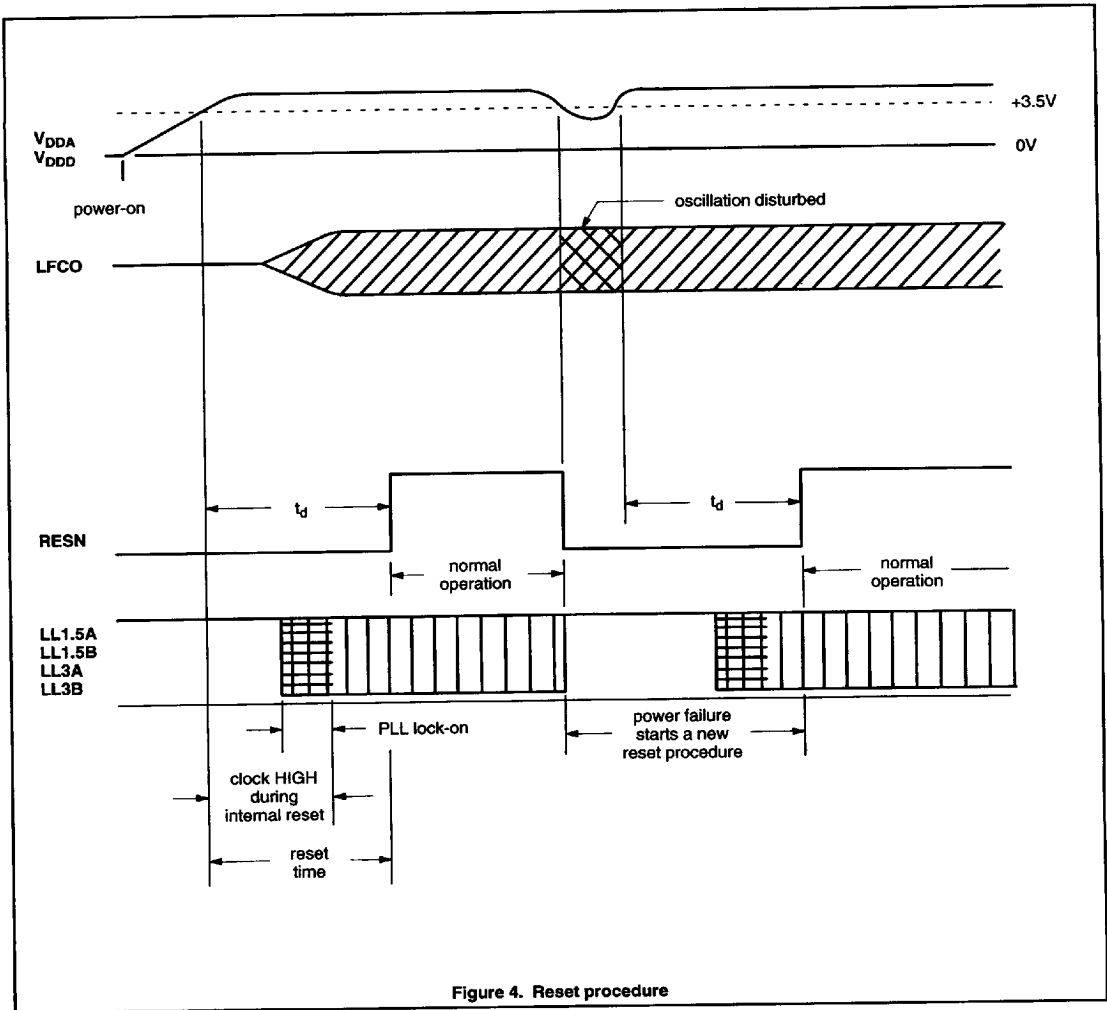


Figure 4. Reset procedure