HA17080PS, HA17082PS, HA17083P, HA17084P, HA17080GS, HA17082GS, HA17083G

AUTOMOTIVE VERSION

J-FET Input Operational Amplifiers

J-FET Input Operational Amp. provides excellent characteristics including high input impedance and low input bias current, since its input differential amp. is constructed by J-FET Pair Transistor. Accordingly it finds wide application of general controlling instrument, medical instrument. Especially it is optimum in signal precessing from sensor of high impedance. Hitachi prepares J-FET Input Operational Amp. series of one monolithic bipolar chip, HA17080, HA17082, HA17083, HA17084.

■PRODUCT OUTLINE

J-FET Input Operational Amp. series provides single, dual, quad, and they are all internal phase compensated type excepting HA17080, and include condenser for phase compensation use. And HA17080 and HA17083 are capable of offset adjustment. Package provides two types of plastic sealing and glass sealing, and "A" grade with rigid electrical characteristic specification.

Item	HA17080	HA17082	HA17083	HA17084
The number of Operational Amplifier (the number of channel)	Single	Dual		Quad.
Offset Adjusting Terminal	Exist	Not exist	Exist	Not exist
Phase Compensating Method	External	Internal		

■FEATURES

- Wide operating supply voltage range ±5 to ±18V
- Low input bias current 30pA
- Low input offset current 5pA
- High input impedance $10^{12}\Omega$
- High slew rate 13V/µs
- Wide common mode input voltage range
- Operation to input near supply voltage (Vcc) is possible.
- High voltage gain 106dB
- HA17080, HA17083 are capable of offset adjustment.
- Pin for pin compatible with Texas TL080 series

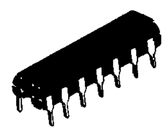
■NOTE

Since this IC is high input impedance operational amp, handling by hand may cause the input bias current and input offset current to be rise due dirt. Care shealed be taken for handling.

HA17080PS, HA17082PS

(DP-8)

HA17083P, HA17084P

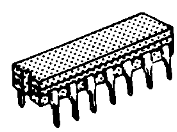


(DP-14)

HA17080GS, HA17082GS

(DG-8)

HA17083G

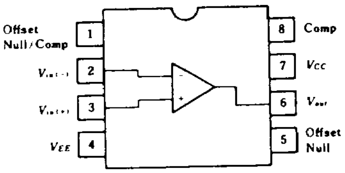


(DG-14)

Data Sheets contain information for automotive operation only. Refer to **Reference Guide** (Section 9) for a listing of supplementary publications which provide complete specifications.

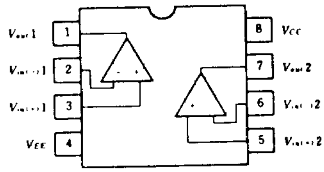
■PIN ARRANGEMENT

●HA17080



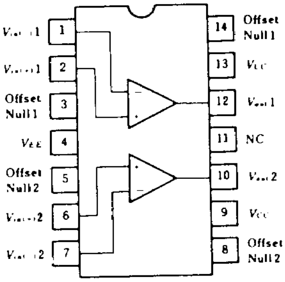
Top View

●HA17082



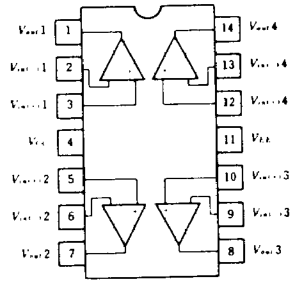
Top View

●HA17083



Top View

●HA17084



Top View

■ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Item	Symbol	P, PS series	G, GS series	Unit	Note
Supply Voltage	V_{CC}	+18	+18	V	
Supply Voltage	V_{EE}	−18	−18	V	
Differential Input Voltage	$V_{IN(diff)}$	±30	±30	V	
Input Voltage	V_{IN}	±15	±15	V	1
Power Dissipation	P_T	625	625	mW	2
Operating Temperature	T_{opr}	−40 to +85	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	−65 to +150	°C	

Notes 1. If supply voltage is less than ±15V, input voltage is to supply voltage.
2. P and PS are permissible values to $Ta = 50°C$, and beyond that, derate with 8.3mW/°C. G and GS are permissible values to $Ta = 70°C$, and beyond that, derate with 7.8mW/°C.

■ELECTRICAL CHARACTERISTICS ($V_{CC} = -V_{EE} = 15V$, $Ta = -40$ to $+85°C$)

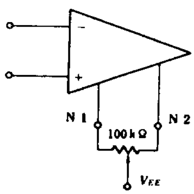
Item	Symbol	Test Condition		min	typ	max	Unit	Note
Input Offset Voltage	V_{IO}	$R_S = 50\Omega$	Non A	—	5	15	mV	1
			A version	—	3	6		
Input Offset Current	I_{IO}	$I_{IO} = \| I_I(+) - I_I(-) \|$	Non A	—	5	200	pA	1
			A version	—	5	100		
Input Bias Current	I_I		Non A	—	30	400	pA	1, 2
			A version	—	30	200		
Common Mode Input Voltage Range	V_{CM}		Non A	±10	—	—	V	1
			A version	±11	—	—		
Peak To Peak Output Voltage	V_{OP-P}	$R_L \geqq 10k\Omega$		24	27	—	V	
		$R_L \geqq 2k\Omega$		20	24	—		
Voltage Gain	A_{VD}	$R_L \geqq 2k\Omega$	Non A	88	106	—	dB	1
		$V_O = \pm 10V$	A version	94	106	—		
Common Mode Rejection Ratio	CMR	$R_S \leqq 10k\Omega$	Non A	70	86	—	dB	1
			A version	80	86	—		

■ELECTRICAL CHARACTERISTICS (Continued)

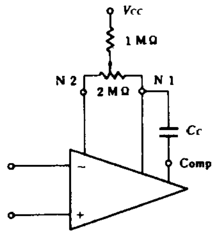
Item	Symbol	Test Condition		min	typ	max	Unit	Note
Line Regulation	$PSRR$	$R_S \leq 10k\Omega$	Non A	70	86	—	dB	1
			A version	80	86	—		
Supply Current	I_{CC}			—	1.4	2.8	mA	3
Band Width	BW	$A_{VD}=1$		—	3	—	MHz	
Slew Rate	SR	$V_{in}=10V$, $R_L=2k\Omega$, $C_L=100pF$, $A_{VD}=1$		—	13	—	V/μs	
Channel Separation	V_{o1}/V_{o2}	$A_{VD}=100$		—	120	—	dB	
Rise Time	t_r	$V_{in}=20mV$, $R_L=2k\Omega$, $C_L=100pF$, $A_{VD}=1$		—	0.1	—	μs	
Overshoot	V_{over}			—	10	—	%	
Input Resistance	R_{in}			—	10^{12}	—	Ω	
Input Noise Voltage	V_n	$R_S=100\Omega$, $f=1kHz$		—	35		nV/$\sqrt{Hz}$	

Notes: 1. Non A is the standard to HA17080, HA17082, HA17083, HA17084.
A version is the standard to HA17080A, HA17082A, HA17083A, HA17084A.
2. It's Gate Leak Current of J-FET, and depends on temperature.
At the time of measurement, it is necessary to keep junction temperature.
3. It's the value per 1 channel.

■VOLTAGE OFFSET ADJUSTING CIRCUIT

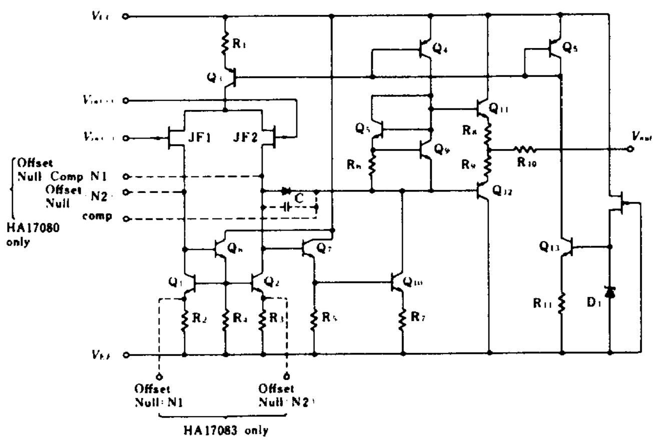


HA17083

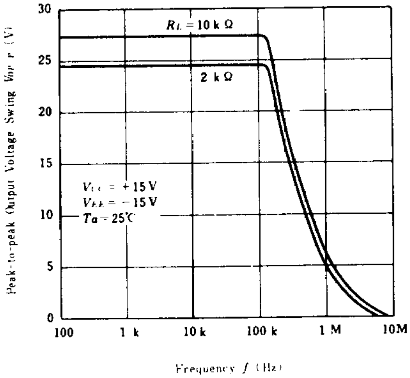


HA17080

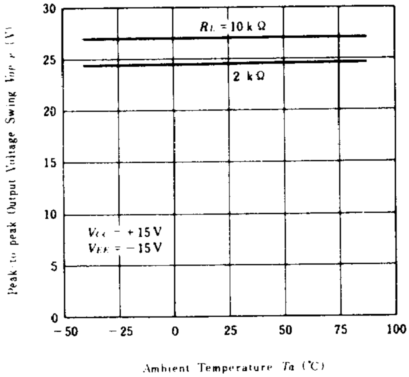
■CIRCUIT SCHEMATIC



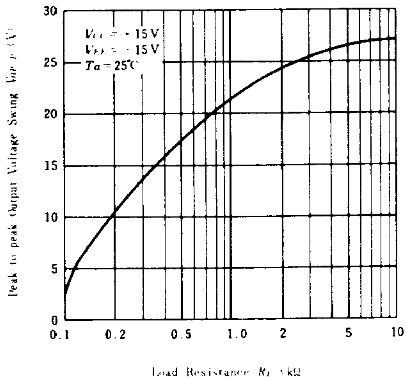
PEAK TO PEAK OUTPUT VOLTAGE SWING VS FREQUENCY



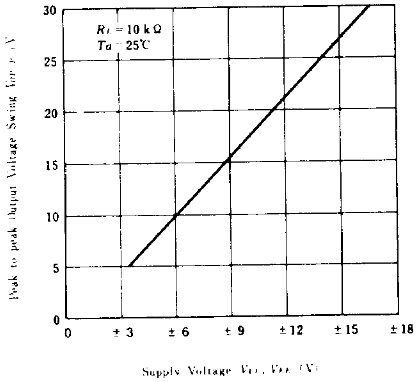
PEAK TO PEAK OUTPUT VOLTAGE SWING VS AMBIENT TEMPERATURE



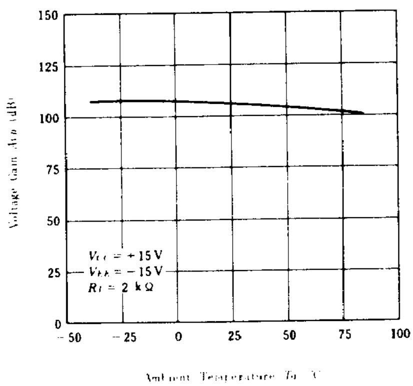
PEAK TO PEAK OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



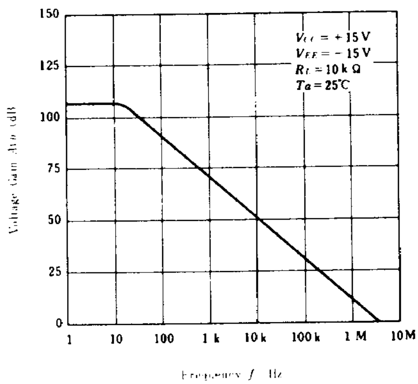
PEAK TO PEAK OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE



VOLTAGE GAIN VS AMBIENT TEMPERATURE



VOLTAGE GAIN VS FREQUENCY



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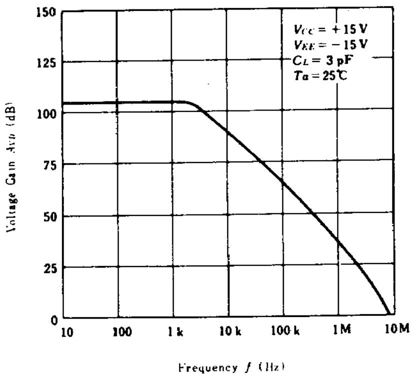
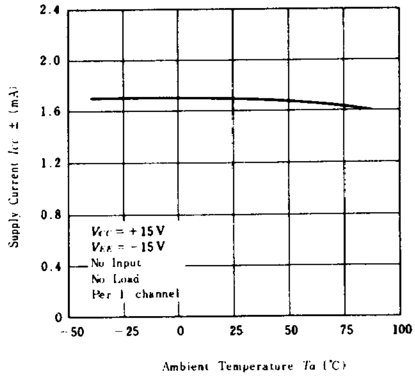
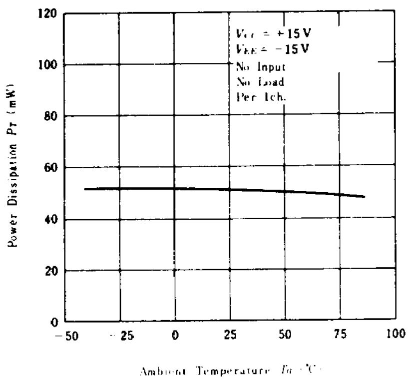
HA17080 VOLTAGE GAIN VS FREQUENCY



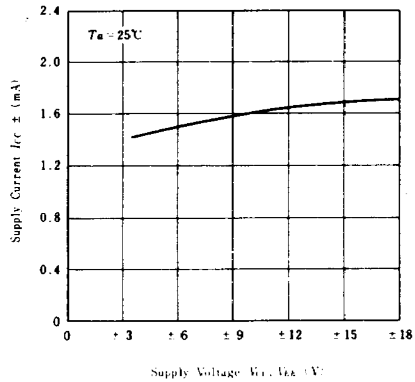
SUPPLY CURRENT VS AMBIENT TEMPERATURE



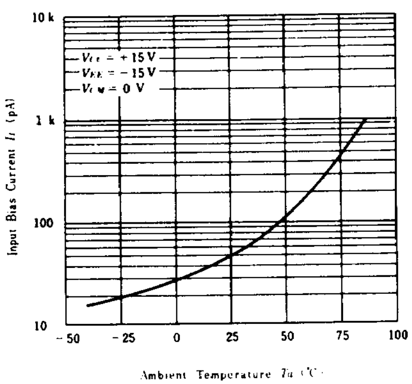
POWER DISSIPATION VS AMBIENT TEMPERATURE



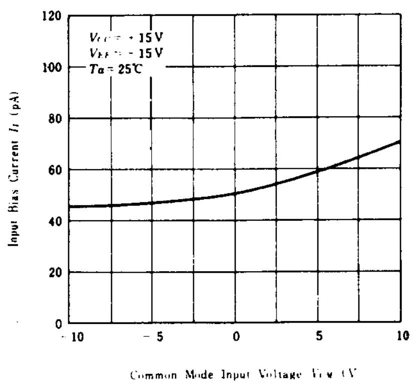
SUPPLY CURRENT VS SUPPLY VOLTAGE



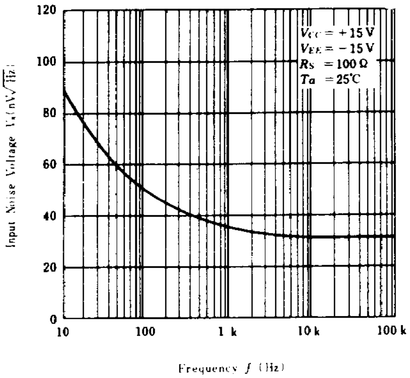
INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



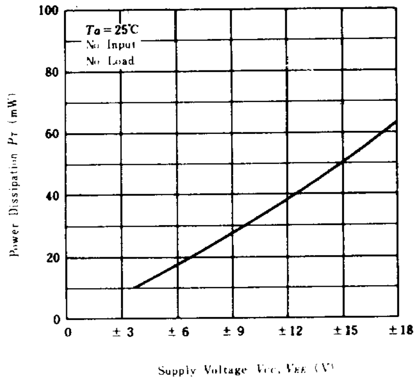
INPUT BIAS CURRENT VS COMMON MODE INPUT VOLTAGE



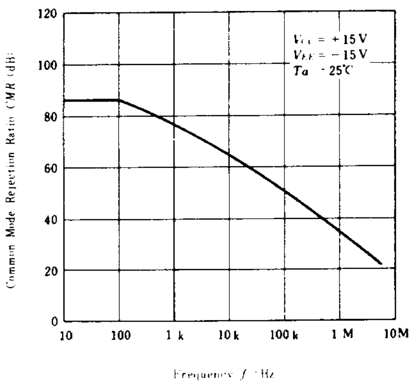
INPUT NOISE VOLTAGE VS FREQUENCY



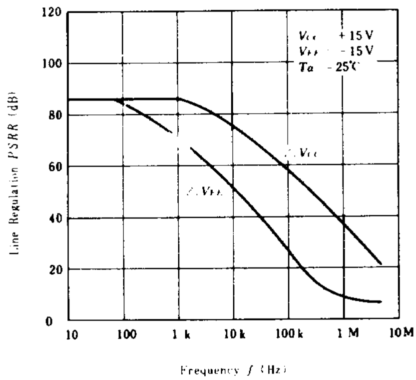
POWER DISSIPATION VS SUPPLY VOLTAGE



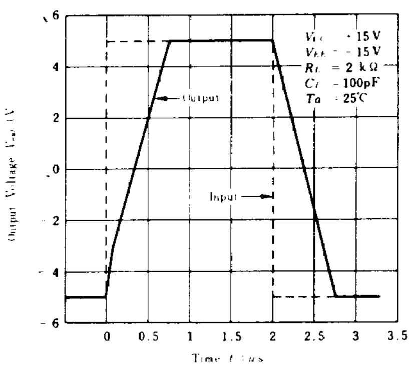
COMMON MODE REJECTION RATIO VS FREQUENCY



LINE REGULATION VS FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



HA17083 OFFSET ADJUSTING