Am90CL256

Low-Power 256K x 1 CMOS Enhanced Page Mode DRAM

OVERVIEW

The 256K x 1 CMOS Low-Power ('L') DRAM versions share common functional descriptions, DC and AC characteristics with the corresponding standard CMOS (non-'L') versions. The only additions to these sections are:

DISTINCTIVE CHARACTERISTICS

- Extended refresh period
  — 32 ms (Max.) during standby
- Low data retention current
  — 230 μA (Max.)
- Low-power dissipation
  — 0.55 mW (Max.)

ORDERING INFORMATION

The Ordering Information for the Low-Power DRAM versions are the same as for the Standard CMOS DRAMs, with the exception of an 'L' inserted within the device number to denote 'Low-Power.' For example, the Am90CL255 is = a 256K x 1 CMOS "Low-Power" Nibble Mode DRAM. All temperature ranges, speed and package options remain the same as those listed in Ordering Information sections for the respective Standard CMOS DRAMs.

DC CHARACTERISTICS

The low-power version DRAMs are screened for one additional parameter, viz, CMOS standby current. All other DC characteristics remain the same for both families.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{CC6}	V_{CC} Supply Current CMOS Standby	$\overline{RAS} \geq V_{CC} - 0.5$ V and $\overline{CAS}$ at V_{IH}, all other inputs and outputs $\geq V_{SS}$	Am90CL256		0.1	mA

The Am90CL256-15 is screened for I_{CC1} = 60 mA, I_{CC3} = 60 mA, and I_{CC4} = 60 mA

AC CHARACTERISTICS

AC Characteristics remain unchanged on the low-power 100 ns and 120 ns versions. The AC characteristics corresponding to the 150 ns speed are on the following page.

FUNCTIONAL DESCRIPTION

The Functional Descriptions for low-power versions are the same as the corresponding standard versions. The low-power devices, however, support Extended Refresh cycles described below:

Extended Refresh Cycle

All low-power versions extend the Refresh Cycle period to 32 ms for $\overline{RAS}$-Only Refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA for data retention. The low-standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC})\ (I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{T_{RI}}$$

where t_{RC} = Refresh Cycle Time

and t_{RI} = Refresh Interval Time or $t_{REF}/256$

Before entering or leaving an Extended Refresh period, the entire array must be refreshed at the normal interval of 4 ms. This can be accomplished by either a burst or distributed refresh.

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SWITCHING CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL256-15 Min.	Am90CL256-15 Max.	Units
READ/WRITE/READ-MODIFY-WRITE AND REFRESH CYCLES					
1	t_{RAS}	$\overline{RAS}$ Pulse Width	150	75,000	ns
2	t_{RC}	Random R/W Cycle Time	245		ns
3	t_{RP}	$\overline{RAS}$ Precharge Time	85		ns
4	t_{CSH}	$\overline{CAS}$ Hold Time	150		ns
5	t_{CAS}	$\overline{CAS}$ Pulse Width	35	75,000	ns
6	t_{WRP}	Write-to-$\overline{RAS}$ Precharge Time (Note 10)	–		ns
7	t_{RWH}	$\overline{RAS}$-to-Write Hold Time (Note 10)	–		ns
8	t_{ASR}	Row Address Setup Time	0		ns
9	t_{RAH}	Row Address Hold Time	20		ns
10	t_{CP}	$\overline{CAS}$ Precharge Time	10		ns
11	t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	10		ns
12	t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time (Note 1)	30	120	ns
13	t_{ASC}	Column Address Setup Time	0		ns
14	t_{CAH}	Column Address Hold Time	20		ns
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	65		ns
16	t_{REF}	Time Between Refresh		4	ms
17	t_T	Transition Time (Rise and Fall) (Note 2)	1	25	ns
18	t_{ON}	Output Buffer Turn-On Delay	0		ns
19	t_{OFF}	Output Buffer Turn-Off Delay		25	ns
READ CYCLE					
20	t_{RAC}	Access Time From $\overline{RAS}$ (Notes 3 & 5)		150	ns
21	t_{CAC}	Access Time From $\overline{CAS}$ (Notes 4 & 5)		30	ns
22	t_{CAA}	Access Time from Column Address (Note 5)		70	ns
23	t_{RSH} (R)	$\overline{RAS}$ Hold Time (Read Cycle)	30		ns
24	t_{RCS}	Read Command Setup Time	0		ns
25	t_{CAR}	Column Address-to-$\overline{RAS}$ Setup Time	70		ns
26	t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$ (Note 6)	5		ns
27	t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$ (Note 6)	10		ns
WRITE CYCLE					
28	t_{RSH} (W)	$\overline{RAS}$ Hold Time (Write Cycle)	30		ns
29	t_{RWL}	Write Command to $\overline{RAS}$ Setup Time	30		ns
30	t_{CWL}	Write Command to $\overline{CAS}$ Setup Time	30		ns
31	t_{WP}	Write Command Pulse Width	25		ns
32	t_{WCS}	Write Command Setup Time (Note 7)	0		ns
33	t_{WCH}	Write Command Hold Time	30		ns
34	t_{DS}	Data-In Setup Time	0		ns
35	t_{DH}	Data-In Hold Time	25		ns
READ-MODIFY-WRITE (RMW) CYCLE					
36	t_{RWC}	RMW Cycle Time	280		ns
37	t_{RRW}	RMW $\overline{RAS}$ Pulse Width	185	75,000	ns
38	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	65	75,000	ns
39	t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time (Note 7)	150		ns
40	t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time (Note 7)	30		ns
41	t_{AWD}	Column Address-to-$\overline{WE}$ Delay Time (Note 7)	65		ns

Notes: See next page for notes.

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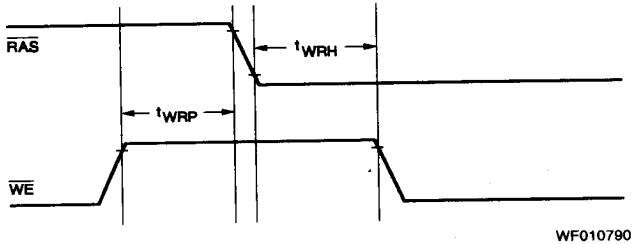
SWITCHING CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Am90CL256-15 Min.	Am90CL256-15 Max.	Units
ENHANCED PAGE MODE CYCLE					
42	t_{CAP}	Access Time from Column Precharge Time (Note 8)		70	ns
43	t_{PC}	Enhanced Page Mode Read/Write Cycle Time (Note 8)	75		ns
44	t_{PCM}	Enhanced Page Mode RMW Cycle Time	110		ns

Notes:
1. t_{RCD} (Max.) is specified for reference only.
2. t_T is measured between V_{IH} (Min.) and V_{IL} (Max.).
3. Assumes that $t_{RCD} \leq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), then t_{RAC} will increase by an amount that t_{RCD} exceeds t_{RCD} (Max.).
4. Assumes $t_{RCD} \geq t_{RCD}$ (Max.).
5. If $t_{ASC} < (t_{CAA}$ (Max.) $- t_{CAC}$ (Max.) $- t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
6. Either t_{RCH} or t_{RRH} must be satisfied.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is a $\overline{CAS}$-controlled write cycle (early write cycle) and D_{OUT} pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{RWD} \geq t_{RWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), then the cycle is a RMW cycle and the data-out will contain the data read from the selected address. If any of these conditions are not satisfied, the condition of data-out is indeterminate.
8. Access time and cycle time are determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.
9. All AC parameters are measured with a load equivalent to two TTL loads and 100-pF capacitive load.
10. Timing parameters t_{WRP} and t_{RWH} (see below), referenced to $\overline{RAS}$, are redundant on the Am90CL256, and hence, not specified in the data sheet.



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