



Quad 2-Input NOR Gate with Strobe

ELECTRICALLY TESTED PER: MPG 10500

The 10500 is a quad 2 input **NOR** gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

- 40 mW Max/Gate (No Load)
- $t_{pd} = 2.0$ ns typ
- $t_r, t_f = 2.0$ ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
AOUT	2	6	3	51 Ω to V_{TT}
BOUT	3	7	4	51 Ω to V_{TT}
A _{IN}	4	8	5	OPEN
A _{IN}	5	9	7	OPEN
B _{IN}	6	10	8	OPEN
B _{IN}	7	11	9	OPEN
VEE	8	12	10	VEE
Common Input	9	13	12	OPEN
C _{IN}	10	14	13	OPEN
C _{IN}	11	15	14	OPEN
D _{IN}	12	16	15	OPEN
D _{IN}	13	1	17	OPEN
COUT	14	2	18	51 Ω to V_{TT}
DOUT	15	3	19	51 Ω to V_{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

$V_{TT} = -2.0$ V MAX/ -2.2 V MIN

$V_{EE} = -5.7$ V MAX/ -5.2 V MIN

Military 10500

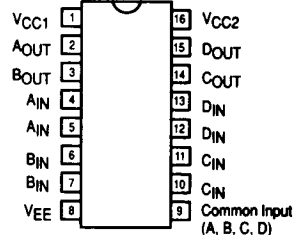


AVAILABLE AS

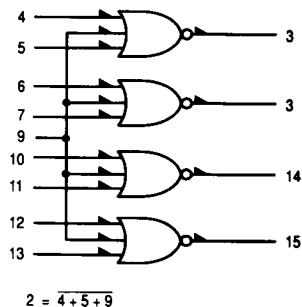
- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10500/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

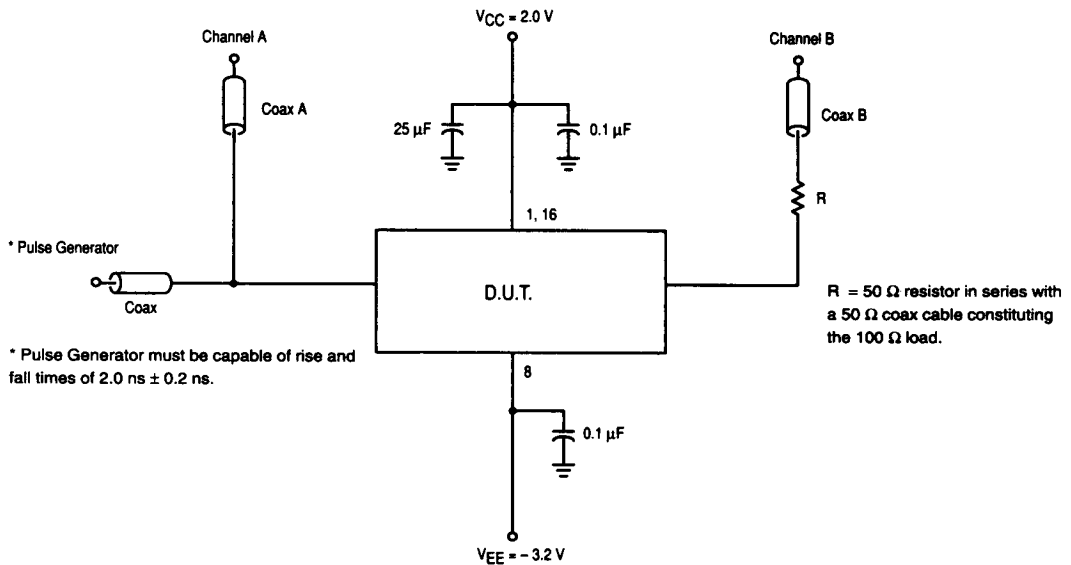
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



**NOTES**

1. Length of Coax_A and Coax_B should be of equal length for equal time delay.
2. Unused outputs should be loaded $100\text{ }\Omega$ to ground.
3. 2:1 divider may be used.

NOTES

1. V_{IN} waveform has the following characteristics:

- a) Pulse width $\geq 20\text{ ns}$.
- b) frequency = 1.0 MHz .
- c) t_r and $t_f = 2.0\text{ ns} \pm 0.2\text{ ns}$.

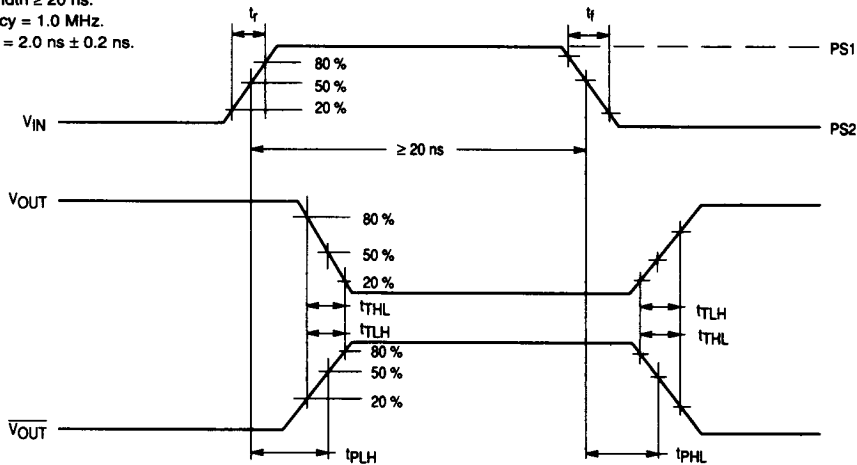


Figure 1. Switching Test Circuit and Waveforms

10500 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	V _{CC}	VEEL	VEE	VEE
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-2.94	-5.2	-5.2
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.345	+2.0	-2.94	-5.2	-5.2
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.03	+0.285	+2.0	-2.94	-5.2	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:										
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V										
		Subgroup 1		Subgroup 2		Subgroup 3													
		Min	Max	Min	Max	Min	Max												
VOH	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V											
VOL	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.565	- 1.92	- 1.655	V	4 - 7, 9 - 13										
VOHA	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V				4 - 7, 9 - 13							
VOLA	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.565	- 1.92	- 1.635	V				4 - 7, 9 - 13							
IEE	Power Supply Drain Current	- 26	- 3.0	- 29	- 3.0	- 29	- 3.0	mA											
IIH	Input Current High		245		415		415	μA	4 - 7, 9 - 13										
IIH1	Input Current High		470		800		800	μA	9										
II_L	Input Current Low	0.5		0.3		0.5		μA		4 - 7, 9 - 13									

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	Functional Parameters:	+ 25 °C		+ 125 °C				- 55 °C		Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11											
		Min	Max	Min	Max	Min	Max										
t _{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	V _{IN}	V _{OUT}	V _{CC}	V _{EEL}	P. U. T.				
t _{TLH}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15				
t _{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14				
t _{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14				