240 Channel Common Driver for Dot matrix STN Liquid Crystal Display with High Voltage Drive

EM65H137

Contents

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General description

The EM65H137 is a 240-channel common driver which drives a dot matrix STN liquid crystal panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43V high-voltage CMOS process technology, a high-voltage drive of +21.5 V and -21.5 V, centering on VM is possible. -21.5V is generated from max +21.5V with built-in switching circuit and external capacity. 3 V is used for logic drive. This device is used together with the segment driver EM65H130 or EM65H134.

Feature

- Display duty: Up to 1 / 240
- LCD drive voltage: 43 V max
- Built-in 240 bits bi-directional shift register
- Built-in switching circuit (to generate -21.5V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit
- Pin programmable, Output mode change: 240-output mode 200-output mode 160-output mode
- Built-in display-off function: when /DSPOF is “L”, all LCD drive output remain at the VM level.
- Flex TCP

Applications

- PDA
- Dictionary
- Message display product

Pin configurations (package)

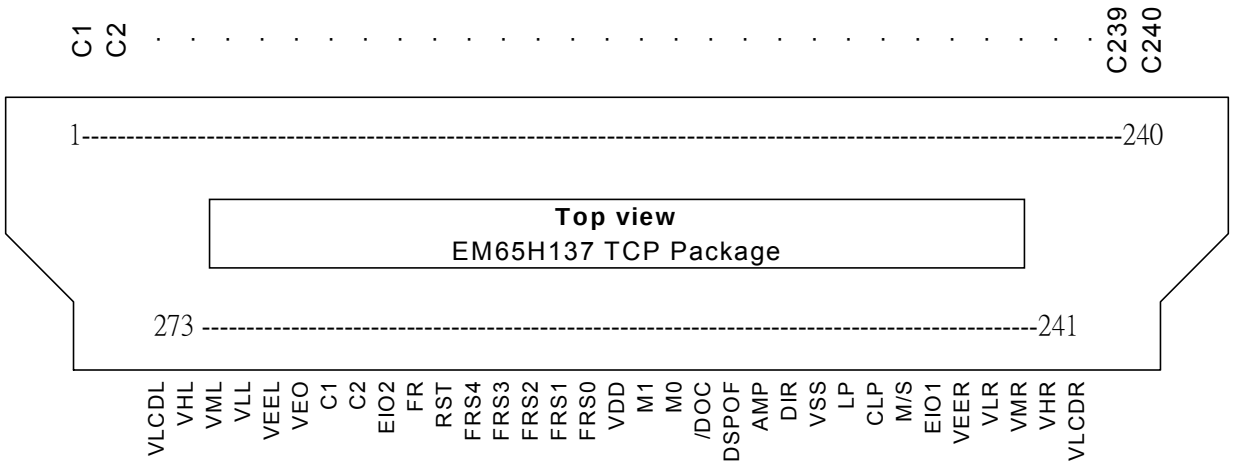


Figure1. TCP package pin arrangement

Functional block diagram

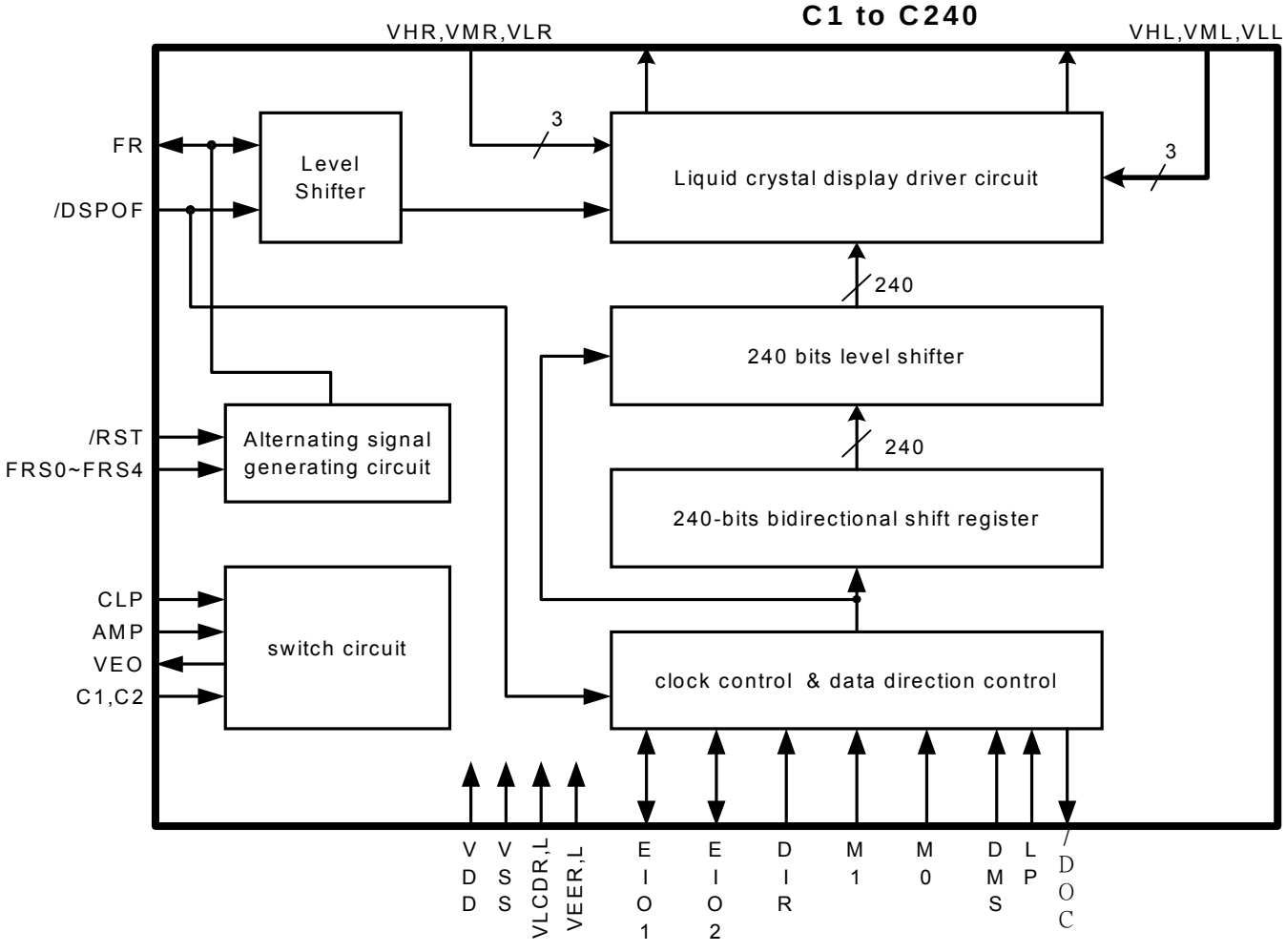


Figure 2. System block diagram

Pin descriptions

Table 1. Pin arrangement

Pin NO.	Symbol	I/O	Description
1 to 240	C1–C240	O	LCD driver output
241,273	VLCDR, VLCDL	-	Power supply for LCD driver
242,272	VHR, VHL	-	
243,271	VMR, VML	-	
244,270	VLR, VLL	-	
245,269	VEER, VEEL	-	
246 265	EIO1 EIO2	I/O	Serial data input / output pin
247	DMS	I	Controls the display-off function and display-off signal output from /DOC pin.
248	CLP	I	Built-in switching circuit clock input.
249	LP	I	Shift clock input for segment mode
250	VSS	I	Ground (0V)
251	DIR	I	Display data shift direction selection
252	SWC	I	Built-in switching circuit on-off control.
253	/DSPOF	I	Control input for deselect output level
254	/DOC	O	Display off control pin for segment driver.
256 255	M1 M0	I	Mode select for the number of LCD drive output pins.
257	VDD	I	Power supply for logic system
258~262	FRS0~FRS4	I	This pin specifies the cycle of the alternating signal, FR signal in the unit of the number of lines(LP signal)
263	RST	I	Setting this pin to initializes the FR signal circuit
264	FR	I/O	AC-converting signal input for LCD driver waveform
265	C2	-	Capacitance
266	C1	-	Capacitance
267	VEO	O	Voltage output of built-in switching circuit

Table 2. Pin descriptions

<table>
<tr><th>Symbol</th><th>I/O</th><th>Connect To</th><th>Description</th></tr>
<tr><td>VLCDL, R
VEEL, R</td><td>I</td><td>Power supply</td><td>LCD driver output</td></tr>
<tr><td>VHL,R
VML,R
VLL,R</td><td>I</td><td>Power supply</td><td>Power supply for LCD driver level
Select level : VH,VL
Non-select level : VM</td></tr>
<tr><td>VDD
VSS</td><td>I</td><td>Power supply</td><td>Power supply for internal logic system</td></tr>
<tr><td>VEO</td><td>O</td><td>VEE</td><td>When using built-in switching circuit to generate VEE, VM voltage is point of reference. VLCD - VM voltage is reversed and output as VEE. If switching circuit not used, set this pin to open, don’t connect to any pin</td></tr>
<tr><td>C1
C2</td><td>-</td><td>-</td><td>When using built-in switching circuit to generate VEE, should be connected, or it don’t connect.</td></tr>
<tr><td>LP</td><td>I</td><td>Controller</td><td>Shift clock for bi-directional shift register, data is shifted on the falling edge of the clock</td></tr>
<tr><td>FR</td><td>I/O</td><td>Controller
or
Open</td><td>AC signal for LCD drive
The LCD driver output voltage level can be set by line latch output signal and FR signal
It can be produced by internal function of FRS0~FRS4</td></tr>
<tr><td>FR S0
FR S1
FR S2
FR S3
FR S4</td><td>I</td><td>VDD/VSS</td><td>This pin specifies the cycle of the alternating signal, FR signal in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the EM65H137 is driven by an external alternating signal, specify the number of lines as zero.</td></tr>
<tr><td>M0
M1</td><td>I</td><td>VDD/VSS</td><td>Switch terminals for the number of LCD drive output pins.
<table>
<tr><td>M0</td><td>M1</td><td>Description(DIR=”H”)</td></tr>
<tr><td>H</td><td>H</td><td>240 output (C1-C240)</td></tr>
<tr><td>H</td><td>L</td><td>200 output (C21-C220)</td></tr>
<tr><td>L</td><td>H</td><td>160 output (C41-C200)</td></tr>
<tr><td>L</td><td>L</td><td>Prohibited</td></tr>
</table></td></tr>
<tr><td>EIO1
EIO2</td><td>I</td><td>Controller</td><td>Data input/output shift for bi-directional shift register
<table>
<tr><td>DIR</td><td>EIO1</td><td>EIO2</td></tr>
<tr><td>H</td><td>Output</td><td>Input</td></tr>
<tr><td>L</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>CLP</td><td>I</td><td>LP/VSS</td><td>When using built-in switching circuit and generating VEE, this pin connect LP pin. If built-in switching circuit is not used, CLP must be fixed to VSS.</td></tr>
<tr><td>/RST</td><td>I</td><td>Controller</td><td>
<table>
<tr><td>/RST</td><td>Description</td></tr>
<tr><td>H</td><td>Normal status</td></tr>
<tr><td>L</td><td>Initializes the FR signal circuit</td></tr>
</table></td></tr>
<tr><td>/DSPOF</td><td>I</td><td>Controller</td><td>Control signal for output deselect level
• When the signal is low，the output (C1 – C240) of LCD driver be set to level VM，the internal register is not cleared
• When the signal is high, returns to the normal status.</td></tr>
<tr><td>DMS</td><td>I</td><td>VDD/VSS</td><td>Display-off function mode selection.
<table>
<tr><td>DMS</td><td>Description</td></tr>
<tr><td>H</td><td>When /DSPOF is low level,
C1-C240 set VM level.</td></tr>
<tr><td>L</td><td>Until 16 times serial data is into EIO,
C1-C240 set VM level.</td></tr>
</table></td></tr>
</table>

Continuous Table 2

<table>
<tr><th>Symbol</th><th>I/O</th><th>Connect To</th><th>Description</th></tr>
<tr><td>/DOC</td><td>O</td><td>-</td><td>Display off control pin for segment driver., when using DMS is low level , /DOC pin should be connected to segment LSI display off control pin.
When DMS=”H” , /DSPOF=”H”, /DOC output “H” level
/DSPOF=”L” , /DOC output “L” level.
When M/S = “L”,. Until 16 times serial data is into DIO, C1-C240 set to VM level.</td></tr>
<tr><td>DIR</td><td>I</td><td>VDD/VSS</td><td>Directional selection of bi-directional shift register
<table>
<tr><th>DIR</th><th>M0</th><th>M1</th><th>Shift direction</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>C1 to C240</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>C240 to C1</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>C21 to C220</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>C220 to C21</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>C41 to C200</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>C200 to C41</td></tr>
<tr><td>X</td><td>L</td><td>L</td><td>Prohibited</td></tr>
</table>
X: don’t care</td></tr>
<tr><td>SWC</td><td>I</td><td>VDD/VSS</td><td>Built-in switch circuit control
When using built-in switching circuit, this pin must be fixed to VDD, or this pin must be fixed to VSS</td></tr>
<tr><td>C1 to C240</td><td>O</td><td>LCD Panel</td><td>LCD driver output. By a combination of the display data and the FR signal, when /DSPOF is set to VDD, either VH, VL, or VM is selected and transmitted to the output circuit.</td></tr>
</table>

Function description

. Clock control and data direction control

This circuit controlled the input/output data of bi-directional pins, direction of data shift and display off function for segment driver (/DOC signal)

. Line Shift Register

This is 240-bits shift register circuit. The shift direction is determined by DIR pin. The first data is from EIO1 and EIO2 pin, Shifts data from the data input pin on the falling edge of the LP signal.

. Level Shifter

The logic voltage signal is boost to the LCD driver voltage level, and output to the driver block.

. 3-level Driver

Drive the LCD driver output pins from the line shift register data, selecting one of 3 levels (VH, VM, VL) based on the FR and /DSPOF signals

. Alternating signal generating circuit

This circuit generate FR signal for LCD driver to suppress cross-talk. The number of lines, which is an integer from 2 to 31, is specified by FRS0~FRS5. When the EM65H137 is driven by an external alternating signal, specify the number of lines as zero.

. Switch circuit

A high voltage driver of VH and VL centering on VM, VH is generated from VH with built-in switch circuit and external capacity.

. Relation between FR, data input and Liquid crystal display driver output voltage level, Explain as following table 3:

Table 3. Liquid crystal display driver output voltage level

FR	Latch data	/DSPOF	Driver output voltage level
H	H	H	VL
H	L	H	VM
L	H	H	VH
L	L	H	VM
X	**X**	L	VM

VL<VM< VH H: VDD L: VSS X: Don't care

. Relationship between the display data and driver output pin

Table 4. . Relationship between the display data and driver output pin

DIR	M0	M1	Data transfer direction	EIO_1	EIO_2
H	H	H	C1→C240	Output	Input
	H	L	C21→C220		
	L	H	C41→C200		
L	H	H	C240→C1	Input	Output
	H	L	C220→C21		
	L	H	C200→C41		
X	L	L	Prohibited	**X**	**X**

X: don't care

. Example of power supply circuit

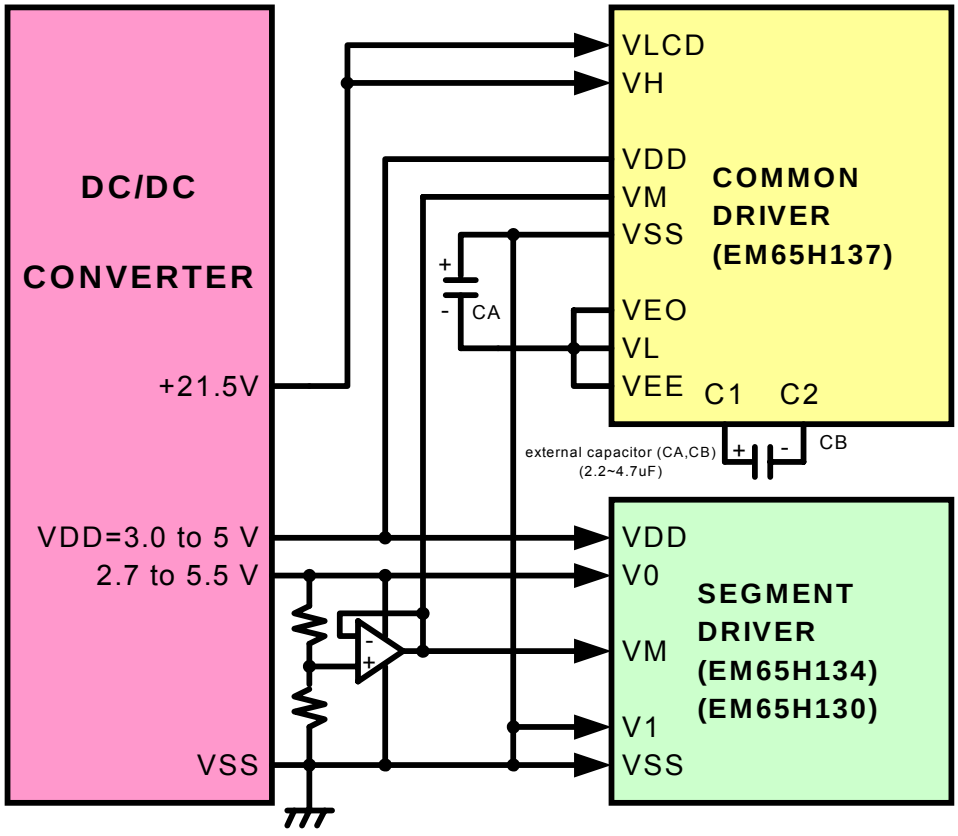


Figure 3. Power supply circuit example

. Precaution when connecting or disconnecting the power.

This LSI has a high voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating. When connecting or disconnecting the power supply, show the following recommend sequence.

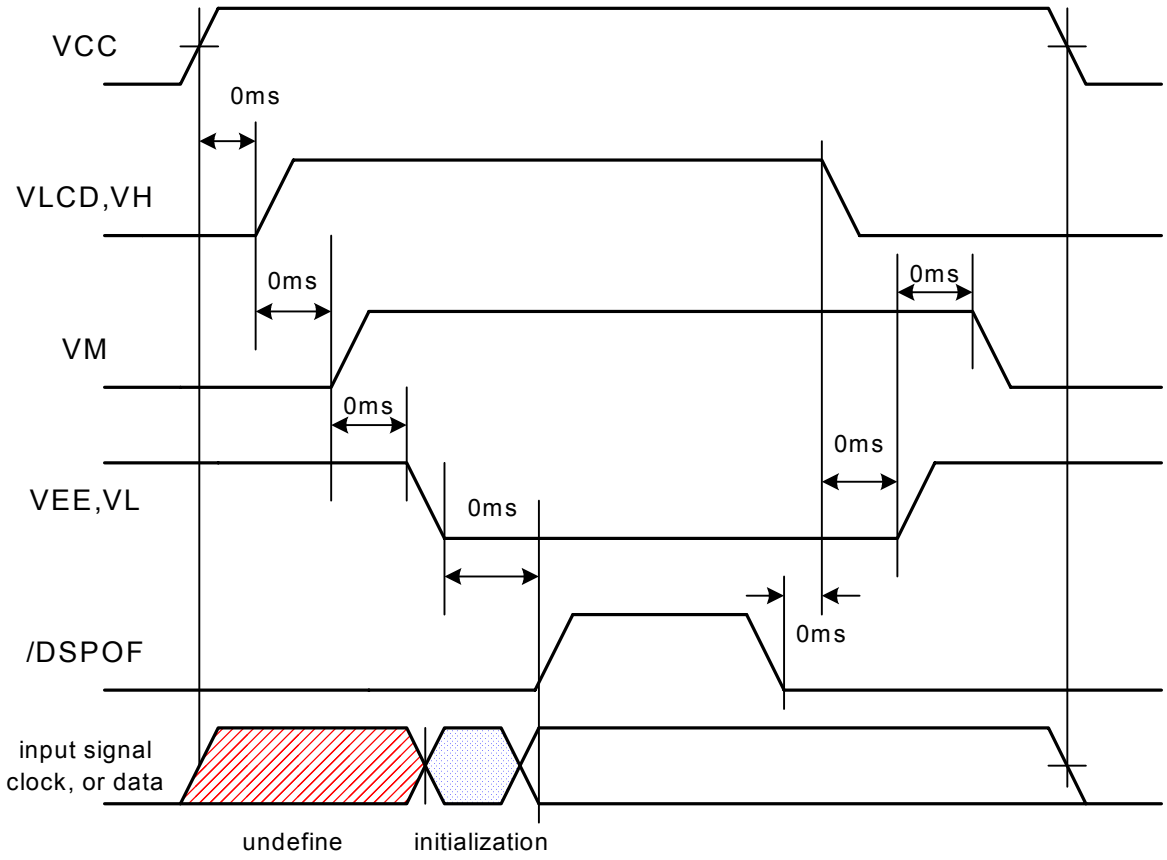


Figure 4.Sequence for connecting or disconnecting the power supply

Absolute maximum rating

Table 5 absolute maximum ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	VDD	Ta=25℃ Referenced to VSS (0V)	VDD	-0.3 to +7.0	V
Supply voltage (2)	VLCD		VLCDL, VLCDR	-0.3 to +25.0	V
	VEE		VEEL, VEER	-20.0 to +0.3	V
Input voltage (1)	V_I		Logic input pin	-0.3 to VDD+0.3	V
Input voltage (2)	VH		VHL, VHR	-0.3 to VLCD	V
Input voltage (3)	VM		VML, VMR	-0.3 to +5.0	V
Input voltage (4)	VL		VLL, VLR	+0.3 to VEE	V
Operating temperature	Topr			-30 to +75	℃
Storage temperature	Tstg			-45 to +125	℃

DC electrical characteristics

Table 6.DC characteristics of common mode (VSS=0V, VDD=+2.5 to 5.5V, Ta = -20~85°C)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		LP, DIR, FR, M1, M0, EIO1, EIO2, /DSPOF, FRS0-4, /RST, DMS , /DOC , CLP , SWC	$0.8V_{DD}$			V
	V_{IL}					$0.2V_{DD}$	V
Output voltage	V_{OH}	I_{OH}= -0.4mA	EIO_1, EIO_2 , FR , /DOC	V_{DD}-0.4			V
	V_{OL}	I_{OL}= +0.4mA				+0.4	V
Input leakage current	I_{LIH}	$V_I=V_{DD}$	LP, DIR, FR, M1, M0, EIO1, EIO2, /DSPOF, FRS0-4, /RST, DMS , /DOC , CLP , SWC			+5	μA
	I_{LIL}	$V_I=V_{SS}$				-5	μA
Output resistance	R_{ON}	I_{ON}=150uA	C1-C240		0.7	2.0	kΩ
Stand-by current	I_{STB}	*1	V_{SS}			2.0	μA
Consumed current (1)	I_{DD}	*2	V_{DD}		10	40	μA
Consumed current (2)	I_{DD}	*3	V_{DD}		20	50	μA
Consumed current(3)	I_{LCD}	*2	V_0		20	35	μA

NOTE:

1. V_{DD} = +5V, VLCD-VEE=40V, V_I = V_{SS}
2. V_{DD} = +3.3V, VLCD-VEE=40V, V_I = V_{SS}, f_{LP}=19.2kHz, f_{FR}=1.5kHz.
3. V_{DD} = +5V, VLCD-VEE=40V, V_I = V_{SS}, f_{LP}=19.2kHz, f_{FR}=1.5kHz.

AC electrical characteristics

Table 7. AC characteristics of Common driver timing 1, VCC=2.5 to 5.5V, VLCD-VEE=15 to 43V, Ta=-30~+75℃

Item	Symbol	Pin Name	Min.	Max.	Unit.	Note.
Clock cycle time	tCYC	LP	400	--	ns	
LP high-level width	tCWH	LP	25	--	ns	
LP low-level width	TCWL	LP	370	--	ns	
LP rising time	tr	LP	--	30	ns	
LP falling time	tf	LP	--	30	ns	
Data setup time	tDS	EIO1, EIO2, LP	100	--	ns	
Data hold time	tDH	EIO1, EIO2, LP	0	--	ns	
Data output delay time	tDD	EIO1, EIO2, LP	--	150	ns	*1
FR output delay time	tMD	FR, LP	--	150	ns	*1
FR setup time	tMS	FR, LP	20	--	ns	
FR hold time	tMH	FR, LP	20	--	ns	
/DOC delay time 1	tDOC1	/DSPOF, /DOC	--	300	ns	*2
/DOC delay time 2	tDOC2	EIO1, EIO2, /DOC	--	300	ns	*2

Table 8. AC characteristics of Common driver timing 2, VCC=2.5 to 5.5V, VLCD-VEE=15 to 43V, Ta=-30~+75℃

Item	Symbol	Pin Name	Min.	Max.	Unit.	Note.
Output delay time 1	tpd1	C(n), FR	--	1.2	us	*2

Table 9. AC characteristics of Common driver timing 3, VCC=2.5 to 5.5V, VLCD-VEE=15 to 43V, Ta=-30~+75℃

Item	Symbol	Pin Name	Min.	Max.	Unit.	Note.
Output delay time 2	tpd2	C(n), FR	--	1.2	us	*2

Notes: *1.Defined by connecting the load circuit shown in next figure

*2.Defined by connecting the load circuit shown in next figure

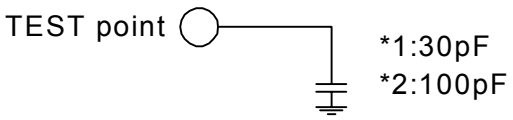
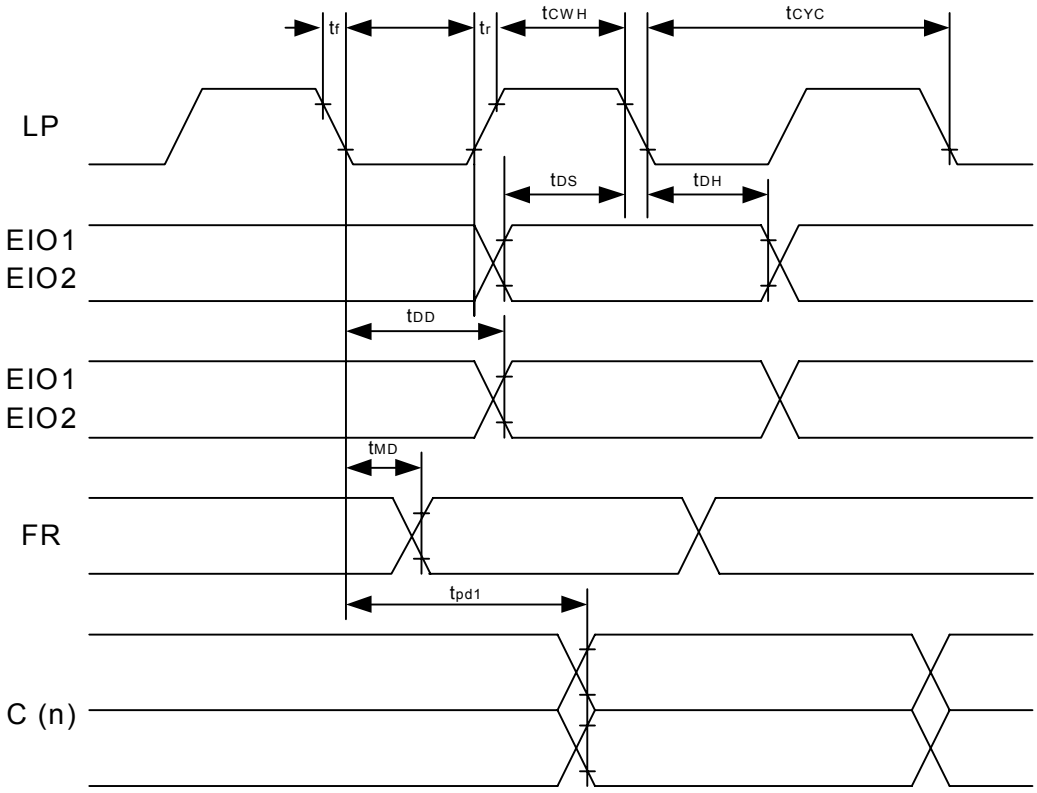
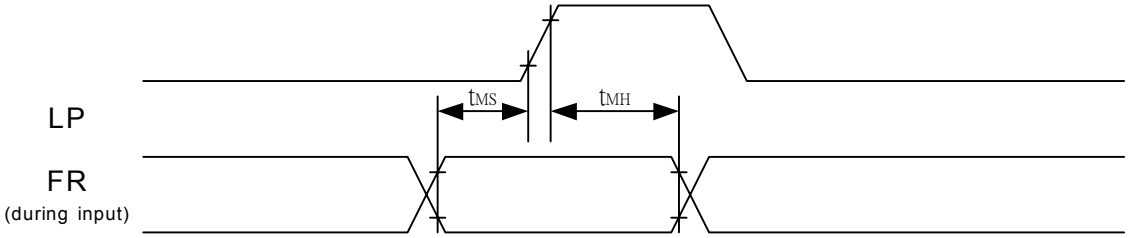


Figure 5. Load circuit

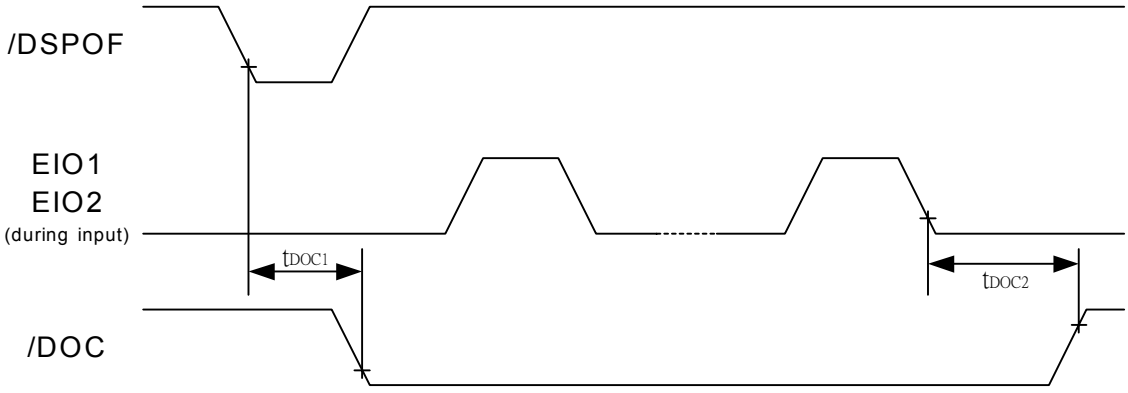
Timing diagrams



(a) AC characteristics of Common driver timing 1



(b) AC characteristics of Common driver timing 2



(c) AC characteristics of Common driver timing 3

Figure 6. AC timing

Application circuit

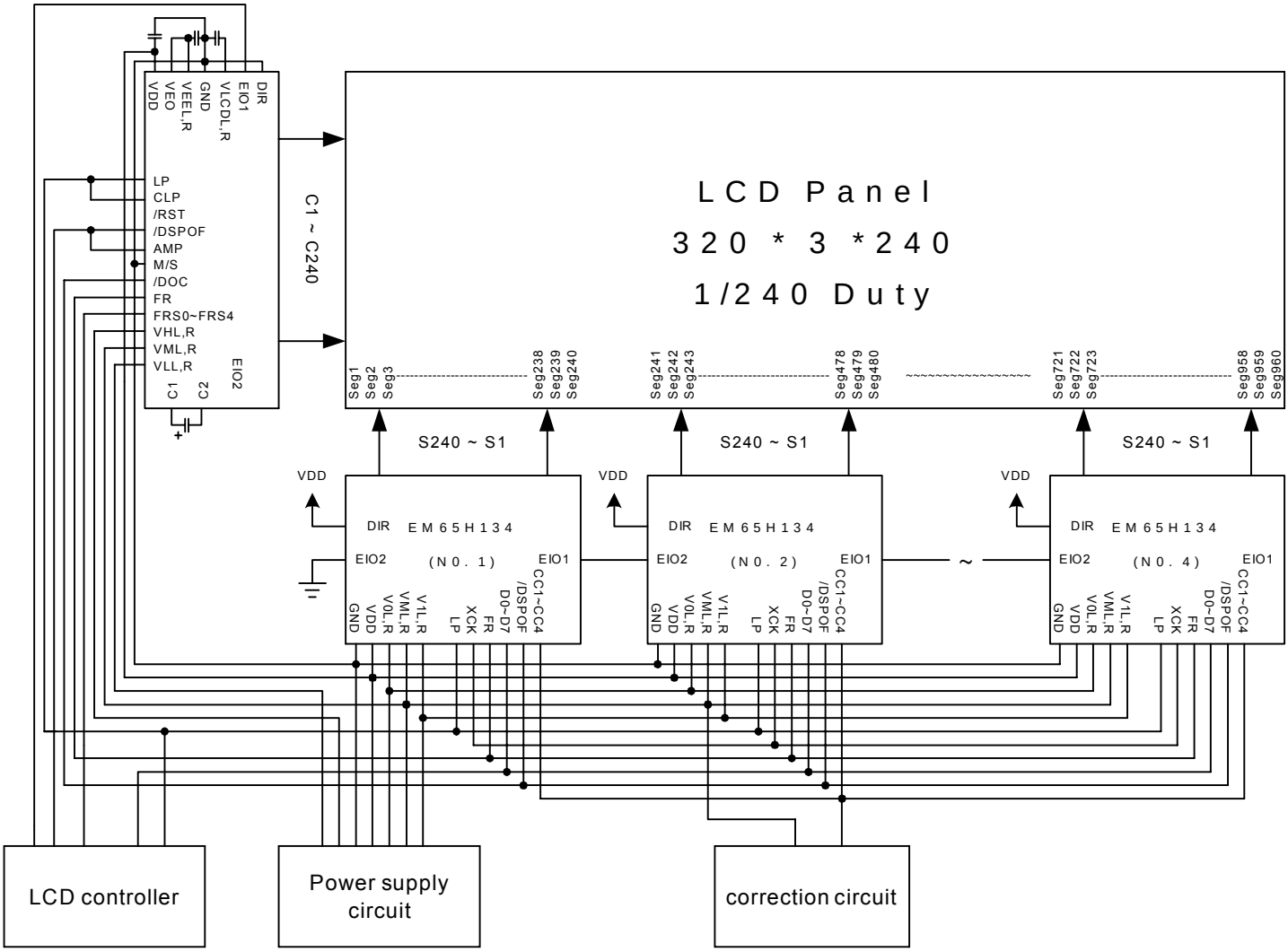


Figure 7. Application circuit