



4-Input Quad OR/NOR Gate

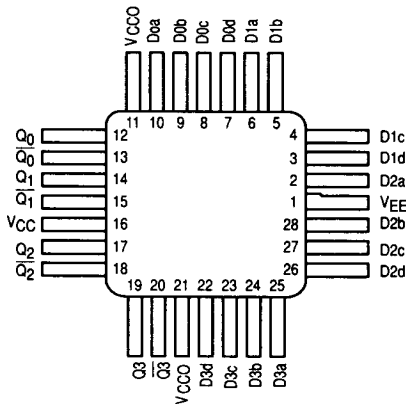
Product Preview
ELECTRICALLY TESTED PER:
10E501

The 10E501 is a quad 4-Input **OR/NOR** gate.

- 500 ps Max. Propagation Delay
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D _{0a} - D _{3d}	Data Inputs
Q ₀ - Q ₃	True Outputs
$\overline{Q_0} - \overline{Q_3}$	Inverting Outputs



Military 10E501

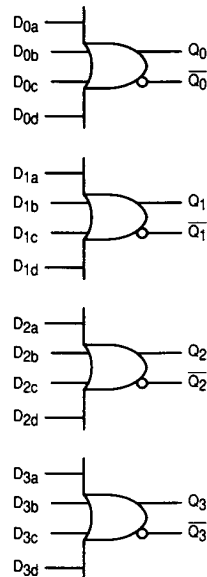


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: Planned
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA MILITARY MECL DATA

5-5

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10E501

10E Series DC CHARACTERISTICS: $V_{EE} = -5.2 V \pm 5\%$; $V_{CC} = V_{CCO} = GND^1$

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		- 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		μA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25 Ω .

DC CHARACTERISTICS: $V_{EE} = V_{EE}(\min)$ to $V_{EE}(\max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
		+ 25° C		+ 125° C		- 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High D		150		150		150	μA	
I_{EE}	Power Supply Current		36		36		36	mA	

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AC CHARACTERISTICS: $V_{EE} = V_{EE}(\min)$ to $V_{EE}(\max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
		+ 25° C		+ 125° C		- 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	500	200	500	200	500	ps	
t_{Skew}	Within-device Skew	50		50		50		ps	(Note 1)
t_{Skew}	Within-Gate Skew	25		25		25		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	300	575	300	575	300	575	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.