MOTOROLA

Product Preview

16K × 16 Bit Asynchronous/Latched Address Fast Static RAM

62995A

Commercial Plus and Mil/Aero Applications

ELECTRICALLY TESTED PER:
MPG62995A

The 62995A is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high the device can be used as an asynchronous SRAM. When latch enable (LE, DL) is low the address, data in and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0-DQ7, the lower bits. While $\overline{BWH}$ controls DQ8-DQ15, the upper bits.

Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

This device is ideally suited for systems which require wide data bus widths, cache memory and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead CQF Package

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 62995A - XX/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE:
LCC: Y

XX = Speed in ns (12, 15, 20, 25)

The letter "M" appears after the speed on LCC

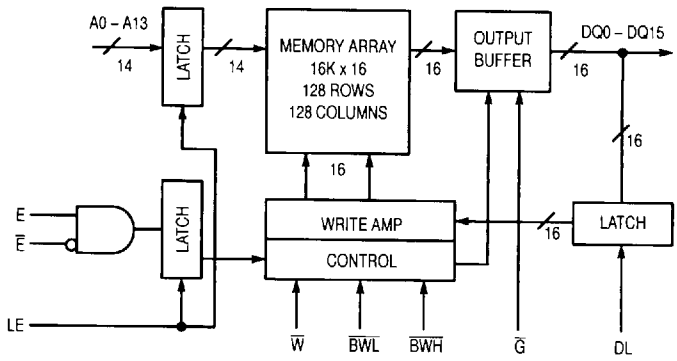
PIN NAMES

A0 – A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

This document contains information on a new product. Information and specifications herein are subject to change without notice.

BLOCK DIAGRAM



TRUTH TABLE

Es	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	LE	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High-Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High-Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data-In	I_{CC}	High-Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data-In	I_{CC}	High-Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and Addresses satisfy the specified setup and hold times for the falling edge of LE. Data-in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C)	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 55 to + 125	°C
Operating Temperature	T_A	– 55 to + 125	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = – 55 to + 125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Typ	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	5.0	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	5.0 3.3	4.5 3.0	5.5 3.6	V
Input High Voltage	V_{IH}	3.0	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	0.0	– 0.5*	0.8	V

* V_{IL}(min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Typ	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA15} I_{CCA25} I_{CCA35}	310 300 290	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OLmax}	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OHmin}	2.4	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	pF

AC TEST LOADS

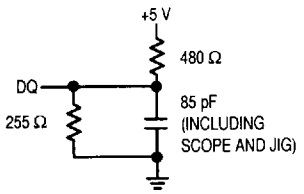


Figure 1A

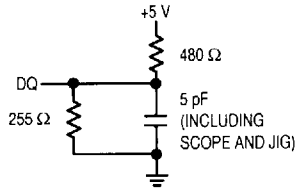
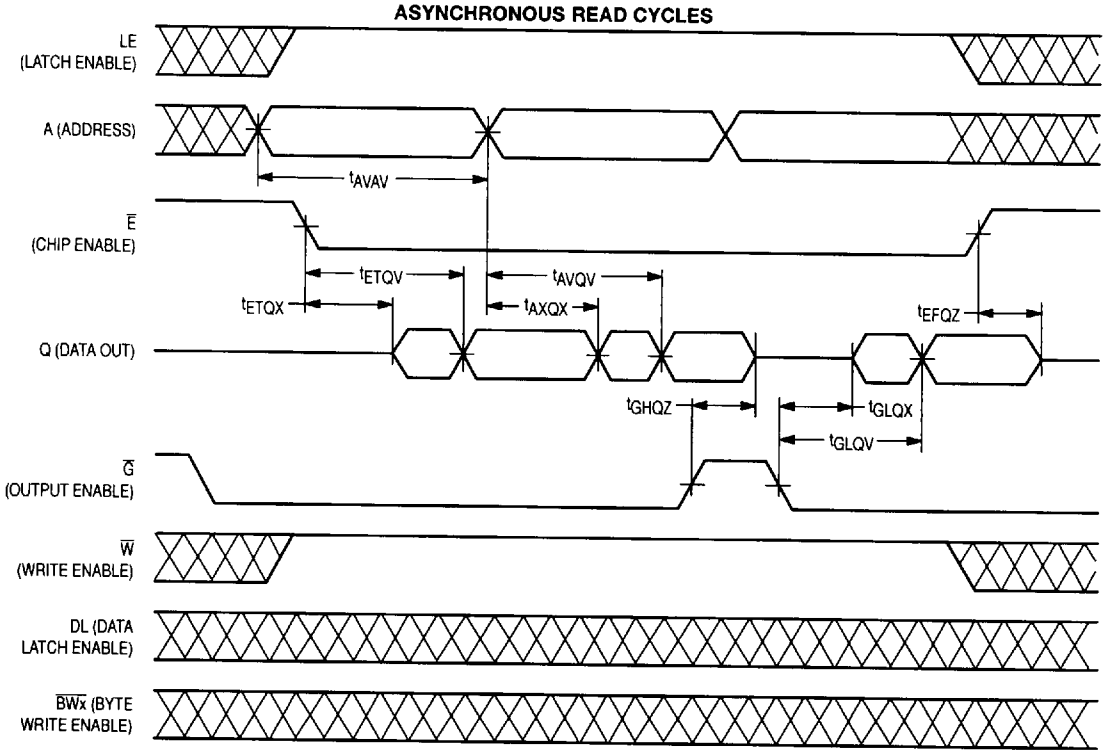
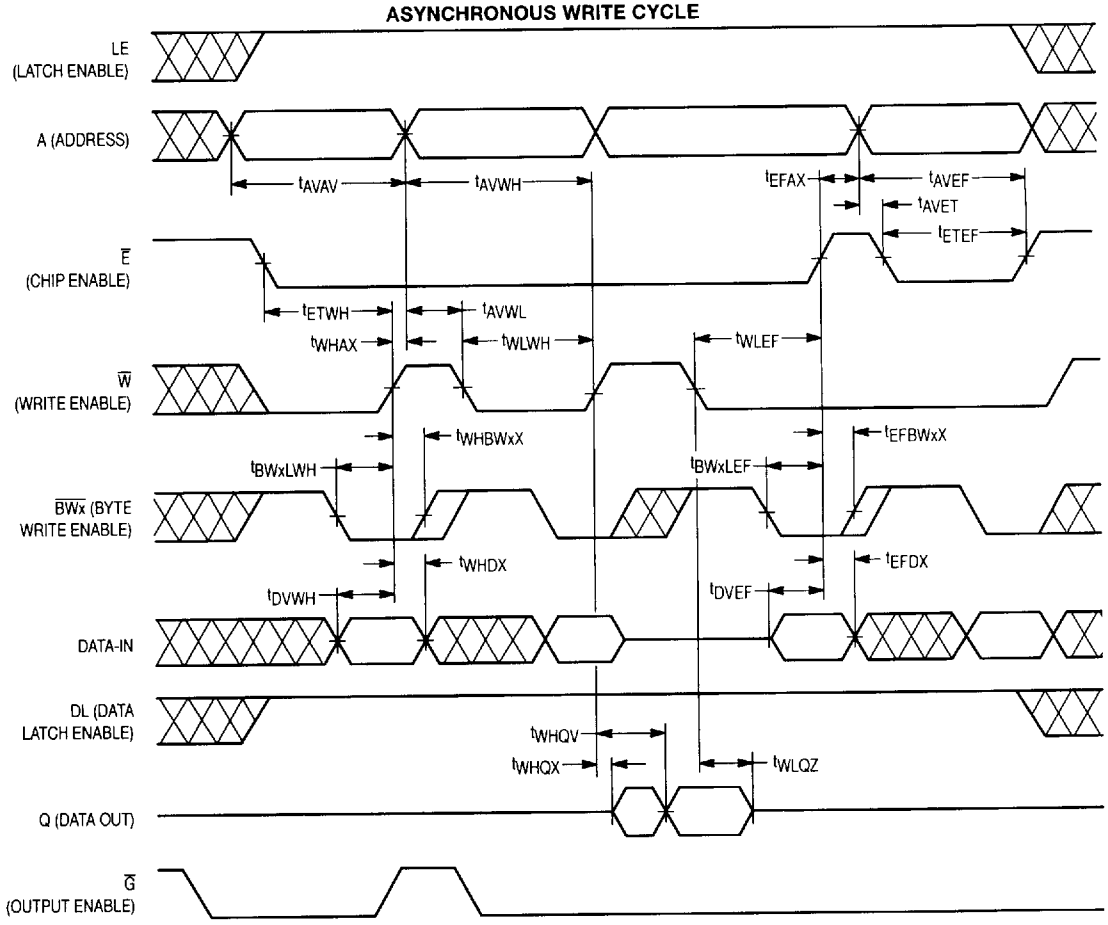


Figure 1B

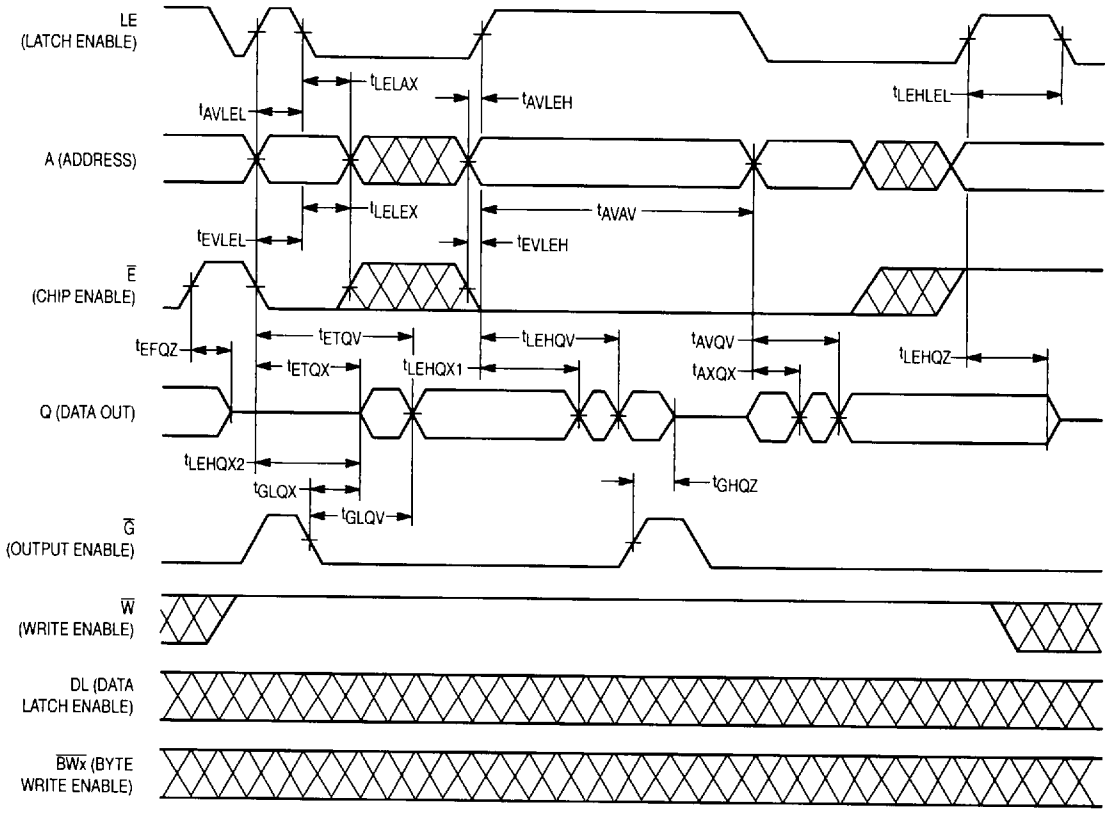
ASYNCHRONOUS READ CYCLES



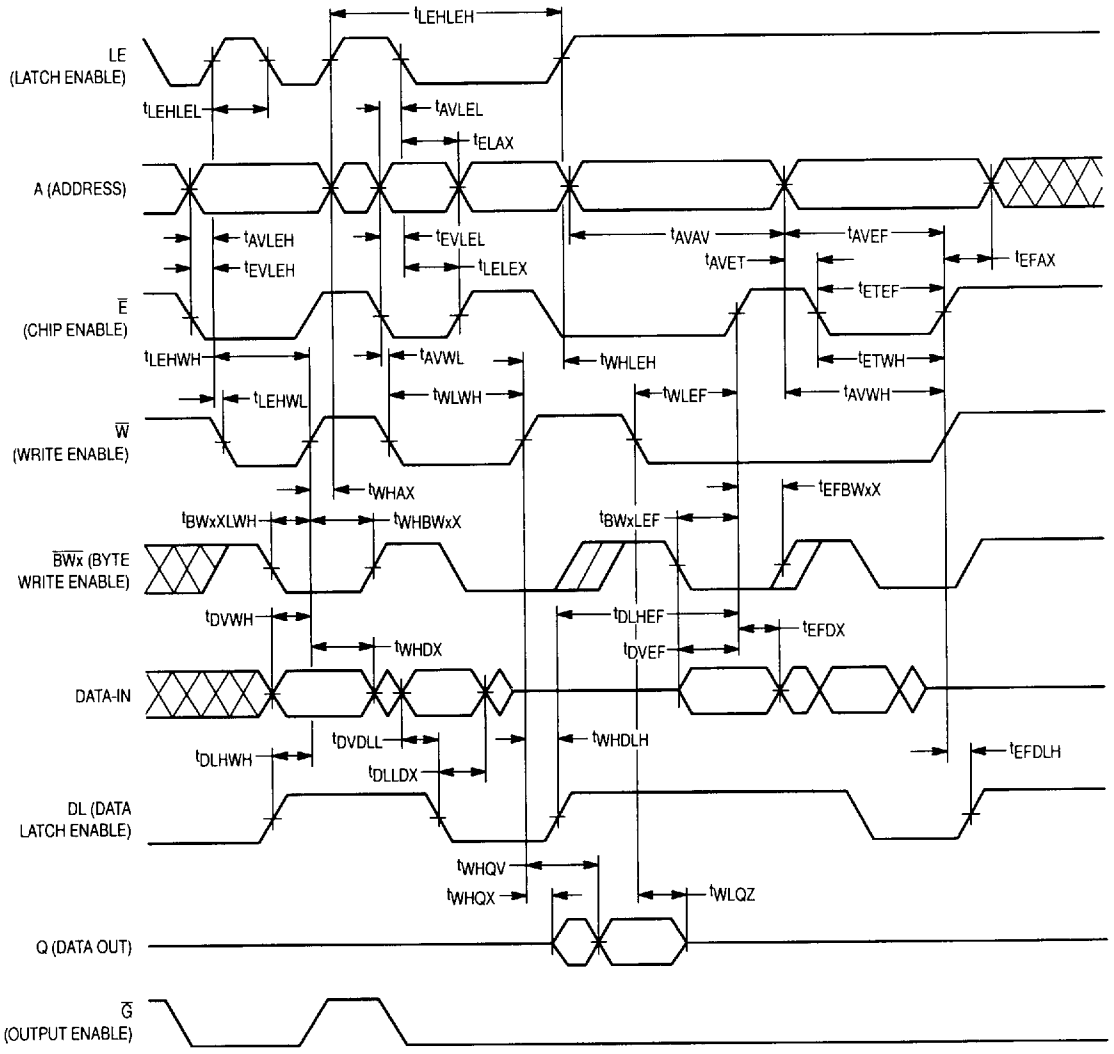
ASYNCHRONOUS WRITE CYCLE



LATCHED READ CYCLES



LATCHED WRITE CYCLES



R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola 62995A Latched SRAMs