CYPRESS SEMICONDUCTOR

CY7M194

64K x 4 SRAM Module

Features

- **Very high speed 256K SRAM module**
  —Access time of 10 ns
- **300-mil-wide hermetic DIP package**
- **Low active power**
  —1.8W (max.)
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C194 monolithic SRAMs**
- **Small PCB footprint**
  —0.36 sq. in.

Functional Description

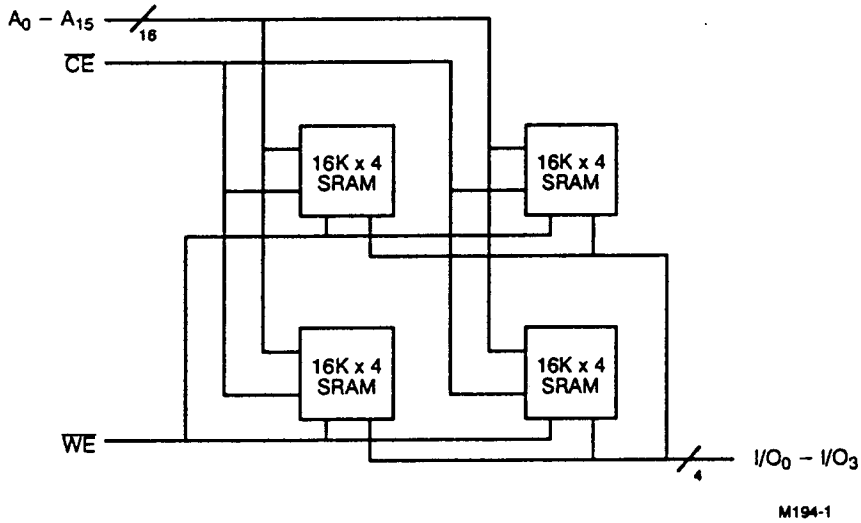
The CY7M194 is an extremely high performance 256-kilobit static RAM module organized as 65,536 words by 4 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the four output pins (I/O_0 through I/O_3).

The data output pins remain in a high-impedance state unless the module is selected and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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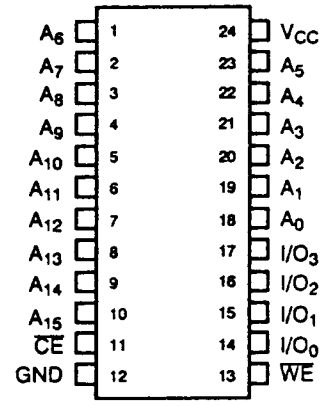
Pin Configuration

DIP
Top View



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Selection Guide

		7M194–10	7M194–12	7M194–15	7M194–20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	325	325	325	20
	Military		375	375	375
Maximum Operating Current (mA)	Commercial	200	200	200	
	Military		250	250	250

Shaded area contains preliminary information.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7M194 Min.	7M194 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.9		V
V_{IL}	Input LOW Voltage[1]				0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ ≤ V_{IL}	Com'l		325	mA
			Mil		375	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		200	mA
			Mil		250	

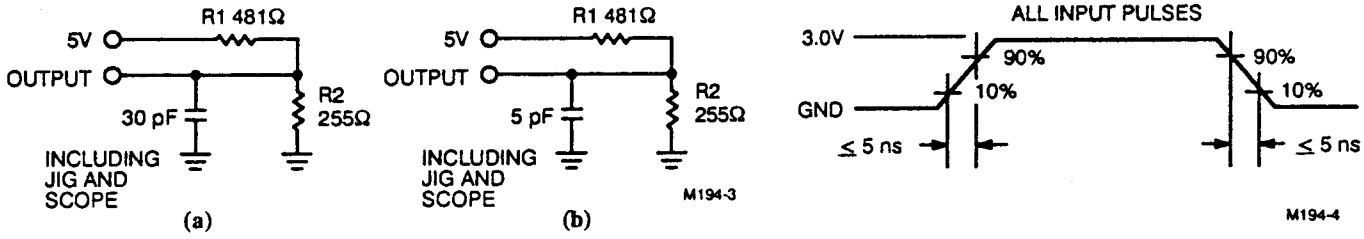
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Notes:

1. $V_{IL(min.)}$ = − 3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



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Switching Characteristics Over the Operating Range[3]

Parameter	Description	7M194–10		7M194–12		7M194–15		7M194–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z	2		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4]		6		8		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		10		15		ns
t_{AW}	Address Set-Up to Write End	8		10		10		15		ns
t_{HA}	Address Hold from Write End	1		1		1		1		ns
t_{SA}	Address Set-Up from Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		10		15		ns
t_{SD}	Data Set-Up to Write End	8		9		9		10		ns
t_{HD}	Data Hold from Write End	1		1		1		1		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	5	0	7	0	7	0	10	ns

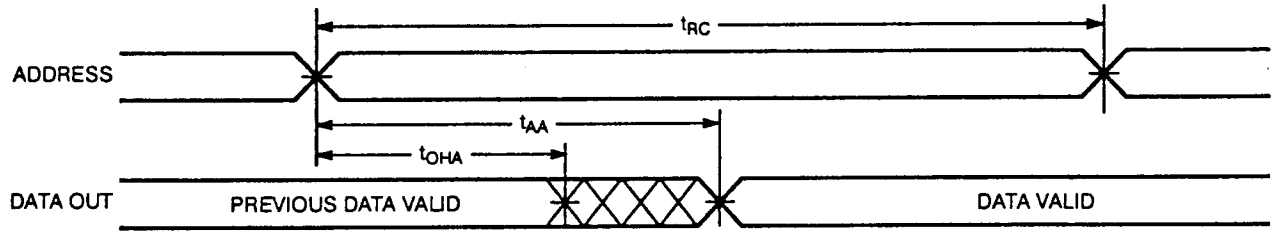
Shaded area contains preliminary information.

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms

Read Cycle No. 1[6, 7]



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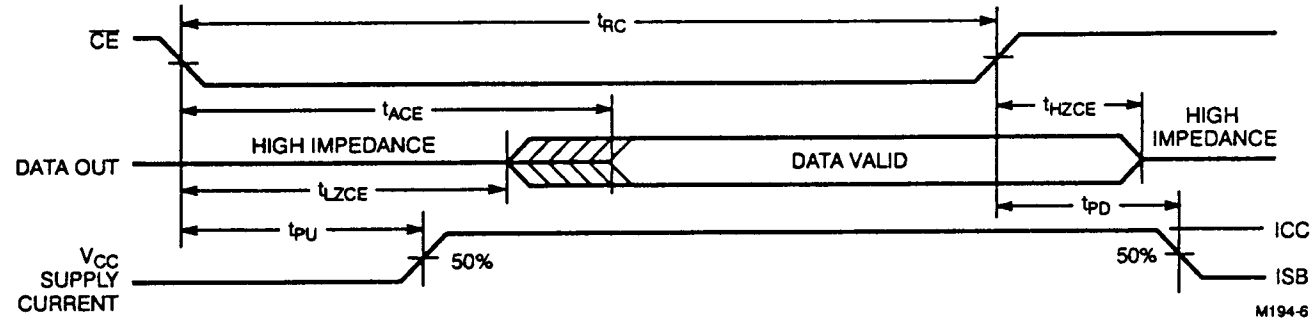
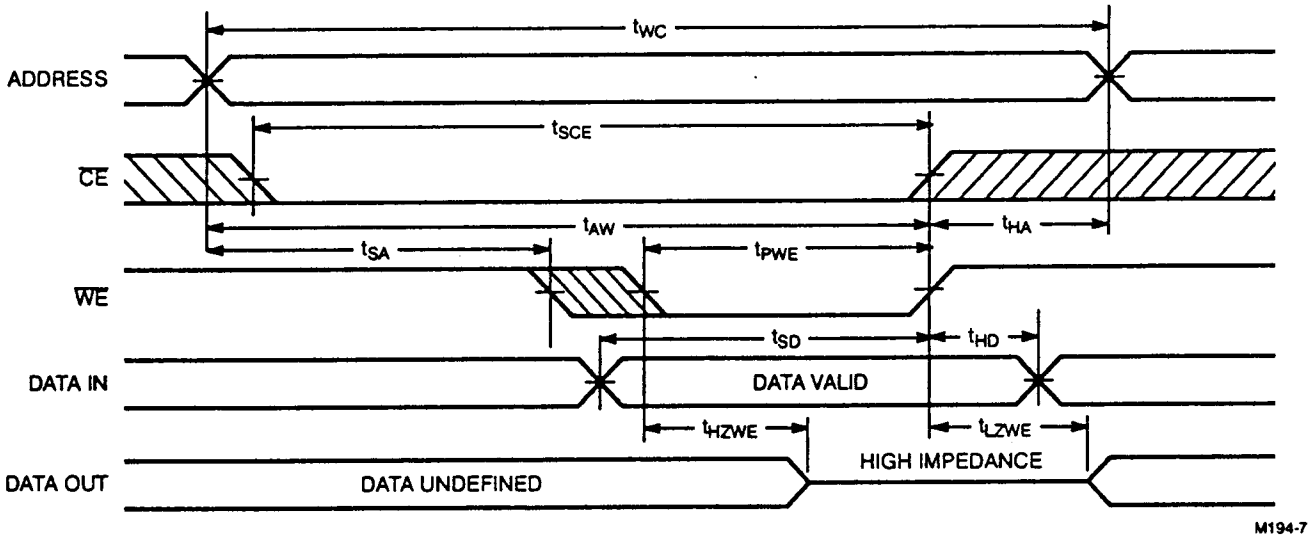
Switching Waveforms (continued)

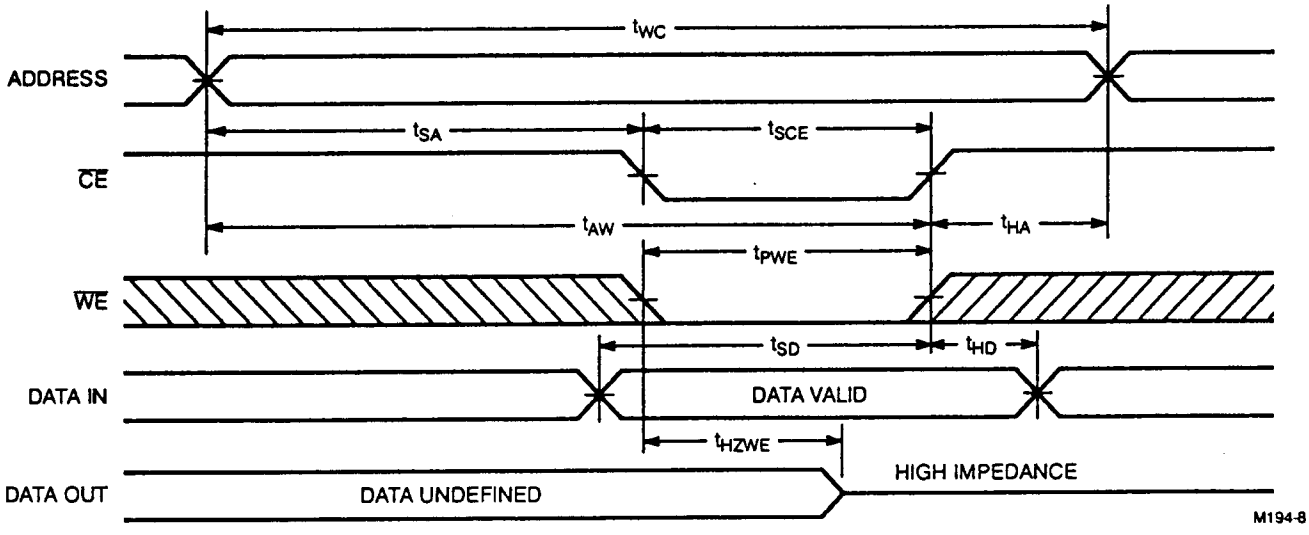
Read Cycle No. 2[7, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[5, 9]



Notes:
7. Device is continuously selected, $\overline{CE} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

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Truth Table

$\overline{CS}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read Word
L	L	Data In	Write Word

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7M194-10DC	HD08	Commercial
12	CY7M194-12DC	HD08	Commercial
	CY7M194-12DMB	HD08	Military
15	CY7M194-15DC	HD08	Commercial
	CY7M194-15DMB	HD08	Military
20	CY7M194-20DMB	HD08	Military

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Package Diagram

24-Pin DIP Module HD08