

MC100EL30

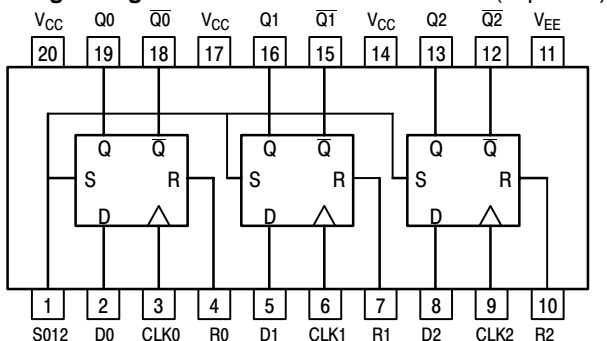
5V ECL Triple D Flip-Flop with Set and Reset

The MC100EL30 is a triple master-slave D flip flop with differential outputs. Data enters the master latch when the clock input is LOW and transfers to the slave upon a positive transition on the clock input.

In addition to a common Set input individual Reset inputs are provided for each flip flop. Both the Set and Reset inputs function asynchronous and overriding with respect to the clock inputs.

- 1200 MHz Minimum Toggle Frequency
 - 450 ps Typical Propagation Delays
 - ESD Protection: >2 KV HBM
 - The 100 Series Contains Temperature Compensation.
 - PECL Mode Operating Range: $V_{CC} = 4.2\text{ V to }5.7\text{ V}$ with $V_{EE} = 0\text{ V}$
 - NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
 - Internal Input Pulldown Resistors
 - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
 - Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
 - Transistor Count = 347 devices

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0-D2	ECL Data Inputs
R0-R2	ECL Reset Inputs
CLK0-CLK2	ECL Clock Inputs
S012	ECL Common Set Input
Q0-Q2; Q0-Q2	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R*	S*	D*	CLK*	Q	Q̄
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

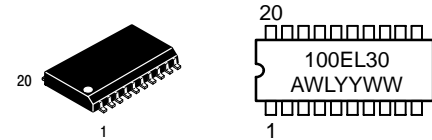
* Pins will default low when left open.



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MARKING DIAGRAM*



SO-20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL30DW	SO-20	38 Units/Rail
MC100EL30DWR2	SO-20	1000 Units/Reel

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MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8 to 0	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 to 0 -6 to 0	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		55	62		55	62		55	64	mA
V _{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V _{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V _{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.

NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= -5.0 V (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		55	62		55	62		55	64	mA
V _{OH}	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V _{OL}	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.

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AC CHARACTERISTICS $V_{CC}= 5.0\text{ V}$; $V_{EE}= 0.0\text{ V}$ or $V_{CC}= 0.0\text{ V}$; $V_{EE}= -5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency	1.0			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	460 470		690 710	480 490		710 730	500 515		730 755	ps
t_S t_H	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	400 650			400 650			400 650			ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280	450	550	280		550	ps

1. V_{EE} can vary +0.8 V / -0.5 V.

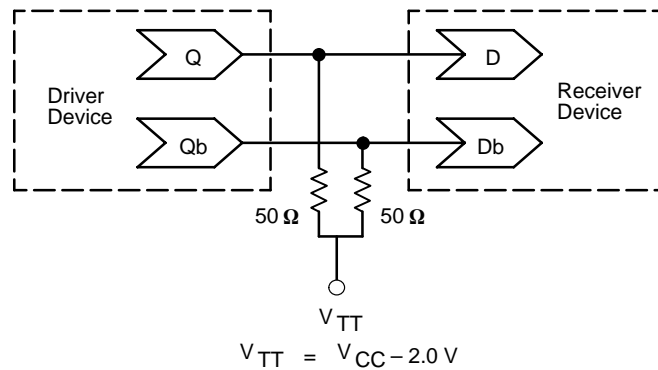


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

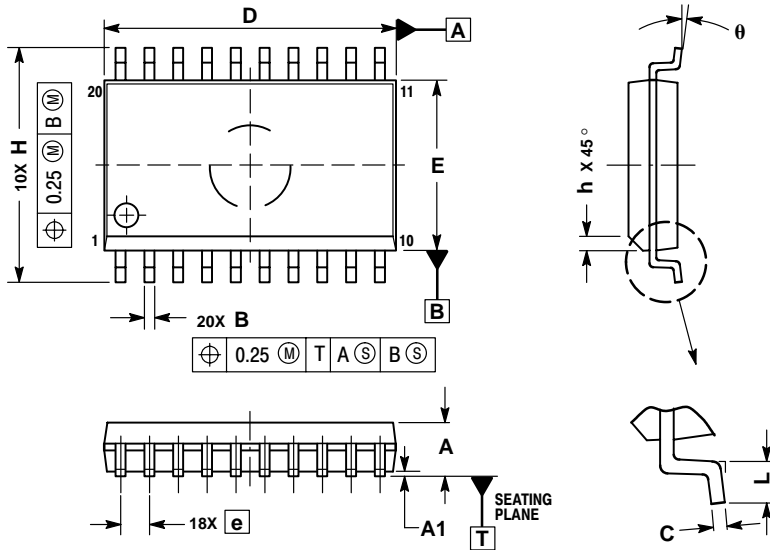
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS


SO-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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