S71WS-P based MCP Products

1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71WS-P_00 **Revision** A **Amendment** 2 **Issue Date** August 21, 2006

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Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 to 1.95V**
- **Flash access time: 80 ns, 25 ns**
- **Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz**
- **pSRAM Access time: 70 ns, 20 ns**
- **pSRAM burst frequency: 66 MHz, 80 MHz, 104 MHz**
- **Package:**
  - 8.0 x 11.6 mm MCP
- **Operating Temperature**
  - –25°C to +85°C (wireless)

The S71WS series is a product line of stacked packages and consists of:

- One or two S29WS-P NOR flash memory die
- CellularRAM die

The products covered by this document are listed in the table below.

Device	CellularRAM Density (Mb)	
	64 Mb	128 Mb
S29WS512P	S71WS512PC0	S71WS512PD0

Note:
For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

For detailed specifications, please refer to the individual data sheets.

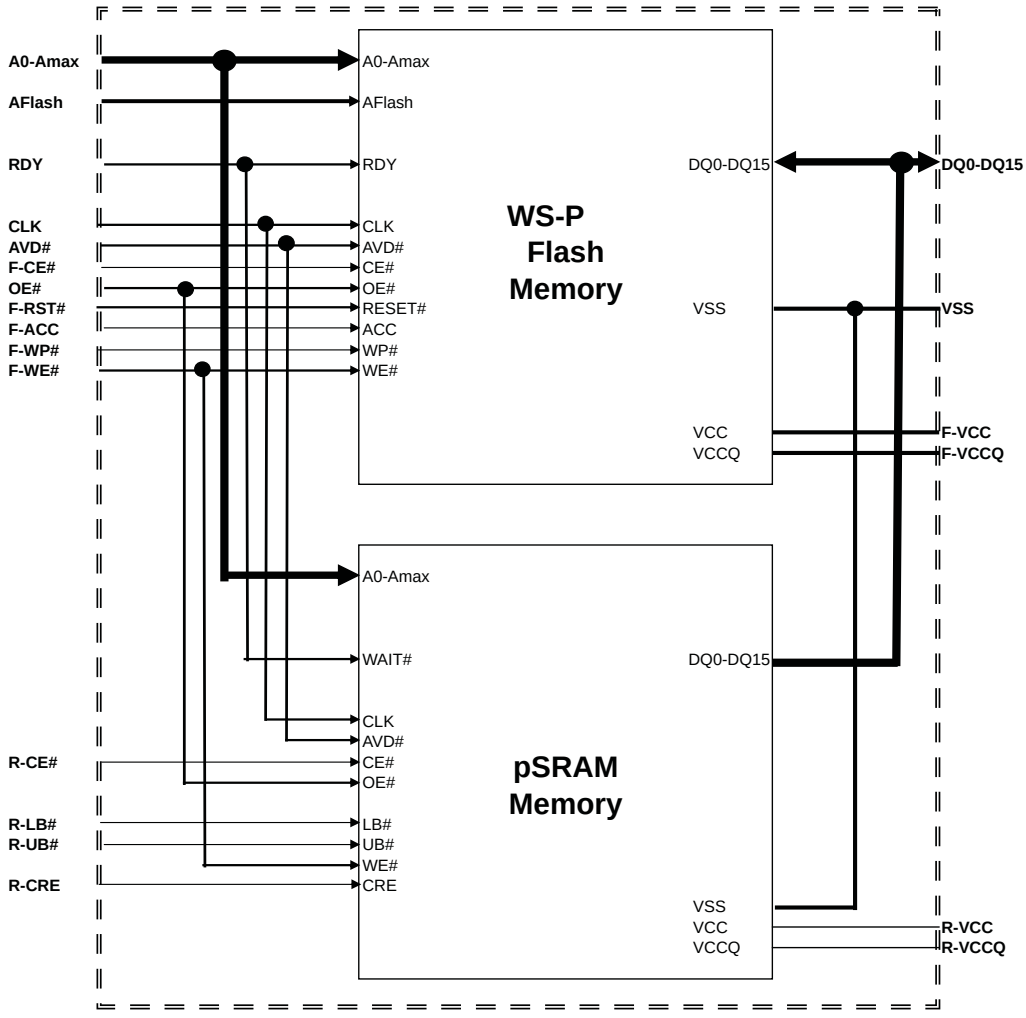
Document	Publication Identification Number (PID)
S29WS-P	S29WS-P_00
128 M CellularRAM Type 2	Cellram_04
64 M CellularRAM Type 2	Cellram_07

Publication Number S71WS-P_00 **Revision** A **Amendment** 2 **Issue Date** August 21, 2006

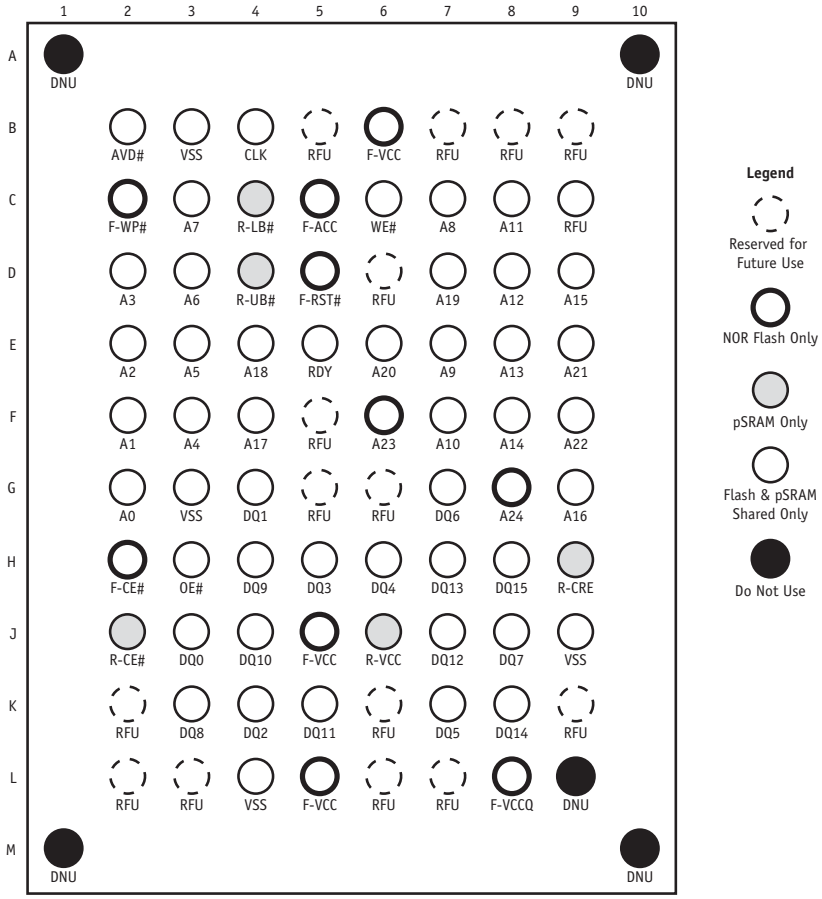
1. Product Selector Guide

Device	Model Number	Flash Density (Mb)	CellularRAM Density (Mb)	Flash Speed (MHz)	CellularRAM Speed (MHz)	CellularRAM Supplier	Package
S71WS512PD0HF3	HR	512	128	80	104	Type 2	MCP 8 x 11.6 mm
S71WS512PC0HF3	SV		64	66			
S71WS512PD0HF3	HL		128	108	104		

2. MCP Block Diagram



3. Connection Diagrams



MCP	Flash-only Addresses	Shared Addresses
S71WS512PD0	A24-A23	A22-A0
S71WS512PC0	A24-A22	A21-A0

3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150×C for prolonged periods of time.

3.2 Look-ahead Ballout for Future Designs

Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design_Scalable_Wireless_A0_E). Contact your local Spansion sales representative for more details.

3.3 NOR Flash and pSRAM Input/Output Descriptions

Amax-A0	=	NOR Flash Address inputs
DQ15-DQ0	=	Flash Data input/output, shared between NOR and ORNAND Flash. DQ0-DQ7 shared for x8 ORNAND
F-CE#	=	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
OE#	=	Output Enable input. Asynchronous relative to CLK for Burst mode.
WE#	=	Write Enable input.
F-V_{CC}	=	NOR Flash device power supply (1.7 V - 1.95V).
F-V_{CCQ}	=	Input/Output Buffer power supply.
V_{SS}	=	Ground
RFU	=	Reserved for Future Use
RDY	=	Flash ready output. Indicates the status of the Burst read. VOL = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.
CLK	=	NOR Flash Clock, shared with CLK of burst-mode pSRAM.. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	=	NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs. VIL = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. VIH= device ignores address inputs
F-RST#	=	NOR Flash hardware reset input. VIL= device resets and returns to reading array data
F-WP#	=	NOR Flash hardware write protect input. VIL = disables program and erase functions in the four outermost sectors.
F-ACC	=	NOR Flash accelerated input. At VHH, accelerates programming; automatically places device in unlock bypass mode. At VIL, disables all program and erase functions. Should be at VIH for all other conditions.
R-CE#	=	Chip-enable input for pSRAM
R-CRE	=	Control Register Enable (pSRAM). For CellularRAM only.
R-VCC	=	pSRAM Power Supply
R-UB#	=	Upper Byte Control (pSRAM)
R-LB#	=	Lower Byte Control (pSRAM)
DNU	=	Do Not Use

4. Ordering Information

The order number is formed by a valid combinations of the following:

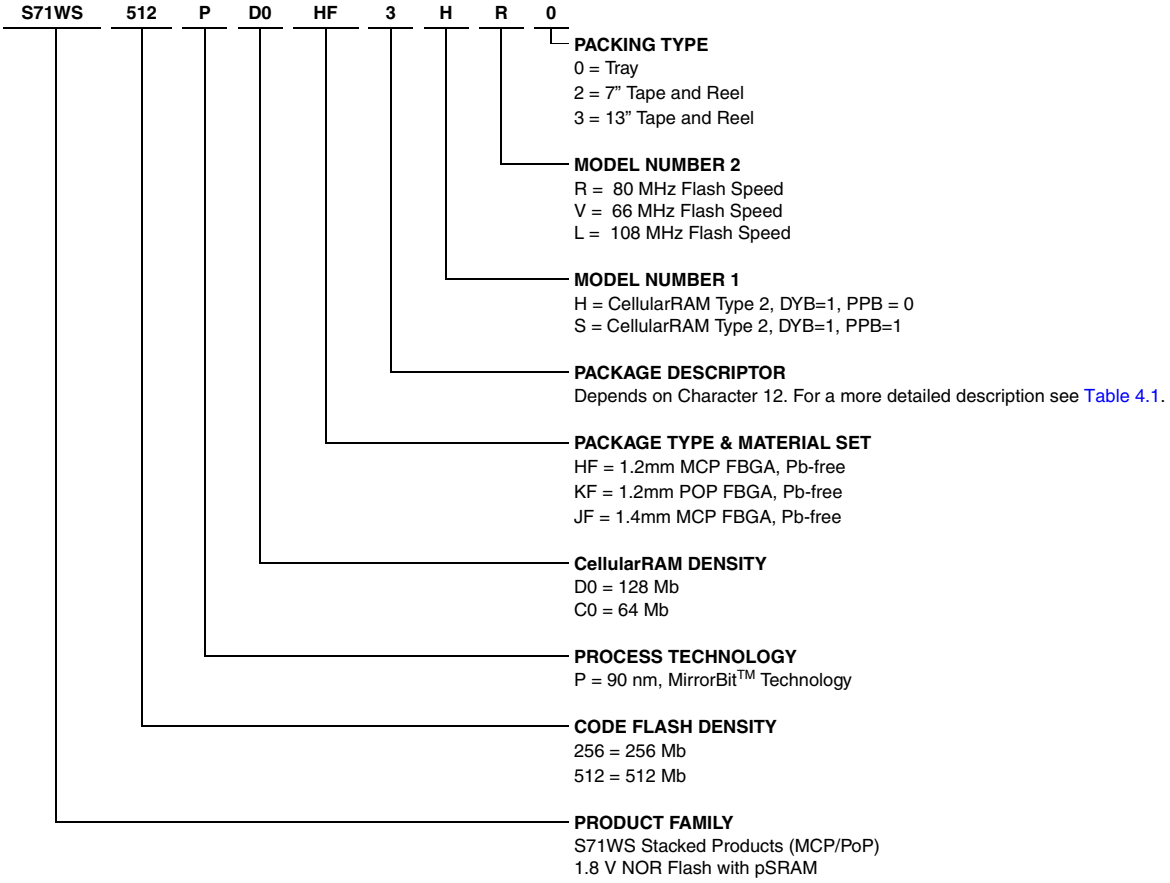


Table 4.1 Character Position Descriptions (Sheet 1 of 2)

Character 12	Character 14	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H, J, or G	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	

Table 4.1 Character Position Descriptions (Sheet 2 of 2)

Character 12	Character 14	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

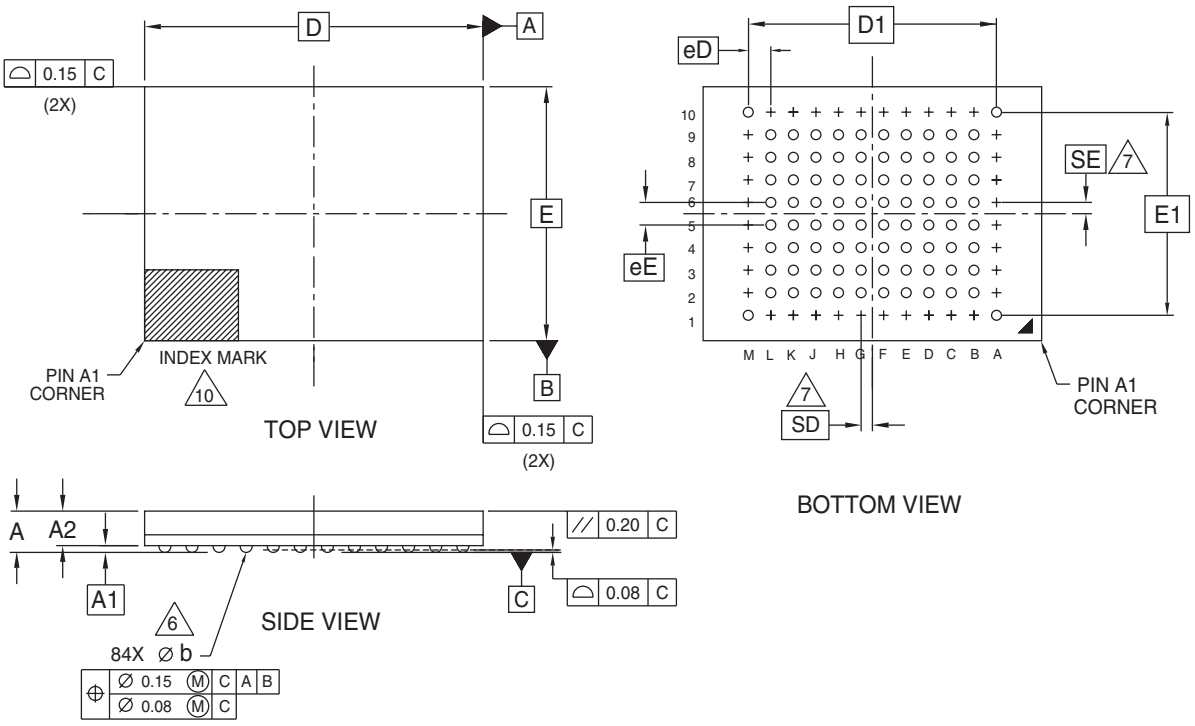
S71WS-P Valid Combinations					NOR Flash Speed (MHz)	CellularRAM Speed (MHz)	CellularRAM Supplier	Package Type	Package Markings
Device	Package & Material Set	Package Descriptor	Model Number	Packing Type					
S71WS512PD0	HF	3	HL	0, 2, 3 (Note 1)	108	104	Type 2	8 x 11.6 mm	(Note 2)
			HR		80				
S71WS512PC0			SV		66				

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 TLA084— 84-ball Fine Pitch Ball Grid Array (FBGA) 8x11.6mm Package



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		84		BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Revision History

6.1 Revision A (February 21, 2006)

Initial release.

6.2 Revision A1 (April 12, 2006)

Added the S71WS512PC0

6.3 Revision A2 (August 21, 2006)

Added the S71WS512PD0 108MHz OPN