

# Proprietary 32-bit Microcontroller

CMOS

## FR60 MB91310 Series

### MB91F312A/FV310A

#### ■ DESCRIPTION

The FR families are lines of single-chip microcontrollers based on a 32-bit high-performance RISC CPU, incorporating a variety of I/O resources for embedded control applications which require high CPU performance for high-speed processing.

The FR families are best suited for embedded applications which require high-performance CPU power for processing, such as TV and POP control.

Based on the FR30/FR40 family CPU, this FR60 family is enhanced in bus access for use in faster applications.

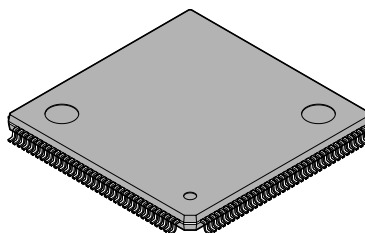
#### ■ FEATURE

- FR CPU
  - 32-bit RISC, load/store architecture with a five-stage pipeline
  - Operating frequency: 40 MHz (using PLL at an oscillation frequency of 10 MHz)
  - 16 - bit fixed length instructions (basic instructions), 1 instruction per cycle
  - Instruction set optimized for embedded applications: Memory-to-memory transfer, bit manipulation, barrel shift etc.

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#### ■ PACKAGE

144-pin plastic LQFP



(FTP-144P-M08)

# MB91310 Series

- Instructions adapted for high-level languages: Function entry/exit instructions, multiple-register load/store instructions
  - Register interlock functions: Facilitating coding in assemblers
  - On-chip multiplier supported at the instruction level.
    - Signed 32-bit multiplication: 5 cycles.
    - Signed 16-bit multiplication: 3 cycles
  - Interrupt (PC, PS save): 6 cycles, 16 priority levels
  - Harvard architecture allowing program access and data access to be executed simultaneously
  - Instruction prefetch function implemented by a four-word queue in the CPU
  - Instruction compatible with FR family
- Bus interface

This bus interface is used for macro connection. (USB, MS-IF, OSDC)

    - Operating frequency Max 20 MHz
    - 16-bit data input/output (Interface to the USB, MS-IF, and OSDC)
    - Chip-select signals can be output for completely independent eight areas allocatable in a minimum of 64 KB. The  $\overline{CS1}$ ,  $\overline{CS2}$ , and  $\overline{CS3}$  areas are reserved as follows.  $\overline{CS0}$ ,  $\overline{CS4}$ , to  $\overline{CS7}$  are Musable.
      - $\overline{CS1}$  area : USB host
      - $\overline{CS2}$  area : USB function
      - $\overline{CS3}$  area : MS-IF, OSDC
    - Basic bus cycle : 2 cycles
    - Programmable automatic wait cycle generator capable of inserting wait cycles for each area  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$  are reserved; their settings are fixed.
- Built-in RAM
    - 16 KB built RAM capacity
    - This RAM can be used as instruction RAM by writing instruction code as well as data.
- DMAC (DMA Controller)
    - Connected to five channels (ch0, ch1 → USB function; ch2 → MS-IF).
    - 3 forwarding factors (internal peripheral/software)
    - Addressing using 32 - bit full addressing mode (increment, decrement, fixed)
    - Demand transfer, burst transfer, step transfer, or block transfer
    - Selectable transfer data size: 8-bit, 16-bit, or 32-bit
- Bit search module (for REALOS)
    - Search for the position of the bit 1/0-changed first in one word from the MSB
- Reload timer (including 1 channel for REALOS)
    - 16-bit PPG timer ch3
    - The internal clock is optional from 2/8/32 en surroundings.

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- UART
  - Full duplex double buffer
  - UART : 5 channels
  - With parity / no parity selection
  - Asynchronous (start - stop synchronized) or CLK - synchronous communications selectable
  - Internal timer for dedicated baud rate
  - External clock can be used as transfer clock
  - Assorted error detection functions (for parity, frame, and overrun errors)
- I<sup>2</sup>C Interface
  - Four channels are incorporated. (ch3 can be used as two ports.)
  - Master/slave sending and receiving
  - Clock synchronization function
  - Detecting transmitting direction function
  - Bus error detection function
  - Standard mode (Max 100 Kbps)/High speed mode (Max 400 Kbps) supported
  - Arbitration function
  - Slave address and general call address detection function
  - Start condition repeat generation and detection function
  - 10 bit/7 bit slave address
- Interrupt controller
  - A total of five external interrupt lines are provided (1 nonmaskable interrupt pin ( $\overline{\text{NMI}}$ ) and 4 normal interrupt pins ( $\overline{\text{INT3}}$  to  $\text{INT0}$ ).
  - Interrupt from internal peripheral devices.
  - Programmable priorities (16 levels) for all interrupts except the non - maskable interrupt
  - Available for wakeup from STOP mode
- A/D converter
  - 10-bit resolution. 10 channels
  - Successive comparator type, conversion time : approx. 10  $\mu\text{s}$
  - Conversion modes (Single conversion mode, Scan conversion mode)
  - Startup sources (software and external triggers)
- PPG
  - 4 channels
  - Six-bit down-counter, 16-bit data register with cycle setting buffer
  - The internal clock is optional from 1/4/16/64 en surroundings.
- PWC
  - One channel (input) incorporated
  - 16 bits up counter
  - Simple LFP digital filter incorporated
- Timer
  - Lowpass filter eliminating noise below the clock setting
  - Capable of pulse width measurement according to fine settings using seven types of clock signals
  - Event count function based on pin input
  - Interval timer function using seven different clocks and one external input clock

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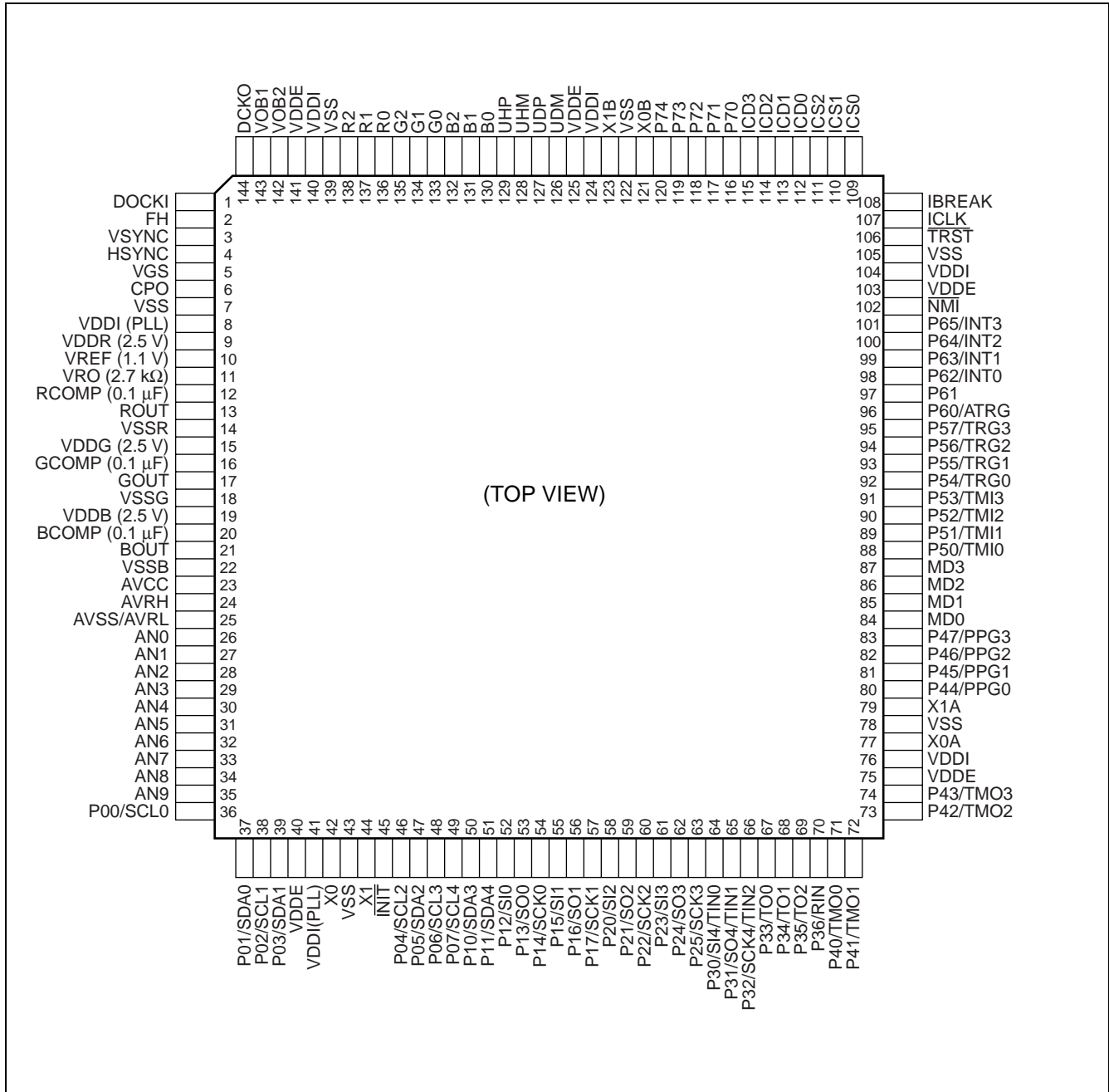
# MB91310 Series

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- USB host function
  - U.S.B 1.0 Specification
  - 8 KB of internal RAM for parameters
- USB function
  - USB 1.1 compliant full-speed double buffering
  - CONTROL IN/OUT, BULK IN/OUT, INTERRUPT IN
- OSDC function
  - High-quality OSDC integrated
  - Analog RGB interface (with internal DAC)
  - Digital RGB I/F
  - Internal dot clock generator PLL
- Other internal times
  - 16-bit PPG timer ch3(u-timer)
  - Watch dog timer
- I/O port
  - Max 72 ports
- Other features
  - Internal oscillator circuit as clock source
  - $\overline{\text{INIT}}$  is prepared as a reset terminal.
  - Watchdog timer reset. Software reset.
  - Low power consumption modes supported: Stop mode and Sleep mode
  - Gear function
  - Built-in time base timer
  - Package : LQFP-144, 0.5 mm pitch, 20 mm × 20 mm
  - CMOS technology (0.25  $\mu\text{m}$ )
  - Supply voltage: Dual power supplies at 3.3 V  $\pm$  0.3 V, 2.5 V  $\pm$  0.2 V

THE I<sup>2</sup>C LICENSE : "Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips."

## PIN ASSIGNMENT



# MB91310 Series

## ■ PIN DESCRIPTION

| Pin no. | Pin name              | Circuit type | Description                  |
|---------|-----------------------|--------------|------------------------------|
| 1       | DOCKI                 | D            | Dot clock input              |
| 2       | FH                    | D            | Vertical synchronous output  |
| 3       | VSYNC                 | D            | Horizontal synchronous input |
| 4       | HSYNC                 | D            | Vertical synchronous input   |
| 5       | VGS                   | —            | Device Ground                |
| 6       | CPO                   | K            | Charge pump output           |
| 7       | VSS                   | —            | Dot clock PLL ground         |
| 8       | VDDI (PLL)            | —            | Dot clock PLL power supply   |
| 9       | VDDR (2.5 V)          | —            | D/A power supply for R       |
| 10      | VREF (1.1 V)          | K            | Voltage reference input      |
| 11      | VRO (2.7 k $\Omega$ ) | K            | Resistor connection pin      |
| 12      | RCOMP (0.1 $\mu$ F)   | K            | Capacitor connection pin     |
| 13      | ROUT                  | K            | R output (Analog)            |
| 14      | VSSR                  | —            | D/A Ground for R             |
| 15      | VDDG (2.5 V)          | —            | D/A power supply for G       |
| 16      | GCOMP (0.1 $\mu$ F)   | K            | Capacitor connection pin     |
| 17      | GOUT                  | K            | G output (Analog)            |
| 18      | VSSG                  | —            | Device Ground for G          |
| 19      | VDDB (2.5 V)          | —            | D/A power supply for B       |
| 20      | BCOMP (0.1 $\mu$ F)   | K            | Capacitor connection pin     |
| 21      | BOUT                  | K            | B output (Analog)            |
| 22      | VSSB                  | —            | D/A Ground for B             |
| 23      | AVCC                  | —            | A/D Power Supply             |
| 24      | AVRH                  | —            | A/D referense power supply   |
| 25      | AVSS/AVRL             | —            | A/D Ground                   |
| 26      | AN0                   | E            | Analog input                 |
| 27      | AN1                   | E            | Analog input                 |
| 28      | AN2                   | E            | Analog input                 |
| 29      | AN3                   | E            | Analog input                 |
| 30      | AN4                   | E            | Analog input                 |
| 31      | AN5                   | E            | Analog input                 |
| 32      | AN6                   | E            | Analog input                 |
| 33      | AN7                   | E            | Analog input                 |
| 34      | AN8                   | E            | Analog input                 |
| 35      | AN9                   | E            | Analog input                 |

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# MB91310 Series

| Pin no. | Pin name                 | Circuit type | Description                |
|---------|--------------------------|--------------|----------------------------|
| 36      | P00                      | C            | General-purpose port       |
|         | SCL0                     |              | I <sup>2</sup> C clock pin |
| 37      | P01                      | C            | General-purpose port       |
|         | SDA0                     |              | I <sup>2</sup> C Data pin  |
| 38      | P02                      | C            | General-purpose port       |
|         | SCL1                     |              | I <sup>2</sup> C Clock     |
| 39      | P03                      | C            | General-purpose port       |
|         | SDA1                     |              | I <sup>2</sup> C Data pin  |
| 40      | VDDE                     | —            | 3.3 V Power Supply         |
| 41      | VDDI (PLL)               | —            | 2.5 V Power Supply         |
| 42      | X0                       | A            | 10-MHz oscillation pin     |
| 43      | VSS                      | —            | Ground                     |
| 44      | X1                       | A            | 10-MHz oscillation pin     |
| 45      | $\overline{\text{INIT}}$ | B            | Initial (reset) pin        |
| 46      | P04                      | C            | General-purpose port       |
|         | SCL2                     |              | I <sup>2</sup> C clock     |
| 47      | P05                      | C            | General-purpose port       |
|         | SDA2                     |              | I <sup>2</sup> C Data pin  |
| 48      | P06                      | N            | General-purpose port       |
|         | SCL3                     |              | I <sup>2</sup> C clock     |
| 49      | P07                      |              | General-purpose ports      |
|         | SCL4                     |              | I <sup>2</sup> C clock     |
| 50      | P10                      | N            | General-purpose port       |
|         | SDA3                     |              | I <sup>2</sup> C data pin  |
| 51      | P11                      |              | General-purpose port       |
|         | SDA4                     |              | I <sup>2</sup> C data pin  |
| 52      | P12                      | C            | General-purpose port       |
|         | SI0                      |              | UART0 serial input         |
| 53      | P13                      | C            | General-purpose port       |
|         | SO0                      |              | UART0 serial output        |
| 54      | P14                      | C            | General-purpose port       |
|         | SCK0                     |              | UART0 clock input/output   |
| 55      | P15                      | C            | General-purpose port       |
|         | SI1                      |              | UART1 serial input         |
| 56      | P16                      | C            | General-purpose port       |
|         | SO1                      |              | UART1 serial output        |

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# MB91310 Series

| Pin no. | Pin name | Circuit type | Description                   |
|---------|----------|--------------|-------------------------------|
| 57      | P17      | C            | General-purpose port          |
|         | SCK1     |              | UART1 clock input/output      |
| 58      | P20      | C            | General-purpose port          |
|         | SI2      |              | UART2 serial input            |
| 59      | P21      | C            | General-purpose port          |
|         | SO2      |              | UART2 serial output           |
| 60      | P22      | C            | General-purpose port          |
|         | SCK2     |              | UART2 clock input/output      |
| 61      | P23      | C            | General-purpose port          |
|         | SI3      |              | UART3 serial input            |
| 62      | P24      | C            | General-purpose port          |
|         | SO3      |              | UART3 serial output           |
| 63      | P25      | C            | General-purpose port          |
|         | SCK3     |              | UART3 clock input/output      |
| 64      | P30      | C            | General-purpose port          |
|         | SI4      |              | UART4 serial input            |
|         | TIN0     |              | Reload timer 0 trigger input  |
| 65      | P31      | C            | General-purpose port          |
|         | SO4      |              | UART4 serial output           |
|         | TIN1     |              | Reload timer 1 trigger input  |
| 66      | P32      | C            | General-purpose port          |
|         | SCK4     |              | UART4 clock input/output      |
|         | TIN2     |              | Reload timer 2 trigger input  |
| 67      | P33      | C            | General-purpose port          |
|         | TO0      |              | Reload timer 0 output         |
| 68      | P34      | C            | General-purpose port          |
|         | TO1      |              | Reload timer 1 output         |
| 69      | P35      | C            | General-purpose port          |
|         | TO2      |              | Reload timer 2 output         |
| 70      | P36      | C            | General-purpose port          |
|         | RIN      |              | PWC input                     |
| 71      | P40      | C            | General-purpose port          |
|         | TMO0     |              | Multi-function timer 0 output |
| 72      | P41      | C            | General-purpose port          |
|         | TMO1     |              | Multi-function timer 1 output |

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# MB91310 Series

| Pin no. | Pin name | Circuit type | Description                   |
|---------|----------|--------------|-------------------------------|
| 73      | P42      | C            | General-purpose port          |
|         | TMO2     |              | Multi-function timer 2 output |
| 74      | P43      | C            | General-purpose port          |
|         | TMO3     |              | Multi-function timer 3 output |
| 75      | VDDE     | —            | 3.3 V power supply            |
| 76      | VDDI     | —            | 2.5 V power supply            |
| 77      | X0A      | A            | 32 kHz oscillation pin        |
| 78      | VSS      | —            | Ground                        |
| 79      | X1A      | A            | 32 kHz oscillation pin        |
| 80      | P44      | C            | General-purpose port          |
|         | PPG0     |              | PPG0 output                   |
| 81      | P45      | C            | General-purpose port          |
|         | PPG1     |              | PPG1 output                   |
| 82      | P46      | C            | General-purpose port          |
|         | PPG2     |              | PPG2 output                   |
| 83      | P47      | C            | General-purpose port          |
|         | PPG3     |              | PPG3 output                   |
| 84      | MD0      | F            | Mode Pins                     |
| 85      | MD1      | F            | Mode Pins                     |
| 86      | MD2      | F            | Mode Pins                     |
| 87      | MD3      | F            | Mode Pins (ground)            |
| 88      | P50      | C            | General-purpose port          |
|         | TMI0     |              | Multi-function timer 0 input  |
| 89      | P51      | C            | General-purpose port          |
|         | TMI1     |              | Multi-function timer 1 input  |
| 90      | P52      | C            | General-purpose port          |
|         | TMI2     |              | Multi-function timer 2 input  |
| 91      | P53      | C            | General-purpose port          |
|         | TMI3     |              | Multi-function timer 3 input  |
| 92      | P54      | —            | General-purpose port          |
|         | TRG0     |              | PPG0 trigger input            |
| 93      | P55      | —            | General-purpose port          |
|         | TRG1     |              | PPG1 trigger input            |
| 94      | P56      | —            | General-purpose port          |
|         | TRG2     |              | PPG2 trigger input            |

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# MB91310 Series

| Pin no. | Pin name                 | Circuit type | Description                   |
|---------|--------------------------|--------------|-------------------------------|
| 95      | P57                      | C            | General-purpose port          |
|         | TRG3                     |              | PPG3 trigger input            |
| 96      | P60                      | C            | General-purpose port          |
|         | ATRG                     |              | A/D conversion trigger input  |
| 97      | P61                      | C            | General-purpose port          |
| 98      | P62                      | O            | General-purpose port          |
|         | INT0                     |              | External interrupt input 0    |
| 99      | P63                      | O            | General-purpose port          |
|         | INT1                     |              | External interrupt input 1    |
| 100     | P64                      | O            | General-purpose port          |
|         | INT2                     |              | External interrupt input 2    |
| 101     | P65                      | O            | General-purpose port          |
|         | INT3                     |              | External interrupt input 3    |
| 102     | $\overline{\text{NMI}}$  | B            | $\overline{\text{NMI}}$ input |
| 103     | VDDE                     | —            | 3.3 V power supply            |
| 104     | VDDI                     | —            | 2.5 V power supply            |
| 105     | VSS                      | —            | Ground                        |
| 106     | $\overline{\text{TRST}}$ | B            | DSU tool reset                |
| 107     | ICLK                     | C            | DSU clock                     |
| 108     | IBREAK                   | L            | DSU break                     |
| 109     | ICS0                     | M            | DSU status                    |
| 110     | ICS1                     | M            | DSU status                    |
| 111     | ICS2                     | M            | DSU status                    |
| 112     | ICD0                     | H            | DSU data                      |
| 113     | ICD1                     | H            | DSU data                      |
| 114     | ICD2                     | H            | DSU data                      |
| 115     | ICD3                     | H            | DSU data                      |
| 116     | P70                      | I            | General-purpose port          |
| 117     | P71                      | C            | General-purpose port          |
| 118     | P72                      | C            | General-purpose port          |
| 119     | P73                      | C            | General-purpose port          |
| 120     | P74                      | H            | General-purpose port          |
| 121     | X0B                      | A            | 48 MHz oscillation pin        |
| 122     | VSS                      | —            | Ground                        |

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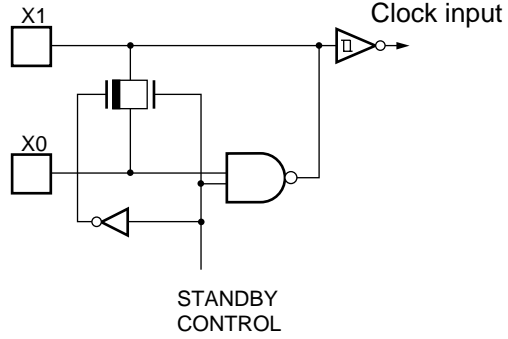
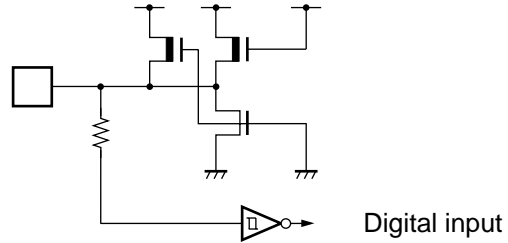
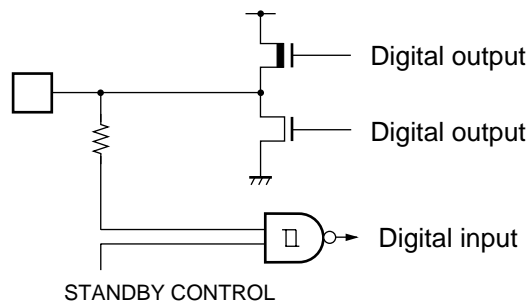
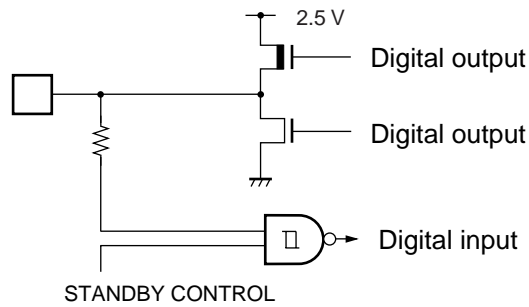
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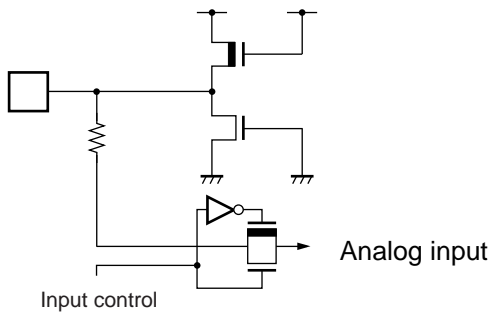
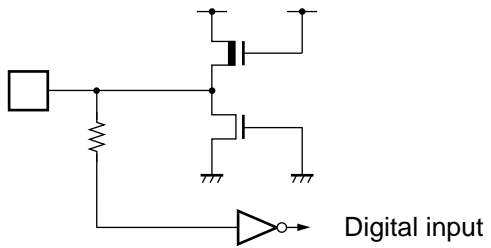
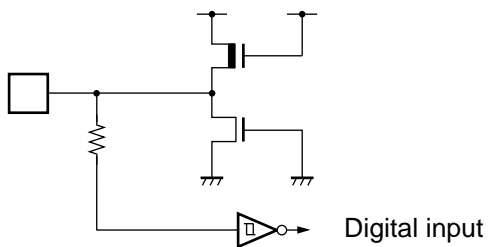
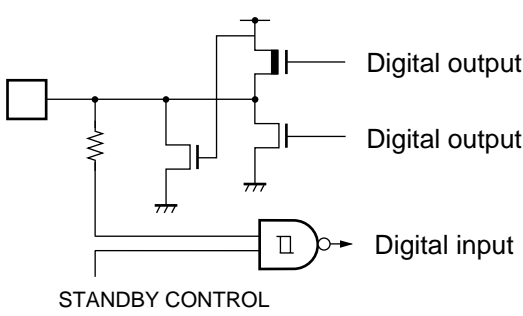
| Pin no. | Pin name | Circuit type | Description                         |
|---------|----------|--------------|-------------------------------------|
| 123     | X1B      | A            | 48 MHz oscillation pin              |
| 124     | VDDI     | —            | 2.5 V power supply                  |
| 125     | VDDE     | —            | 3.3 V power supply                  |
| 126     | UDM      | USB          | USB-Function                        |
| 127     | UDP      |              | USB-Function                        |
| 128     | UHM      | USB          | USB-Host                            |
| 129     | UHP      |              | USB-Host                            |
| 130     | B0       | D            | RGB digital output                  |
| 131     | B1       | D            | RGB digital output                  |
| 132     | B2       | D            | RGB digital output                  |
| 133     | G0       | D            | RGB digital output                  |
| 134     | G1       | D            | RGB digital output                  |
| 135     | G2       | D            | RGB digital output                  |
| 136     | R0       | D            | RGB digital output                  |
| 137     | R1       | D            | RGB digital output                  |
| 138     | R2       | D            | RGB digital output                  |
| 139     | VSS      | —            | Ground                              |
| 140     | VDDI     | —            | 2.5 V power supply                  |
| 141     | VDDE     | —            | 3.3 V power supply                  |
| 142     | VOB2     | D            | Semi Transparent color periodoutput |
| 143     | VOB1     | D            | OSD display period output           |
| 144     | DCKO     | D            | Dot clock output                    |

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## ■ I/O CIRCUIT TYPE

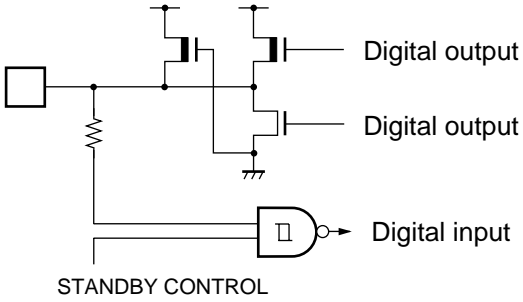
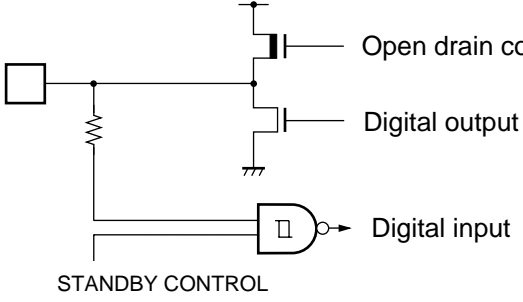
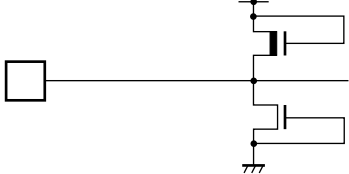
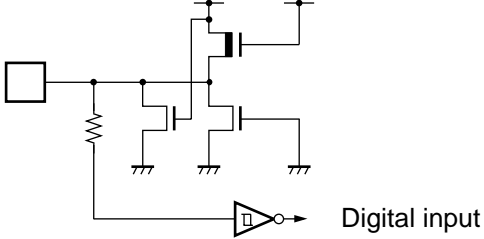
| Type | Circuit type  | Remarks   |
|------|---|---|
| A    |    | <ul style="list-style-type: none"> <li>Oscillation circuit</li> </ul>   |
| B    |   | <ul style="list-style-type: none"> <li>CMOS hysteresis input<br/>With pull-up resistance</li> </ul>                                 |
| C    |  | <ul style="list-style-type: none"> <li>CMOS level output.<br/>CMOS level hysteresis input<br/>With standby control</li> </ul>       |
| D    |  | <ul style="list-style-type: none"> <li>2.5 V CMOS level output.<br/>CMOS level hysteresis input<br/>With standby control</li> </ul> |

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| Type | Circuit type  | Remarks   |
|------|---|---|
| E    |    | <ul style="list-style-type: none"> <li>• Analog input with switch</li> </ul>  |
| F    |   | <ul style="list-style-type: none"> <li>• CMOS level input<br/>Without standby control</li> </ul>  |
| G    |  | <ul style="list-style-type: none"> <li>• CMOS level hysteresis input<br/>Without standby control</li> </ul>   |
| H    |  | <ul style="list-style-type: none"> <li>• CMOS level output<br/>Hysteresis input<br/>Standby control provided<br/>Pull-down resistor provided</li> </ul> |

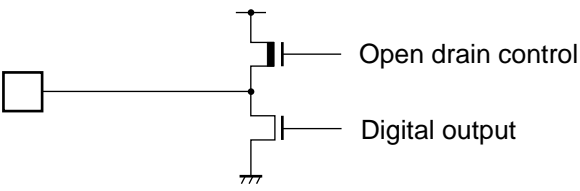
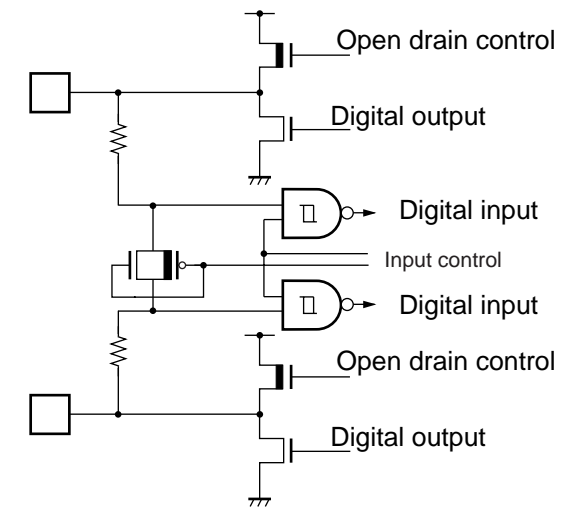
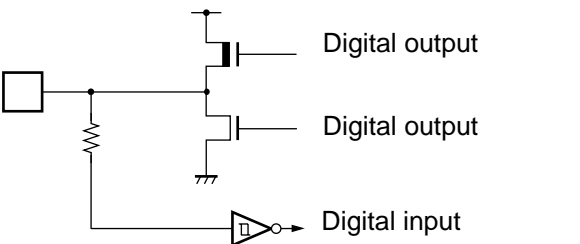
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# MB91310 Series

| Type | Circuit type  | Remarks  |
|------|---|--|
| I    |    | <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>Hysteresis input</li> <li>Standby control provided</li> <li>Pull-up resistor provided</li> </ul> |
| J    |   | <ul style="list-style-type: none"> <li>• Open drain output</li> <li>CMOS level hysteresis input</li> <li>With standby control</li> </ul>                             |
| K    |  | <ul style="list-style-type: none"> <li>• Analog pin</li> </ul>   |
| L    |  | <ul style="list-style-type: none"> <li>• CMOS hysteresis input</li> <li>With pull-down resistance</li> </ul>   |

(Continued)

(Continued)

| Type | Circuit type  | Remarks   |
|------|---|---|
| M    |    | <ul style="list-style-type: none"> <li>• CMOS level output</li> </ul>   |
| N    |   | <ul style="list-style-type: none"> <li>• Two ports for I<sup>2</sup>C</li> <li>• CMOS hysteresis input</li> <li>• CMOS output</li> <li>• Stop control provided</li> </ul> |
| O    |  | <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS hysteresis input</li> </ul>  |

## ■ HANDLING DEVICES

- Preventing Latchup

Latch-up may occur in a CMOS IC if a voltage greater than  $V_{CC}$  or less than  $V_{SS}$  is applied to an input or output pin or if an above-rating voltage is applied between  $V_{CC}$  and  $V_{SS}$ . A latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

- Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- About Power Supply Pins

If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally. The power pins should be connected to  $V_{CC}$  and  $V_{SS}$  of this device at the lowest possible impedance from the current supply source.

It is also advisable to connect a ceramic bypass capacitor of approximately  $0.1\mu\text{F}$  between  $V_{CC}$  and  $V_{SS}$  near this device.

- About Crystal Oscillator Circuit

Noise near the X0 and X1 pin may cause the device to malfunction. When designing a PC board using the device, place the X0 and X1 pins, the crystal (or ceramic) oscillator, and the bypass capacitor leading to the ground as close to one another as possible.

It is strongly recommended to design PC board so that X0 and X1 pins are surrounded by grounding area for stable operation.

- About Mode Pins (MD0 to MD3)

These pins should be connected directly to  $V_{CC}$  or  $V_{SS}$ . To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and  $V_{CC}$  or  $V_{SS}$  is as short as possible and the connection impedance is low.

- About Tool Reset Pin ( $\overline{\text{TRST}}$ )

This pin must input the same signal as that to  $\overline{\text{INIT}}$  when the tool is not used. Apply the same treatment to mass-produced products as well.

- Operation at Start-up

A setting initialization reset (INIT) must always be performed via the  $\overline{\text{INIT}}$  pin immediately after the power supply is turned on or recycled.

Immediately after the power supply is turned on, hold the Low level input to the  $\overline{\text{INIT}}$  pin for the settling time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit. (For INIT via the  $\overline{\text{INIT}}$  pin, the oscillation stabilization wait time setting is initialized to the minimum value.)



- Oscillation Input at Power-ON

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

- Notes on Power-ON/shut-down

Cautions to take when turning on/off VDDI (2.5-V internal power supply) and VDDE (3.3-V external-pin power supply)

Do not apply VDDE (external) alone continuously (for over an indication of one minute) with VDDI (internal) disconnected not to cause a reliability problem with the LSI.

When VDDE (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

---

When the power is turned on    VDDI (internal)→Analog→VDDE (external)→Signal

When the power is turned off    Signal→VDDE (external)→Analog→VDDI (internal)

---

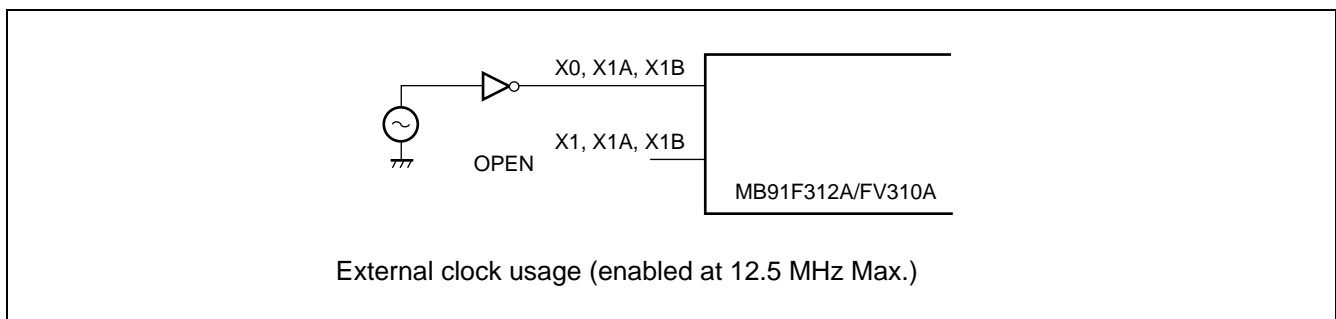
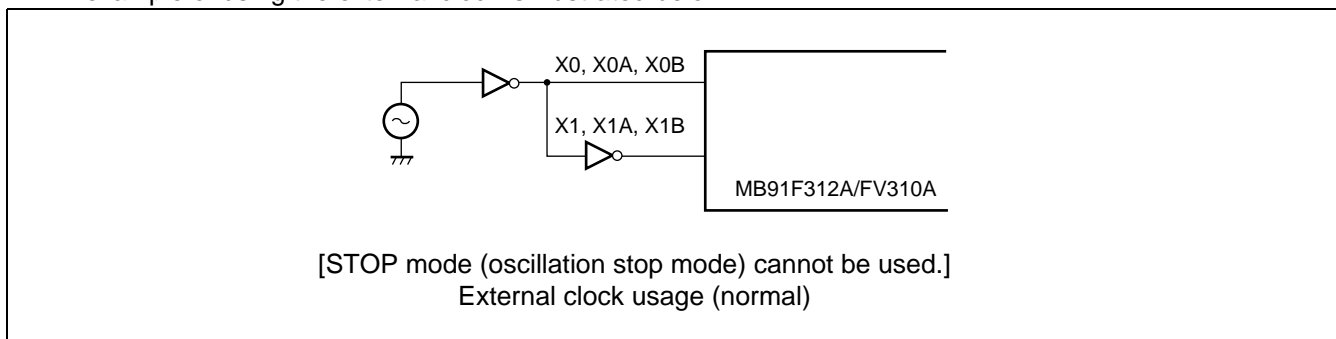
- Undefined Output on Power-ON

When the power supply is turned on, the output pin may remain indeterminate until the internal power supply becomes stable.

- About the attention when the external clock is used

When the external clock is used, in principle, supply a clock signal to the X0 (X0A, X0B) pin and an opposite-phase clock signal to the X1 (X1A, X1B) pin at the same time. However, In this case, the stop mode must not be used. (This is because, in STOP mode, the X1 (X1A, X1B) pin stops at "H" output.) At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 (X0A, X0B) pin.

An example of using the external clock is illustrated below.



Note : The X1 (X1A, X1B) pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 (X0A, X0B) pin.

# MB91310 Series

- Restrictions

Common in the MB91310 series

(1) Clock Control Block

Take the oscillation stabilization wait time during Low level input to the  $\overline{\text{INIT}}$  pin.

(2) Bit Search Module

The 0-detection data register (BSD0), 1-detection data register (BSD1), and transition-detection data register (BSDC) are only word-accessible.

(3) I/O Port

Ports are accessed only in bytes.

(4) Low Power Consumption Mode

To enter the standby mode, use the synchronous standby mode (set with the SYNC\_S bit as bit 8 in the TBCR, or time-base counter control register) and be sure to use the following sequence:

(LDI #value\_of\_standby, R0)

(LDI #\_STCR, R12)

STB R0, @R12 : Write to standby control register (STCR)

LDUB @R12, R0 : STCR lead for synchronous standby

LDUB @R12, R0 : Dummy re-lead of STCR

NOP : NOP  $\times$  5 for timing adjustment

NOP

NOP

NOP

NOP

In addition, set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.

Please do not do the following when the monitor debugger is used.

- Set a break point within the above array of instructions.
- Single-step the above instructions.

(5) Pre-fetch

When accessing a prefetch-enabled little endian area, be sure to use word access (in 32-bit, word length) only. Byte or half-word access results in wrong data read.

(6) Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

1. The following operations are performed when (c) the instruction followed by a data event or a DIVOU/DIVOS emulator menu instruction (a) receives a user interrupt or NMI or (b) breaks when single-stepped.

- The D0 and D1 flags are updated in advance.
  - An EIT handling routine (user interrupt, NMI, or emulator) is executed.
  - Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1).
2. The following operations are performed when the ORCCR/STILM/MOV Ri and PS instructions are executed.
- The PS register is updated in advance.
  - An EIT handling routine (user interrupt or NMI) is executed.
  - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1).

## (7) Watchdog Timer

The watchdog timer built in this model monitors a program to check that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on watching programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution. Refer to the watchdog timer function description for the exceptional condition.

If the system runs out of control and develops the above condition, a watchdog reset may not be generated. In that case, please reset (INIT) by external  $\overline{\text{INIT}}$  terminal.

## (8) Notes on using the A/D converter

The MB91310 series contains an A/D converter. Supply power to the AV<sub>CC</sub> at 3.3 V.

Unique to the evaluation chip MB91FV310A

### (1) Simultaneous occurrences of a software break and a user interrupt/NMI

If a software break and a user interrupt/NMI occurs simultaneously, the emulator debugger may react as follows.

- The debugger stops pointing to a location other than the programmed break points.
- The halted program is not re - executed correctly.

If this symptom occurs, use a hardware break in place of a hardware break. If you use the monitor debugger, do not set a break point within the relevant array of instructions.

### (2) Single-stepping of the RETI instruction

If an interrupt occurs frequently during single stepping, execute only the relevant processing routine repeatedly after single-stepping RETI. This will prevent the main routine and low-interrupt-level programs from being executed. Do not single-step the RETI instruction for avoidance purposes. When the debugging of the relevant interrupt routine becomes unnecessary, perform debugging with that interrupt disabled.

### (3) About an Operand Break

Do not apply a data event break to access to the area containing the address of a stack pointer.

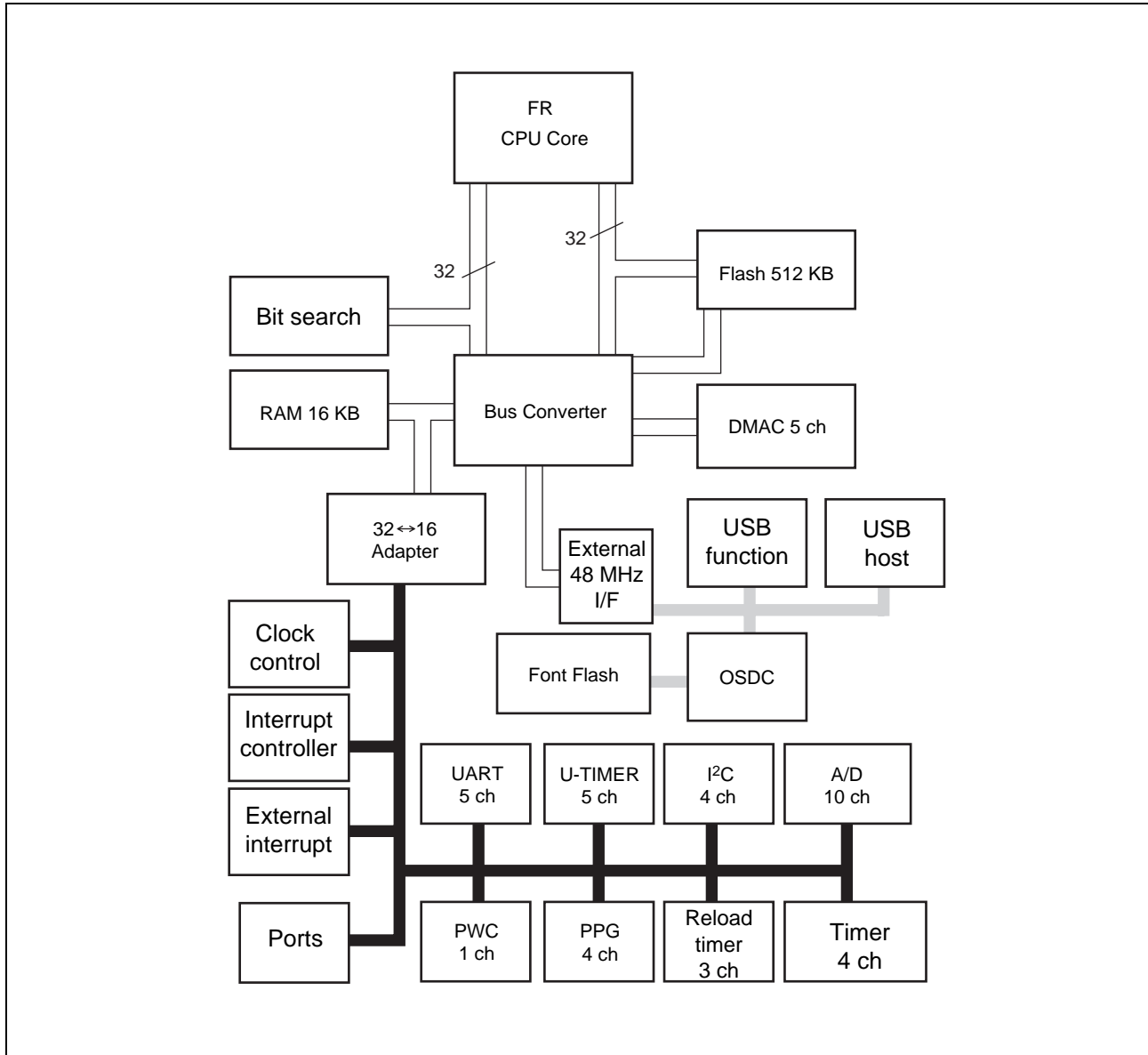
### (4) Sample Batch File for Configuration

To debug a program downloaded to internal RAM, be sure to execute the following batch file after executing RESET.

```
# Set MODR (0x7fd) = Enable In memory + 16-bit External Bus  
set mem/byte 0x7fd = 0x5
```

# MB91310 Series

## ■ BLOCK DIAGRAM



## ■ MEMORY SPACE

### 1. Memory space

The FR family has 4 Gbytes of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

#### Direct Addressing Areas

The following address space areas are used as I/O areas.

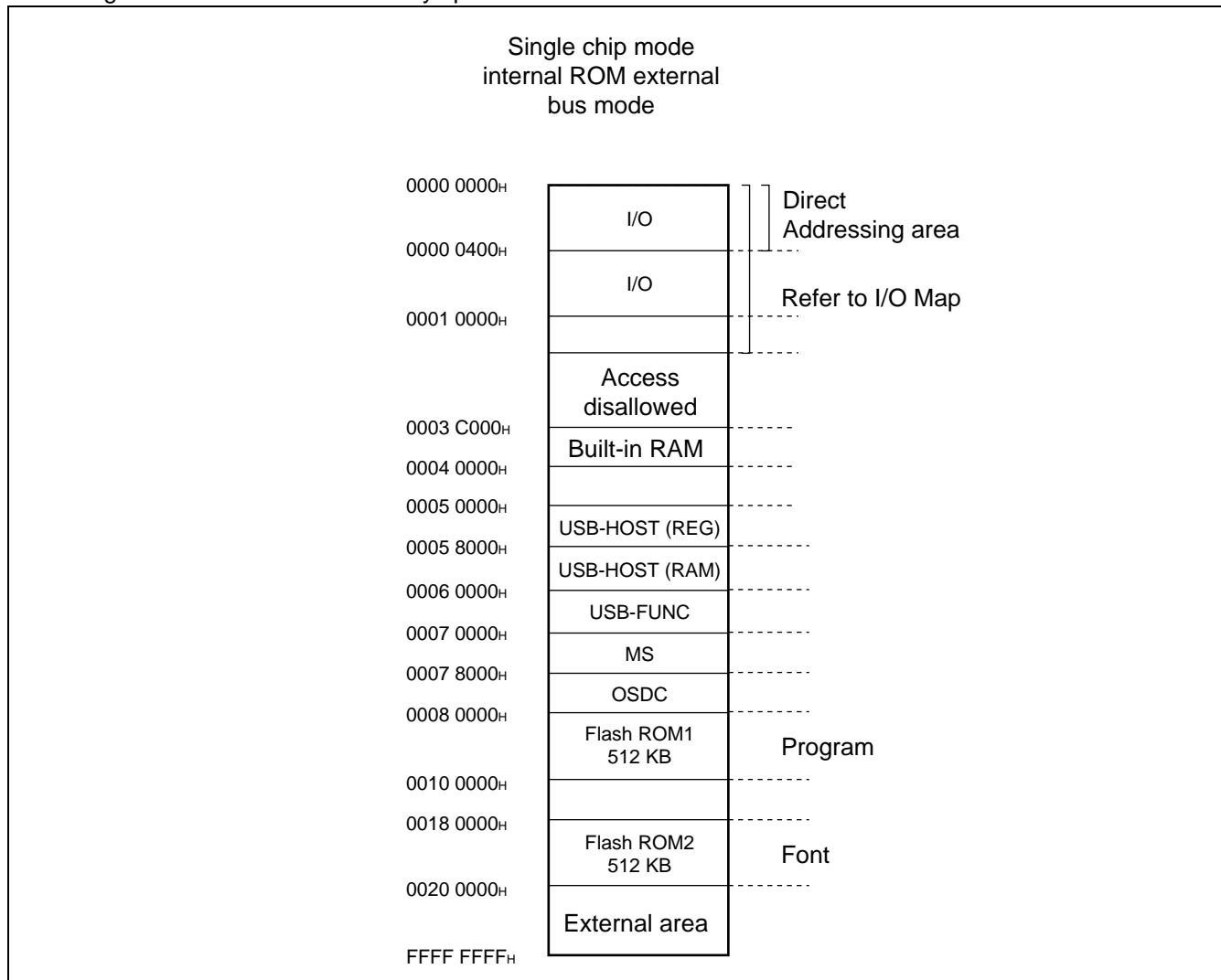
These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The size of directly addressable areas depends on the length of the data being accessed as shown below.

- byte data access : 0-0FF<sub>H</sub>
- half word data access : 0-1FF<sub>H</sub>
- word data access : 0-3FF<sub>H</sub>

### 2. Memory Map

The figure below shows the memory space of the this item kind.



# MB91310 Series

## ■ I/O MAP

This shows the location of the various peripheral resource registers in the memory space.

[How to read the table]

| Address | Register               |                        |                        |                        | Block                           |
|---------|------------------------|------------------------|------------------------|------------------------|---------------------------------|
|         | + 0                    | + 1                    | + 2                    | + 3                    |                                 |
| 000000H | PDR0 [R/W]<br>XXXXXXXX | PDR1 [R/W]<br>XXXXXXXX | PDR2 [R/W]<br>XXXXXXXX | PDR3 [R/W]<br>XXXXXXXX | T-unit<br>Port Data<br>Register |

Read/Write attribute

Initial value after a reset

Register name (First-column register at address 4n; second-column register at address 4n + 2)

Location of left - most register (When using word access, the register in column 1 is in the MSB side of the data.)

Note: Initial values of register bits are represented as follows:

- "1" : Initial Value: "1"
- "0" : Initial Value: "0"
- "X" : Initial Value: "X"
- "-" : No physical register at this location

# MB91310 Series

| Address                  | Register                           |                         |                                   |                        | Block                       |
|--------------------------|------------------------------------|-------------------------|-----------------------------------|------------------------|-----------------------------|
|                          | + 0                                | + 1                     | + 2                               | + 3                    |                             |
| 000000H<br>to<br>00000FH | —                                  | —                       | —                                 | —                      | Reserved                    |
| 000010H                  | PDR0 [R/W]<br>XXXXXXXX             | PDR1 [R/W]<br>XXXXXXXX  | PDR2 [R/W]<br>--XXXXXX            | PDR3 [R/W]<br>-XXXXXXX | R-bus<br>Port Data Register |
| 000014H                  | PDR4 [R/W]<br>XXXXXXXX             | PDR5 [R/W]<br>XXXXXXXX  | PDR6 [R/W]<br>--XXXXXX            | PDR7 [R/W]<br>---XXXXX |                             |
| 000018H                  | —                                  | —                       | —                                 | —                      |                             |
| 00001CH                  | —                                  | —                       | —                                 | —                      |                             |
| 000020H                  | ADCTH [R/W]<br>XXXXXX00            | ADCTL [R/W]<br>00000X00 | ADCH [R/W]<br>00000000_00000000   |                        | 10 bit A/D converter        |
| 000024H                  | ADAT0 [R]<br>XXXXXXXX00_00000000   |                         | ADAT1 [R]<br>XXXXXXXX00_00000000  |                        |                             |
| 000028H                  | ADAT2 [R]<br>XXXXXXXX00_00000000   |                         | ADAT3 [R]<br>XXXXXXXX00_00000000  |                        |                             |
| 00002CH                  | ADAT4 [R]<br>XXXXXXXX00_00000000   |                         | ADAT5 [R]<br>XXXXXXXX00_00000000  |                        |                             |
| 000030H                  | ADAT6 [R]<br>XXXXXXXX00_00000000   |                         | ADAT7 [R]<br>XXXXXXXX00_00000000  |                        |                             |
| 000034H                  | ADAT8 [R]<br>XXXXXXXX00_00000000   |                         | ADAT9 [R]<br>XXXXXXXX00_00000000  |                        |                             |
| 000038H                  | —                                  | —                       | —                                 | —                      | Reserved                    |
| 00003CH                  | —                                  | —                       | —                                 | —                      |                             |
| 000040H                  | EIRR [R/W]<br>00000000             | ENIR [R/W]<br>00000000  | ELVR [R/W]<br>00000000            |                        | Ext int                     |
| 000044H                  | DICR [R/W]<br>-----0               | HRCL [R/W]<br>0--11111  | —                                 |                        | DLYI/I-unit                 |
| 000048H                  | TMRLR0 [W]<br>XXXXXXXXXX XXXXXXXXX |                         | TMR0 [R]<br>XXXXXXXXXX XXXXXXXXX  |                        | Reload Timer 0              |
| 00004CH                  | —                                  |                         | TMCSR0 [R/W]<br>----0000 00000000 |                        |                             |
| 000050H                  | TMRLR1 [W]<br>XXXXXXXXXX XXXXXXXXX |                         | TMR1 [R]<br>XXXXXXXXXX XXXXXXXXX  |                        | Reload Timer 1              |
| 000054H                  | —                                  |                         | TMCSR1 [R/W]<br>----0000 00000000 |                        |                             |
| 000058H                  | TMRLR2 [W]<br>XXXXXXXXXX XXXXXXXXX |                         | TMR2 [R]<br>XXXXXXXXXX XXXXXXXXX  |                        | Reload Timer 2              |
| 00005CH                  | —                                  |                         | TMCSR2 [R/W]<br>----0000 00000000 |                        |                             |

(Continued)

# MB91310 Series

| Address | Register                                  |                        |                                |                         | Block                             |
|---------|---|------------------------|--------------------------------|-------------------------|-----------------------------------|
|         | + 0                                       | + 1                    | + 2                            | + 3                     |                                   |
| 000060H | SSR [R/W]<br>00001-00                     | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100          | SMR [R/W]<br>00--0-0-   | UART0                             |
| 000064H | UTIM [R] (UTIMR [W])<br>00000000 00000000 |                        | DRCL [W]<br>-----              | UTIMC [R/W]<br>0--00001 | U-TIMER 0                         |
| 000068H | SSR [R/W]<br>00001-00                     | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100          | SMR [R/W]<br>00--0-0-   | UART1                             |
| 00006CH | UTIM [R] (UTIMR [W])<br>00000000 00000000 |                        | DRCL [W]<br>-----              | UTIMC [R/W]<br>0--00001 | U-TIMER 1                         |
| 000070H | SSR [R/W]<br>00001-00                     | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100          | SMR [R/W]<br>00--0-0-   | UART2                             |
| 000074H | UTIM [R] (UTIMR [W])<br>00000000 00000000 |                        | DRCL [W]<br>-----              | UTIMC [R/W]<br>0--00001 | U-TIMER 2                         |
| 000078H | SSR [R/W]<br>00001-00                     | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100          | SMR [R/W]<br>00--0-0-   | UART3                             |
| 00007CH | UTIM [R] (UTIMR [W])<br>00000000 00000000 |                        | DRCL [W]<br>-----              | UTIMC [R/W]<br>0--00001 | U-TIMER 3                         |
| 000080H | SSR [R/W]<br>00001-00                     | SIDR [R/W]<br>XXXXXXXX | SCR [R/W]<br>00000100          | SMR [R/W]<br>00--0-0-   | UART4                             |
| 000084H | UTIM [R] (UTIMR [W])<br>00000000 00000000 |                        | DRCL [W]<br>-----              | UTIMC [R/W]<br>0--00001 | U-TIMER 4                         |
| 000088H | —   |                        | —                              |                         | Reserved                          |
| 00008CH | —   |                        | —                              |                         |                                   |
| 000090H | PWCC [R/W]                                | PWCC [R/W]             | —                              |                         | PWC                               |
| 000094H | PWCD [R]<br>XXXXXXXX_XXXXXXXX             |                        | —                              |                         |                                   |
| 000098H | —   |                        | —                              |                         | Reserved                          |
| 00009CH | —   |                        | —                              |                         |                                   |
| 0000A0H | —   |                        | —                              |                         |                                   |
| 0000A4H | —   |                        | —                              |                         |                                   |
| 0000A8H | —   |                        | —                              |                         |                                   |
| 0000ACH | —   |                        | —                              |                         |                                   |
| 0000B0H | —   | —                      | —                              | —                       | I <sup>2</sup> C interface<br>ch0 |
| 0000B4H | IBCR [R/W]<br>00000000                    | IBSR [R/W]<br>00000000 | ITBA [R/W]<br>-----00 00000000 |                         |                                   |
| 0000B8H | ITMK [R/W]<br>00----11 11111111           |                        | ISMK [R/W]<br>01111111         | ISBA [R/W]<br>00000000  |                                   |
| 0000BCH | —   | IDAR [R/W]<br>00000000 | ICCR [R/W]<br>0-011111         | IDBL [R/W]<br>-----0    |                                   |
| 0000C0H | —   | —                      | —                              | —                       | Reserved                          |

(Continued)



# MB91310 Series

| Address | Register                         |                         |                                  |                         | Block                             |
|---------|----------------------------------|-------------------------|----------------------------------|-------------------------|-----------------------------------|
|         | + 0                              | + 1                     | + 2                              | + 3                     |                                   |
| 0000C4H | IBCR [R/W]<br>00000000           | IBSR [R/W]<br>00000000  | ITBA [R/W]<br>-----00 00000000   |                         | I <sup>2</sup> C interface<br>ch1 |
| 0000C8H | ITMK [R/W]<br>00----11 11111111  |                         | ISMK [R/W]<br>01111111           | ISBA [R/W]<br>00000000  |                                   |
| 0000CCH | —                                | IDAR [R/W]<br>00000000  | ICCR [R/W]<br>0-011111           | IDBL [R/W]<br>-----0    |                                   |
| 0000D0H | —                                | —                       | —                                | —                       | Reserved                          |
| 0000D4H | IBCR [R/W]<br>00000000           | IBSR [R/W]<br>00000000  | ITBA [R/W]<br>-----00 00000000   |                         | I <sup>2</sup> C interface<br>ch2 |
| 0000D8H | ITMK [R/W]<br>00----11 11111111  |                         | ISMK [R/W]<br>01111111           | ISBA [R/W]<br>00000000  |                                   |
| 0000DCH | —                                | IDAR [R/W]<br>00000000  | ICCR [R/W]<br>0-011111           | IDBL [R/W]<br>-----0    |                                   |
| 0000E0H | —                                | —                       | —                                | —                       | Reserved                          |
| 0000E4H | IBCR [R/W]<br>00000000           | IBSR [R/W]<br>00000000  | ITBA [R/W]<br>-----00 00000000   |                         | I <sup>2</sup> C interface<br>ch3 |
| 0000E8H | ITMK [R/W]<br>00----11 11111111  |                         | ISMK [R/W]<br>01111111           | ISBA [R/W]<br>00000000  |                                   |
| 0000ECH | —                                | IDAR [R/W]<br>00000000  | ICCR [R/W]<br>0-011111           | IDBL [R/W]<br>-----0    |                                   |
| 0000F0H | T0LPCR [R/W]<br>-----000         | T0CCR [R/W]<br>0-010000 | T0TCR [R/W]<br>00000000          | T0R [R/W]<br>---00000   | Multi-function<br>timer           |
| 0000F4H | T0DRR [R/W]<br>XXXXXXXX XXXXXXXX |                         | T0CRR [R/W]<br>XXXXXXXX XXXXXXXX |                         |                                   |
| 0000F8H | T1LPCR [R/W]<br>-----000         | T1CCR [R/W]<br>0-000000 | T1TCR [R/W]<br>00000000          | T1R [R/W]<br>---00000   |                                   |
| 0000FCH | T1DRR [R/W]<br>XXXXXXXX XXXXXXXX |                         | T1CRR [R/W]<br>XXXXXXXX XXXXXXXX |                         |                                   |
| 000100H | T2LPCR [R/W]<br>-----000         | T2CCR [R/W]<br>0-000000 | T2TCR [R/W]<br>00000000          | T2R [R/W]<br>---00000   |                                   |
| 000104H | T2DRR [R/W]<br>XXXXXXXX XXXXXXXX |                         | T2CRR [R/W]<br>XXXXXXXX XXXXXXXX |                         |                                   |
| 000108H | T3LPCR [R/W]<br>-----000         | T3CCR [R/W]<br>0-000000 | T3TCR [R/W]<br>00000000          | T3R [R/W]<br>---00000   |                                   |
| 00010CH | T3DRR [R/W]<br>XXXXXXXX XXXXXXXX |                         | T3CRR [R/W]<br>XXXXXXXX XXXXXXXX |                         |                                   |
| 000110H | —                                | —                       | —                                | —                       |                                   |
| 000120H | PTMR0 [R]<br>11111111_11111111   |                         | PCSR0 [W]<br>XXXXXXXX_XXXXXXX    |                         | PPG0                              |
| 000124H | PDUT0 [W]<br>XXXXXXXX_XXXXXXX    |                         | PCNH0 [R/W]<br>00000000          | PCNL0 [R/W]<br>00000000 |                                   |

(Continued)

# MB91310 Series

| Address  | Register  |     |                                |                         | Block    |
|--|---|-----|--------------------------------|-------------------------|----------|
|  | + 0   | + 1 | + 2                            | + 3                     |          |
| 000128 <sub>H</sub>                              | PTMR1 [R]<br>11111111_11111111                      |     | PCSR1 [W]<br>XXXXXXXX_XXXXXXXX |                         | PPG1     |
| 00012C <sub>H</sub>                              | PDUT1 [W]<br>XXXXXXXX_XXXXXXXX                      |     | PCNH1 [R/W]<br>00000000        | PCNL1 [R/W]<br>00000000 |          |
| 000130 <sub>H</sub>                              | PTMR2 [R]<br>11111111_11111111                      |     | PCSR2 [W]<br>XXXXXXXX_XXXXXXXX |                         | PPG2     |
| 000134 <sub>H</sub>                              | PDUT2 [W]<br>XXXXXXXX_XXXXXXXX                      |     | PCNH2 [R/W]<br>00000000        | PCNL2 [R/W]<br>00000000 |          |
| 000138 <sub>H</sub>                              | PTMR3 [R]<br>11111111_11111111                      |     | PCSR3 [W]<br>XXXXXXXX_XXXXXXXX |                         | PPG3     |
| 00013C <sub>H</sub>                              | PDUT3 [W]<br>XXXXXXXX_XXXXXXXX                      |     | PCNH3 [R/W]<br>00000000        | PCNL3 [R/W]<br>00000000 |          |
| 000140 <sub>H</sub>                              | —   | —   | —                              | —                       | Reserved |
| 000144 <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 000148 <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 00014C <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 000150 <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 000154 <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 000158 <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 00015C <sub>H</sub>                              | —   | —   | —                              | —                       |          |
| 000160 <sub>H</sub><br>to<br>0001FC <sub>H</sub> | —   | —   | —                              | —                       |          |
| 000200 <sub>H</sub>                              | DMACA0 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX |     |                                |                         |          |
| 000204 <sub>H</sub>                              | DMACB4 [R/W]<br>00000000 00000000 00000000 00000000 |     |                                |                         |          |
| 000208 <sub>H</sub>                              | DMACA1 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX |     |                                |                         |          |
| 00020C <sub>H</sub>                              | DMACB4 [R/W]<br>00000000 00000000 00000000 00000000 |     |                                |                         |          |
| 000210 <sub>H</sub>                              | DMACA2 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX |     |                                |                         |          |
| 000214 <sub>H</sub>                              | DMACB4 [R/W]<br>00000000 00000000 00000000 00000000 |     |                                |                         |          |
| 000218 <sub>H</sub>                              | DMACA3 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX |     |                                |                         |          |
| 00021C <sub>H</sub>                              | DMACB4 [R/W]<br>00000000 00000000 00000000 00000000 |     |                                |                         |          |

(Continued)

# MB91310 Series

| Address                  | Register  |                        |                        |                        | Block                               |
|--------------------------|---|------------------------|------------------------|------------------------|-------------------------------------|
|                          | + 0   | + 1                    | + 2                    | + 3                    |                                     |
| 000220H                  | DMACA4 [R/W]<br>00000000 0000XXXX XXXXXXXX XXXXXXXX |                        |                        |                        | DMAC                                |
| 000224H                  | DMACB4 [R/W]<br>00000000 00000000 00000000 00000000 |                        |                        |                        |                                     |
| 000228H                  | —   |                        |                        |                        |                                     |
| 00022CH<br>to<br>00023CH | —   |                        |                        |                        | Reserved                            |
| 000240H                  | DMACR [R/W]<br>0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX  |                        |                        |                        | DMAC                                |
| 000244H<br>to<br>0002FCH | —   |                        |                        |                        | —                                   |
| 000300H<br>to<br>0003ECH | —   |                        |                        |                        |                                     |
| 0003F0H                  | BSD0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX     |                        |                        |                        |                                     |
| 0003F4H                  | BSD1 [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX   |                        |                        |                        |                                     |
| 0003F8H                  | BSDC [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX     |                        |                        |                        |                                     |
| 0003FCH                  | BSRR [R]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX     |                        |                        |                        |                                     |
| 000400H                  | DDR0 [R/W]<br>00000000                              | DDR1 [R/W]<br>00000000 | DDR2 [R/W]<br>--000000 | DDR3 [R/W]<br>-0000000 | R-bus<br>Port Direction<br>Register |
| 000404H                  | DDR4 [R/W]<br>00000000                              | DDR5 [R/W]<br>00000000 | DDR6 [R/W]<br>--000000 | DDR7 [R/W]<br>---00000 |                                     |
| 000408H                  | —   | —                      | —                      | —                      |                                     |
| 00040CH                  | —   | —                      | —                      | —                      |                                     |
| 000410H                  | PFR0 [R/W]<br>0--00000                              | PFR1 [R/W]<br>00000000 | PFR2 [R/W]<br>000---00 | PFR3 [R/W]<br>00000000 | R-bus<br>Port Function<br>Register  |
| 000414H                  | PFR4 [R/W]<br>0-----                                | —                      | —                      | —                      |                                     |
| 000418H                  | —   | —                      | —                      | —                      |                                     |
| 00041CH                  | —   | —                      | —                      | —                      |                                     |
| 000420H<br>to<br>00043CH | —   |                        |                        |                        | Reserved                            |

(Continued)

# MB91310 Series

| Address  | Register                             |                                      |                                       |                                       | Block                                |
|--|--------------------------------------|--------------------------------------|---------------------------------------|---------------------------------------|--------------------------------------|
|  | + 0                                  | + 1                                  | + 2                                   | + 3                                   |                                      |
| 000440 <sub>H</sub>                              | ICR00 [R/W]<br>---11111              | ICR01 [R/W]<br>---11111              | ICR02 [R/W]<br>---11111               | ICR03 [R/W]<br>---11111               | Interrupt Control unit               |
| 000444 <sub>H</sub>                              | ICR04 [R/W]<br>---11111              | ICR05 [R/W]<br>---11111              | ICR06 [R/W]<br>---11111               | ICR07 [R/W]<br>---11111               |                                      |
| 000448 <sub>H</sub>                              | ICR08 [R/W]<br>---11111              | ICR09 [R/W]<br>---11111              | ICR10 [R/W]<br>---11111               | ICR11 [R/W]<br>---11111               |                                      |
| 00044C <sub>H</sub>                              | ICR12 [R/W]<br>---11111              | ICR13 [R/W]<br>---11111              | ICR14 [R/W]<br>---11111               | ICR15 [R/W]<br>---11111               |                                      |
| 000450 <sub>H</sub>                              | ICR16 [R/W]<br>---11111              | ICR17 [R/W]<br>---11111              | ICR18 [R/W]<br>---11111               | ICR19 [R/W]<br>---11111               |                                      |
| 000454 <sub>H</sub>                              | ICR20 [R/W]<br>---11111              | ICR21 [R/W]<br>---11111              | ICR22 [R/W]<br>---11111               | ICR23 [R/W]<br>---11111               |                                      |
| 000458 <sub>H</sub>                              | ICR24 [R/W]<br>---11111              | ICR25 [R/W]<br>---11111              | ICR26 [R/W]<br>---11111               | ICR27 [R/W]<br>---11111               |                                      |
| 00045C <sub>H</sub>                              | ICR28 [R/W]<br>---11111              | ICR29 [R/W]<br>---11111              | ICR30 [R/W]<br>---11111               | ICR31 [R/W]<br>---11111               | Interrupt Control unit               |
| 000460 <sub>H</sub>                              | ICR32 [R/W]<br>---11111              | ICR33 [R/W]<br>---11111              | ICR34 [R/W]<br>---11111               | ICR35 [R/W]<br>---11111               |                                      |
| 000464 <sub>H</sub>                              | ICR36 [R/W]<br>---11111              | ICR37 [R/W]<br>---11111              | ICR38 [R/W]<br>---11111               | ICR39 [R/W]<br>---11111               |                                      |
| 000468 <sub>H</sub>                              | ICR40 [R/W]<br>---11111              | ICR41 [R/W]<br>---11111              | ICR42 [R/W]<br>---11111               | ICR43 [R/W]<br>---11111               |                                      |
| 00046C <sub>H</sub>                              | ICR44 [R/W]<br>---11111              | ICR45 [R/W]<br>---11111              | ICR46 [R/W]<br>---11111               | ICR47 [R/W]<br>---11111               |                                      |
| 000470 <sub>H</sub><br>to<br>00047C <sub>H</sub> | —                                    |                                      |                                       |                                       | —                                    |
| 000480 <sub>H</sub>                              | RSRR [R/W]<br>10000000* <sup>2</sup> | STCR [R/W]<br>00110011* <sup>2</sup> | TBCR [R/W]<br>00XXXX00* <sup>1</sup>  | CTBR [W]<br>XXXXXXXX                  | Clock Control unit                   |
| 000484 <sub>H</sub>                              | CLKR [R/W]<br>00000000* <sup>1</sup> | WPR [W]<br>XXXXXXXX                  | DIVR0 [R/W]<br>00000011* <sup>1</sup> | DIVR1 [R/W]<br>00000000* <sup>1</sup> |                                      |
| 000488 <sub>H</sub>                              | —                                    | —                                    | OSCCR [R/W]<br>XXXXXXXX0              | —                                     | —                                    |
| 00048C <sub>H</sub>                              | WPCR [R/W] B<br>00---000             | —                                    | —                                     | —                                     | Clock timer                          |
| 000490 <sub>H</sub>                              | OSCR [R/W] B<br>00---000             | —                                    | —                                     | —                                     | Oscillation<br>Stabilization Waiting |

(Continued)

# MB91310 Series

| Address  | Register                          |     |                                   |     | Block                                |
|--|-----------------------------------|-----|-----------------------------------|-----|--------------------------------------|
|  | + 0                               | + 1 | + 2                               | + 3 |                                      |
| 000494 <sub>H</sub><br>to<br>0005FC <sub>H</sub> | —                                 |     |                                   |     | Reserved                             |
| 000600 <sub>H</sub>                              | —                                 | —   | —                                 | —   | T-unit<br>Port Direction<br>Register |
| 000604 <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 000608 <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 00060C <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 000610 <sub>H</sub>                              | —                                 | —   | —                                 | —   | T-unit<br>Port Function<br>Register  |
| 000614 <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 000618 <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 00061C <sub>H</sub>                              | —                                 | —   | —                                 | —   |                                      |
| 000620 <sub>H</sub>                              | —                                 |     |                                   |     |                                      |
| 000624 <sub>H</sub>                              | —                                 |     |                                   |     |                                      |
| 000628 <sub>H</sub><br>to<br>00063F <sub>H</sub> | —                                 |     |                                   |     | Reserved                             |
| 000640 <sub>H</sub>                              | ASR0 [R/W]<br>00000000 00000000*1 |     | ACR0 [R/W]<br>1111XX00 00000000*1 |     | T-unit                               |
| 000644 <sub>H</sub>                              | ASR1 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR1 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000648 <sub>H</sub>                              | ASR2 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR2 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 00064C <sub>H</sub>                              | ASR3 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR3 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000650 <sub>H</sub>                              | ASR4 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR4 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000654 <sub>H</sub>                              | ASR5 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR5 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000658 <sub>H</sub>                              | ASR6 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR6 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 00065C <sub>H</sub>                              | ASR7 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | ACR7 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000660 <sub>H</sub>                              | AWR0 [R/W]<br>01111111 11111111*1 |     | AWR1 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000664 <sub>H</sub>                              | AWR2 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | AWR3 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |
| 000668 <sub>H</sub>                              | AWR4 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     | AWR5 [R/W]<br>XXXXXXXX XXXXXXXX*1 |     |                                      |

(Continued)

# MB91310 Series

| Address                   | Register  |                         |                                   |                         | Block    |
|---------------------------|---|-------------------------|-----------------------------------|-------------------------|----------|
|                           | + 0   | + 1                     | + 2                               | + 3                     |          |
| 00066CH                   | AWR6 [R/W]<br>XXXXXXXX XXXXXXXX*1               |                         | AWR7 [R/W]<br>XXXXXXXX XXXXXXXX*1 |                         | T-unit   |
| 000670H                   | —   |                         |                                   |                         |          |
| 000674H                   | —   |                         |                                   |                         |          |
| 000678H                   | IOWR0 [R/W]<br>XXXXXXXX                         | IOWR1 [R/W]<br>XXXXXXXX | IOWR2 [R/W]<br>XXXXXXXX           | —                       |          |
| 00067CH                   | —   |                         |                                   |                         |          |
| 000680H                   | CSER [R/W]<br>00000001                          | CHER [R/W]<br>11111111  | —                                 | TCR [R/W]<br>00000000   |          |
| 000684H                   | —   |                         |                                   |                         |          |
| 000684H<br>to<br>0007F8 H | —   |                         |                                   |                         | Reserved |
| 0007FCH                   | —   | MODR [W]<br>XXXXXXXX    | —                                 | —                       | —        |
| 000800H<br>to<br>000AFC H | —   |                         |                                   |                         | Reserved |
| 000B00H                   | ESTS0 [R/W]<br>X0000000                         | ESTS1 [R/W]<br>XXXXXXXX | ESTS2 [R]<br>1XXXXXXXX            | —                       | DSU      |
| 000B04H                   | ECTL0 [R/W]<br>0X000000                         | ECTL1 [R/W]<br>00000000 | ECTL2 [W]<br>000X0000             | ECTL3 [R/W]<br>00X00X11 |          |
| 000B08H                   | ECNT0 [W]<br>XXXXXXXX                           | ECNT1 [W]<br>XXXXXXXX   | EUSA [W]<br>XXX00000              | EDTC [W]<br>0000XXXX    |          |
| 000B0CH                   | EWPT [R]<br>00000000 00000000                   |                         | —                                 |                         |          |
| 000B10H                   | EDTR0 [W]<br>XXXXXXXX XXXXXXXX                  |                         | EDTR1 [W]<br>XXXXXXXX XXXXXXXX    |                         |          |
| 000B14H<br>to<br>000B1CH  | —   |                         |                                   |                         |          |
| 000B20H                   | EIA0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |                         |                                   |                         |          |
| 000B24H                   | EIA1 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |                         |                                   |                         |          |
| 000B28H                   | EIA2 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |                         |                                   |                         |          |
| 000B2CH                   | EIA3 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |                         |                                   |                         |          |
| 000B30H                   | EIA4 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |                         |                                   |                         |          |

(Continued)

# MB91310 Series

| Address  | Register   |     |     |     | Block |
|--|--|-----|-----|-----|-------|
|  | + 0  | + 1 | + 2 | + 3 |       |
| 000B34 <sub>H</sub>                              | EIA5 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     | DSU   |
| 000B38 <sub>H</sub>                              | EIA6 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B3C <sub>H</sub>                              | EIA7 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B40 <sub>H</sub>                              | EDTA [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX      |     |     |     |       |
| 000B44 <sub>H</sub>                              | EDTM [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX      |     |     |     |       |
| 000B48 <sub>H</sub>                              | EOA0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B4C <sub>H</sub>                              | EOA1 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B50 <sub>H</sub>                              | EPCR [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX      |     |     |     |       |
| 000B54 <sub>H</sub>                              | EPSR [R/W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX      |     |     |     |       |
| 000B58 <sub>H</sub>                              | EIAM0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX       |     |     |     |       |
| 000B5C <sub>H</sub>                              | EIAM1 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX       |     |     |     |       |
| 000B60 <sub>H</sub>                              | EOAM0/EODM0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |     |     |     |       |
| 000B64 <sub>H</sub>                              | EOAM1/EODM1 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |     |     |     |       |
| 000B68 <sub>H</sub>                              | EOD0 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B6C <sub>H</sub>                              | EOD1 [W]<br>XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX        |     |     |     |       |
| 000B70 <sub>H</sub><br>to<br>000FFC <sub>H</sub> | —  |     |     |     |       |
| 001000 <sub>H</sub>                              | DMASA0 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX    |     |     |     | DMAC  |
| 001004 <sub>H</sub>                              | DMADA0 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX    |     |     |     |       |
| 001008 <sub>H</sub>                              | DMASA1 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX    |     |     |     |       |
| 00100C <sub>H</sub>                              | DMADA1 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX    |     |     |     |       |

(Continued)

# MB91310 Series

| Address                  | Register  |     |     |     | Block             |
|--------------------------|---|-----|-----|-----|-------------------|
|                          | + 0   | + 1 | + 2 | + 3 |                   |
| 001010H                  | DMASA2 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     | DMAC              |
| 001014H                  | DMADA2 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     |                   |
| 001018H                  | DMASA3 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     |                   |
| 00101CH                  | DMADA3 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     |                   |
| 001020H                  | DMASA4 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     |                   |
| 001024H                  | DMADA4 [R/W]<br>XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX                     |     |     |     |                   |
| 001028H<br>to<br>006FFCH | —   |     |     |     | Reserved          |
| 007000H                  | FLCR [R/W]<br>0110_X000   | —   |     |     | Program FLASH I/F |
| 007004H                  | FLWC [R/W]<br>0001_0011   | —   |     |     |                   |
| 007008H<br>to<br>00707CH | —   |     |     |     | Reserved          |
| 007080H<br>to<br>0070FCH | —   |     |     |     | Reserved          |
| 007100H                  | FNCR [R/W]<br>0110_X000   | —   |     |     | FONT FLASH I/F    |
| 007104H                  | FNWC [R/W]<br>0001_0011   | —   |     |     |                   |
| 00050000H                | HR (Hc Revision) [R]<br>00000000_00000000_00000001_00010000             |     |     |     | USB<br>Host       |
| 00050004H                | HC (Hc Control) [R/W]<br>00000000_00000000_00000000_00000000            |     |     |     |                   |
| 00050008H                | HCS (Hc Command Status) [R/W]<br>00000000_00000000_00000000_00000000    |     |     |     |                   |
| 0005000CH                | HIS (Hc Interrupt Status) [R/W]<br>00000000_00000000_00000000_00000000  |     |     |     |                   |
| 00050010H                | HIE (Hc Interrupt Enable) [R/W]<br>00000000_00000000_00000000_00000000  |     |     |     |                   |
| 00050014H                | HID (Hc Interrupt Disable) [R/W]<br>00000000_00000000_00000000_00000000 |     |     |     |                   |

(Continued)



# MB91310 Series

| Address  | Register   |     |     |     | Block       |
|--|--|-----|-----|-----|-------------|
|  | + 0  | + 1 | + 2 | + 3 |             |
| 00050018 <sub>H</sub>                                | HHCCA (Hc HCCA) [R/W]<br>00000000_00000000_00000000_00000000               |     |     |     | USB<br>Host |
| 0005000C <sub>H</sub>                                | HPCED (Hc Period Current ED) [R/W]<br>00000000_00000000_00000000_00000000  |     |     |     |             |
| 00050020 <sub>H</sub>                                | HCHED (Hc Control Head ED) [R/W]<br>00000000_00000000_00000000_00000000    |     |     |     |             |
| 00050024 <sub>H</sub>                                | HCCED (Hc Control Current ED) [R/W]<br>00000000_00000000_00000000_00000000 |     |     |     |             |
| 00050028 <sub>H</sub>                                | HBHED (Hc Bulk Head ED) [R/W]<br>00000000_00000000_00000000_00000000       |     |     |     |             |
| 0005002C <sub>H</sub>                                | HBCED (Hc Bulk Current ED) [R/W]<br>00000000_00000000_00000000_00000000    |     |     |     |             |
| 00050030 <sub>H</sub>                                | HDH (Hc Done Head) [R/W]<br>00000000_00000000_00000000_00000000            |     |     |     |             |
| 00050034 <sub>H</sub>                                | HFI (Hc Fm Interval) [R/W]<br>00000000_00000000_00101110_11011111          |     |     |     |             |
| 00050038 <sub>H</sub>                                | HFR (Hc Fm Remaining) [R]<br>00000000_00000000_00000000_00000000           |     |     |     |             |
| 0005003C <sub>H</sub>                                | HFN (Hc Fm Number) [R]<br>00000000_00000000_00000000_00000000              |     |     |     |             |
| 00050040 <sub>H</sub>                                | HPS (Hc Periodic Start) [R/W]<br>00000000_00000000_00000000_00000000       |     |     |     |             |
| 00050044 <sub>H</sub>                                | HLST (Hc LS Threshold) [R/W]<br>00000000_00000000_00000110_00101000        |     |     |     |             |
| 00050048 <sub>H</sub>                                | HRDA (Hc Rh Descriptor A) [R/W]<br>00000001_00000000_00000000_00000010     |     |     |     |             |
| 0005004C <sub>H</sub>                                | HRDB (Hc Rh Descriptor B) [R/W]<br>00000000_00000000_00000000_00000000     |     |     |     |             |
| 00050050 <sub>H</sub>                                | HRS (Hc Rh Status) [R/W]<br>00000000_00000000_00000000_000000X0            |     |     |     |             |
| 00050054 <sub>H</sub>                                | HRPS1 (Hc Rh Port Status[1]) [R/W]<br>00000000_00000000_00000000_00000X00  |     |     |     |             |
| 00050058 <sub>H</sub>                                | HRPS2 (Hc Rh Port Status[2]) [R/W]<br>00000000_00000000_00000000_00000X00  |     |     |     |             |
| 0005005C <sub>H</sub><br>to<br>00057FFF <sub>H</sub> | —  |     |     |     |             |
| 00058000 <sub>H</sub><br>to<br>00059FFF <sub>H</sub> | SRAM 8 KB  |     |     |     |             |
| 0005A000 <sub>H</sub><br>to<br>0005FFFF <sub>H</sub> | —  |     |     |     |             |

(Continued)

# MB91310 Series

| Address  | Register                          |     |                                   |     | Block           |
|--|-----------------------------------|-----|-----------------------------------|-----|-----------------|
|  | + 0                               | + 1 | + 2                               | + 3 |                 |
| 00060000 <sub>H</sub>                                | FIFO0o [R]<br>XXXXXXXX_XXXXXXXX   |     | FIFO0i [W]<br>XXXXXXXX_XXXXXXXX   |     | USB<br>Function |
| 00060004 <sub>H</sub>                                | FIFO1 [R]<br>XXXXXXXX_XXXXXXXX    |     | FIFO2 [W]<br>XXXXXXXX_XXXXXXXX    |     |                 |
| 00060008 <sub>H</sub>                                | FIFO3 [R]<br>XXXXXXXX_XXXXXXXX    |     | —                                 |     |                 |
| 0006000C <sub>H</sub><br>to<br>0006001F <sub>H</sub> | —                                 |     |                                   |     |                 |
| 00060020 <sub>H</sub>                                | —                                 |     | CONT1 [R/W]<br>XXXXX0XX_XXX00000  |     |                 |
| 00060024 <sub>H</sub>                                | CONT2 [R/W]<br>XXXXXXXX_XXX00000  |     | CONT3 [R/W]<br>XXXXXXXX_XXX00000  |     |                 |
| 00060028 <sub>H</sub>                                | CONT4 [R/W]<br>XXXXXXXX_XXX00000  |     | CONT5 [R/W]<br>XXXXXXXX_XXX00XX   |     |                 |
| 0006002C <sub>H</sub>                                | CONT6 [R/W]<br>XXXXXXXX_XXXX00XX  |     | CONT7 [R/W]<br>XXXXXXXX_XXX00000  |     |                 |
| 00060030 <sub>H</sub>                                | CONT8 [R/W]<br>XXXXXXXX_XXX00000  |     | CONT9 [R/W]<br>XXXX0000_X000000X  |     |                 |
| 00060034 <sub>H</sub>                                | CONT10 [R/W]<br>XXXXXXXX_0XXX0000 |     | TTSIZE [R/W]<br>00010001_00010001 |     |                 |
| 00060038 <sub>H</sub>                                | TRSIZE [R/W]<br>00010001_00010001 |     | —                                 |     |                 |
| 0006003C <sub>H</sub>                                | —                                 |     |                                   |     |                 |
| 00060040 <sub>H</sub>                                | RSIZE0 [R]<br>XXXXXXXX_XXXX0000   |     | —                                 |     |                 |
| 00060044 <sub>H</sub>                                | RSIZE1 [R]<br>XXXXXXXX_X0000000   |     | —                                 |     |                 |
| 00060048 <sub>H</sub><br>to<br>0006005F <sub>H</sub> | —                                 |     |                                   |     |                 |
| 00060060 <sub>H</sub>                                | —                                 |     | ST1 [R/W]<br>XXXXXX00_00000000    |     |                 |
| 00060064 <sub>H</sub>                                | —                                 |     |                                   |     |                 |
| 00060068 <sub>H</sub>                                | ST2 [R]<br>XXXXXXXX_XXX00000      |     | ST3 [R/W]<br>XXXXXXXX_XXX00000    |     |                 |
| 0006006C <sub>H</sub>                                | ST4 [R/W]<br>XXXXX000_00000000    |     | ST5 [R/W]<br>XXXX0XXX_XX00000000  |     |                 |

(Continued)

# MB91310 Series

| Address                      | Register                              |                                       |     |      | Block           |
|------------------------------|---------------------------------------|---------------------------------------|-----|------|-----------------|
|                              | + 0                                   | + 1                                   | + 2 | + 3  |                 |
| 00060070H<br>to<br>0006007DH | —                                     |                                       |     |      | USB<br>Function |
| 0006007EH                    | RESET [R/W]<br>00000---_-----         | —                                     |     |      |                 |
| 00060080H<br>to<br>00077FFFH | —                                     |                                       |     |      | Reserved        |
| 00078000H                    | OSD_VADR [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_CD1 [R/W]<br>XXXXXXXX_XXXXXXXX    |     | OSDC |                 |
| 00078004H                    | OSD_CD2 [R/W]<br>XXXXXXXX_XXXXXXXX    | OSD_RCD1 [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078008H                    | OSD_RCD2 [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_SOC1 [R/W]<br>XXXXXXXX_0000XXXX   |     |      |                 |
| 0007800CH                    | OSD_SOC2 [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_VDPC [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078010H                    | OSD_HDPC [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_CVSC [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078014H                    | OSD_SBFCC [R/W]<br>XXXXXXXX_XXXXXXXX  | OSD_THCC [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078018H                    | OSD_GFCC [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_SBCC1 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |      |                 |
| 0007801CH                    | OSD_SBCC2 [R/W]<br>XXXXXXXX_XXXXXXXX  | OSD_SPCC1 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |      |                 |
| 00078020H                    | OSD_SPCC2 [R/W]<br>XXXXXXXX_XXXXXXXX  | OSD_SPCC3 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |      |                 |
| 00078024H                    | OSD_SPCC4 [R/W]<br>XXXXXXXX_XXXXXXXX  | OSD_SYNC [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078028H                    | OSD_DCLKC1 [R/W]<br>XXXXXXXX_XXXXXXXX | OSD_DCLKC2 [R/W]<br>XXXXXXXX_XXXXXXXX |     |      |                 |
| 0007802CH                    | OSD_DCLKC3 [R/W]<br>XXXXXXXX_XXXXXXXX | OSD_IOC1 [R/W]<br>XXXXXXXX_XXXXXX00   |     |      |                 |
| 00078030H                    | OSD_IOC2 [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_DPC1 [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078034H                    | OSD_DPC2 [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_DPC3 [R/W]<br>XXXXXXXX_XXXXXXXX   |     |      |                 |
| 00078038H                    | OSD_DPC4 [R/W]<br>XXXXXXXX_XXXXXXXX   | OSD_IRC [R/W]<br>XXXXXXXX_XXXXXXXX    |     |      |                 |

(Continued)

# MB91310 Series

(Continued)

| Address  | Register                             |     |                                      |     | Block    |
|--|--------------------------------------|-----|--------------------------------------|-----|----------|
|  | + 0                                  | + 1 | + 2                                  | + 3 |          |
| 0007803C <sub>H</sub>                                | OSD_PLT0 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_PLT1 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSDC     |
| 00078040 <sub>H</sub>                                | OSD_PLT2 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_PLT3 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |          |
| 00078044 <sub>H</sub>                                | OSD_PLT4 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_PLT5 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |          |
| 00078048 <sub>H</sub>                                | OSD_PLT6 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_PLT7 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |          |
| 0007804C <sub>H</sub>                                | OSD_PLT8 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_PLT9 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |          |
| 00078050 <sub>H</sub>                                | OSD_PLT10 [R/W]<br>XXXXXXXX_XXXXXXXX |     | OSD_PLT11 [R/W]<br>XXXXXXXX_XXXXXXXX |     |          |
| 00078054 <sub>H</sub>                                | OSD_PLT12 [R/W]<br>XXXXXXXX_XXXXXXXX |     | OSD_PLT13 [R/W]<br>XXXXXXXX_XXXXXXXX |     |          |
| 00078058 <sub>H</sub>                                | OSD_PLT14 [R/W]<br>XXXXXXXX_XXXXXXXX |     | OSD_PLT15 [R/W]<br>XXXXXXXX_XXXXXXXX |     |          |
| 0007805C <sub>H</sub>                                | OSD_ACT1 [R/W]<br>XXXXXXXX_XXXXXXXX  |     | OSD_ACT2 [R/W]<br>XXXXXXXX_XXXXXXXX  |     |          |
| 00078060 <sub>H</sub><br>to<br>0007FFFF <sub>H</sub> | —                                    |     |                                      |     | Reserved |

\*1 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset.

\*2 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset by the  $\overline{\text{INIT}}$  pin.

## ■ INTERRUPT SOURCE, INTERRUPT VECTOR AND INTERRUPT REGISTER ASSIGNMENT

| Interrupt source                    | Interrupt number |    | Interrupt level            | Offset           | Address of TBR default | RN |
|-------------------------------------|------------------|----|----------------------------|------------------|------------------------|----|
|                                     | 10               | 16 |                            |                  |                        |    |
| Reset                               | 0                | 00 | —                          | 3FC <sub>H</sub> | 000FFFFC <sub>H</sub>  | —  |
| Mode vector                         | 1                | 01 | —                          | 3F8 <sub>H</sub> | 000FFFF8 <sub>H</sub>  | —  |
| System reserved                     | 2                | 02 | —                          | 3F4 <sub>H</sub> | 000FFFF4 <sub>H</sub>  | —  |
| System reserved                     | 3                | 03 | —                          | 3F0 <sub>H</sub> | 000FFFF0 <sub>H</sub>  | —  |
| System reserved                     | 4                | 04 | —                          | 3EC <sub>H</sub> | 000FFFE <sub>C</sub>   | —  |
| System reserved                     | 5                | 05 | —                          | 3E8 <sub>H</sub> | 000FFFE8 <sub>H</sub>  | —  |
| System reserved                     | 6                | 06 | —                          | 3E4 <sub>H</sub> | 000FFFE4 <sub>H</sub>  | —  |
| Coprocessor absent trap             | 7                | 07 | —                          | 3E0 <sub>H</sub> | 000FFFE0 <sub>H</sub>  | —  |
| Coprocessor error trap              | 8                | 08 | —                          | 3DC <sub>H</sub> | 000FFFD <sub>C</sub>   | —  |
| INTE instruction                    | 9                | 09 | —                          | 3D8 <sub>H</sub> | 000FFFD8 <sub>H</sub>  | —  |
| Instruction break exception         | 10               | 0A | —                          | 3D4 <sub>H</sub> | 000FFFD4 <sub>H</sub>  | —  |
| Operand break trap                  | 11               | 0B | —                          | 3D0 <sub>H</sub> | 000FFFD0 <sub>H</sub>  | —  |
| Step trace trap                     | 12               | 0C | —                          | 3CC <sub>H</sub> | 000FFFC <sub>C</sub>   | —  |
| NMI request (tool)                  | 13               | 0D | —                          | 3C8 <sub>H</sub> | 000FFFC8 <sub>H</sub>  | —  |
| Undefined instruction exception     | 14               | 0E | —                          | 3C4 <sub>H</sub> | 000FFFC4 <sub>H</sub>  | —  |
| NMI request                         | 15               | 0F | 15 (F <sub>H</sub> ) fixed | 3C0 <sub>H</sub> | 000FFFC0 <sub>H</sub>  | —  |
| External interrupt 0                | 16               | 10 | ICR00                      | 3BC <sub>H</sub> | 000FFFB <sub>C</sub>   | —  |
| External interrupt 1                | 17               | 11 | ICR01                      | 3B8 <sub>H</sub> | 000FFFB8 <sub>H</sub>  | —  |
| External interrupt 2                | 18               | 12 | ICR02                      | 3B4 <sub>H</sub> | 000FFFB4 <sub>H</sub>  | —  |
| External interrupt 3                | 19               | 13 | ICR03                      | 3B0 <sub>H</sub> | 000FFFB0 <sub>H</sub>  | —  |
| External interrupt 4 (USB-function) | 20               | 14 | ICR04                      | 3AC <sub>H</sub> | 000FFFA <sub>C</sub>   | —  |
| External interrupt 5 (USB-Host)     | 21               | 15 | ICR05                      | 3A8 <sub>H</sub> | 000FFFA8 <sub>H</sub>  | —  |
| External interrupt 6 (OSDC)         | 22               | 16 | ICR06                      | 3A4 <sub>H</sub> | 000FFFA4 <sub>H</sub>  | —  |
| External interrupt 7                | 23               | 17 | ICR07                      | 3A0 <sub>H</sub> | 000FFFA0 <sub>H</sub>  | —  |
| Reload timer 0                      | 24               | 18 | ICR08                      | 39C <sub>H</sub> | 000FFF9 <sub>C</sub>   | 8  |
| Reload timer 1                      | 25               | 19 | ICR09                      | 398 <sub>H</sub> | 000FFF98 <sub>H</sub>  | 9  |
| Reload timer 2                      | 26               | 1A | ICR10                      | 394 <sub>H</sub> | 000FFF94 <sub>H</sub>  | 10 |
| UART0(Reception completed)          | 27               | 1B | ICR11                      | 390 <sub>H</sub> | 000FFF90 <sub>H</sub>  | 0  |
| UART1(Reception completed)          | 28               | 1C | ICR12                      | 38C <sub>H</sub> | 000FFF8 <sub>C</sub>   | 1  |
| UART2(Reception completed)          | 29               | 1D | ICR13                      | 388 <sub>H</sub> | 000FFF88 <sub>H</sub>  | 2  |
| UART0 (RX completed)                | 30               | 1E | ICR14                      | 384 <sub>H</sub> | 000FFF84 <sub>H</sub>  | 3  |
| UART1 (RX completed)                | 31               | 1F | ICR15                      | 380 <sub>H</sub> | 000FFF80 <sub>H</sub>  | 4  |
| UART2 (RX completed)                | 32               | 20 | ICR16                      | 37C <sub>H</sub> | 000FFF7 <sub>C</sub>   | 5  |

(Continued)

# MB91310 Series

| Interrupt source                 | Interrupt number |    | Interrupt level | Offset           | Address of TBR default | RN |
|----------------------------------|------------------|----|-----------------|------------------|------------------------|----|
|                                  | 10               | 16 |                 |                  |                        |    |
| DMAC0 (end, error)               | 33               | 21 | ICR17           | 378 <sub>H</sub> | 000FFF78 <sub>H</sub>  | —  |
| DMAC1 (end, error)               | 34               | 22 | ICR18           | 374 <sub>H</sub> | 000FFF74 <sub>H</sub>  | —  |
| DMAC2 (end, error)               | 35               | 23 | ICR19           | 370 <sub>H</sub> | 000FFF70 <sub>H</sub>  | —  |
| DMAC3 (end, error)               | 36               | 24 | ICR20           | 36C <sub>H</sub> | 000FFF6C <sub>H</sub>  | —  |
| DMAC4 (end, error)               | 37               | 25 | ICR21           | 368 <sub>H</sub> | 000FFF68 <sub>H</sub>  | —  |
| A/D                              | 38               | 26 | ICR22           | 364 <sub>H</sub> | 000FFF64 <sub>H</sub>  | —  |
| PPG0                             | 39               | 27 | ICR23           | 360 <sub>H</sub> | 000FFF60 <sub>H</sub>  | —  |
| PPG1                             | 40               | 28 | ICR24           | 35C <sub>H</sub> | 000FFF5C <sub>H</sub>  | —  |
| PPG2                             | 41               | 29 | ICR25           | 358 <sub>H</sub> | 000FFF58 <sub>H</sub>  | —  |
| PPG3                             | 42               | 2A | ICR26           | 354 <sub>H</sub> | 000FFF54 <sub>H</sub>  | —  |
| PWC                              | 43               | 2B | ICR27           | 350 <sub>H</sub> | 000FFF50 <sub>H</sub>  | —  |
| System reserved                  | 44               | 2C | ICR28           | 34C <sub>H</sub> | 000FFF4C <sub>H</sub>  | —  |
| System reserved                  | 45               | 2D | ICR29           | 348 <sub>H</sub> | 000FFF48 <sub>H</sub>  | —  |
| Main oscillation stabilization   | 46               | 2E | ICR30           | 344 <sub>H</sub> | 000FFF44 <sub>H</sub>  | —  |
| Timebase timer overflow          | 47               | 2F | ICR31           | 340 <sub>H</sub> | 000FFF40 <sub>H</sub>  | —  |
| System reserved                  | 48               | 30 | ICR32           | 33C <sub>H</sub> | 000FFF3C <sub>H</sub>  | —  |
| Clock timer                      | 49               | 31 | ICR33           | 338 <sub>H</sub> | 000FFF38 <sub>H</sub>  | —  |
| I <sup>2</sup> C ch0             | 50               | 32 | ICR34           | 334 <sub>H</sub> | 000FFF34 <sub>H</sub>  | —  |
| I <sup>2</sup> C ch1             | 51               | 33 | ICR35           | 330 <sub>H</sub> | 000FFF30 <sub>H</sub>  | —  |
| I <sup>2</sup> C ch2             | 52               | 34 | ICR36           | 32C <sub>H</sub> | 000FFF2C <sub>H</sub>  | —  |
| I <sup>2</sup> C ch3             | 53               | 35 | ICR37           | 328 <sub>H</sub> | 000FFF28 <sub>H</sub>  | —  |
| UART3(Reception completed)       | 54               | 36 | ICR38           | 324 <sub>H</sub> | 000FFF24 <sub>H</sub>  | —  |
| UART4(Reception completed)       | 55               | 37 | ICR39           | 320 <sub>H</sub> | 000FFF20 <sub>H</sub>  | —  |
| UART3 (RX completed)             | 56               | 38 | ICR40           | 31C <sub>H</sub> | 000FFF1C <sub>H</sub>  | —  |
| UART4(Reception completed)       | 57               | 39 | ICR41           | 318 <sub>H</sub> | 000FFF18 <sub>H</sub>  | —  |
| timer0                           | 58               | 3A | ICR42           | 314 <sub>H</sub> | 000FFF14 <sub>H</sub>  | —  |
| timer1                           | 59               | 3B | ICR43           | 310 <sub>H</sub> | 000FFF10 <sub>H</sub>  | —  |
| timer2                           | 60               | 3C | ICR44           | 30C <sub>H</sub> | 000FFF0C <sub>H</sub>  | —  |
| timer3                           | 61               | 3D | ICR45           | 308 <sub>H</sub> | 000FFF08 <sub>H</sub>  | —  |
| System reserved                  | 62               | 3E | ICR46           | 304 <sub>H</sub> | 000FFF04 <sub>H</sub>  | —  |
| Delay interrupt source bit       | 63               | 3F | ICR47           | 300 <sub>H</sub> | 000FFF00 <sub>H</sub>  | —  |
| System reserved (Used by REALOS) | 64               | 40 | —               | 2FC <sub>H</sub> | 000FFEFC <sub>H</sub>  | —  |
| System reserved (Used by REALOS) | 65               | 41 | —               | 2F8 <sub>H</sub> | 000FFEFC <sub>H</sub>  | —  |
| System reserved                  | 66               | 42 | —               | 2F4 <sub>H</sub> | 000FEFC <sub>H</sub>   | —  |

(Continued)

(Continued)

| Interrupt source        | Interrupt number |                | Interrupt level | Offset                                     | Address of TBR default                              | RN |
|-------------------------|------------------|----------------|-----------------|--|---|----|
|                         | 10               | 16             |                 |  |   |    |
| System reserved         | 67               | 43             | —               | 2F0 <sub>H</sub>                           | 000FFEF0 <sub>H</sub>                               | —  |
| System reserved         | 68               | 44             | —               | 2EC <sub>H</sub>                           | 000FFEEC <sub>H</sub>                               | —  |
| System reserved         | 69               | 45             | —               | 2E8 <sub>H</sub>                           | 000FFEE8 <sub>H</sub>                               | —  |
| System reserved         | 70               | 46             | —               | 2E4 <sub>H</sub>                           | 000FFEE4 <sub>H</sub>                               | —  |
| System reserved         | 71               | 47             | —               | 2E0 <sub>H</sub>                           | 000FFEE0 <sub>H</sub>                               | —  |
| System reserved         | 72               | 48             | —               | 2DC <sub>H</sub>                           | 000FFEDC <sub>H</sub>                               | —  |
| System reserved         | 73               | 49             | —               | 2D8 <sub>H</sub>                           | 000FFED8 <sub>H</sub>                               | —  |
| System reserved         | 74               | 4A             | —               | 2D4 <sub>H</sub>                           | 000FFED4 <sub>H</sub>                               | —  |
| System reserved         | 75               | 4B             | —               | 2D0 <sub>H</sub>                           | 000FFED0 <sub>H</sub>                               | —  |
| System reserved         | 76               | 4C             | —               | 2CC <sub>H</sub>                           | 000FFEC <sub>C</sub>                                | —  |
| System reserved         | 77               | 4D             | —               | 2C8 <sub>H</sub>                           | 000FFEC8 <sub>H</sub>                               | —  |
| System reserved         | 78               | 4E             | —               | 2C4 <sub>H</sub>                           | 000FFEC4 <sub>H</sub>                               | —  |
| System reserved         | 79               | 4F             | —               | 2C0 <sub>H</sub>                           | 000FFEC0 <sub>H</sub>                               | —  |
| Used by INT instruction | 80<br>to<br>255  | 50<br>to<br>FF | —               | 2BC <sub>H</sub><br>to<br>000 <sub>H</sub> | 000FFEC <sub>H</sub><br>to<br>000FFC00 <sub>H</sub> | —  |

# MB91310 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter                   | Symbol                   | Rating                |                        | Unit | Remarks |
|-----------------------------|--------------------------|-----------------------|------------------------|------|---------|
|                             |                          | Min                   | Max                    |      |         |
| Power supply voltage        | V <sub>DDE</sub> (3.3 V) | V <sub>SS</sub> – 0.5 | V <sub>SS</sub> + 4.0  | V    |         |
|                             | V <sub>DDI</sub> (2.5 V) | V <sub>SS</sub> – 0.5 | V <sub>SS</sub> + 3.0  | V    |         |
| Analog power supply voltage | A <sub>VCC</sub>         | V <sub>SS</sub> – 0.5 | V <sub>SS</sub> + 4.0  | V    |         |
| Input voltage               | V <sub>I</sub>           | V <sub>SS</sub> – 0.5 | V <sub>CC</sub> + 0.5  | V    |         |
| Analog pin input voltage    | V <sub>IA</sub>          | V <sub>SS</sub> – 0.5 | A <sub>VCC</sub> + 0.5 | V    |         |
| Output voltage              | V <sub>O</sub>           | V <sub>SS</sub> – 0.5 | V <sub>CC</sub> + 0.5  | V    |         |
| Storage temperature         | T <sub>stg</sub>         | – 40                  | + 125                  | °C   |         |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### 2. Recommended Operating Conditions

| Parameter                   | Symbol                   | Value |      | Unit | Remarks |
|-----------------------------|--------------------------|-------|------|------|---------|
|                             |                          | Min   | Max  |      |         |
| Operating temperature       | T <sub>a</sub>           | – 10  | + 70 | °C   |         |
| Power supply voltage        | V <sub>DDE</sub> (3.3 V) | 3.00  | 3.6  | V    |         |
|                             | V <sub>DDI</sub> (2.5 V) | 2.30  | 2.70 |      |         |
| Analog power supply voltage | A <sub>VCC</sub>         | 3.00  | 3.60 | V    |         |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.



# MB91310 Series

## 3. DC Characteristics

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                       | Symbol   | Conditions  | Value               |      |                      | Unit   | Remarks  |
|---|--|---|---------------------|------|----------------------|--|--|
|   |  |   | Min                 | Typ  | Max                  |  |  |
| Power supply                                    | I <sub>CC</sub>  | ROM product during normal operation<br>$T_a = +25\text{ }^\circ\text{C}$ ,<br>$f_{cp} = 40\text{ MHz}$ ,<br>$f_{cpp} = 20\text{ MHz}$ | —                   | 200  | 250                  | mA   | MB91F312A<br>Dot clock@90 MHz                      |
|   |  |   |                     | 220  | 270                  |  | MB91FV310A<br>Dot clock@90 MHz                     |
|   | I <sub>CCS</sub>   | Main sleep mode<br>$T_a = +25\text{ }^\circ\text{C}$ ,<br>$f_{cp} = 40\text{ MHz}$ ,<br>$f_{cpp} = 20\text{ MHz}$                     | —                   | 150  | 180                  | mA   | MB91F312A<br>Dot clock PLL STOP                    |
|   |  |   |                     | 170  | 200                  |  | MB91FV310A<br>Dot clock PLL STOP                   |
|   | I <sub>CCL</sub>   | Sub RUN mode<br>$T_a = +25\text{ }^\circ\text{C}$ ,<br>$f_{clk} = 32\text{ kHz}$  | —                   | 800  | 1500                 | $\mu\text{A}$                                      | MB91F312A<br>Dot clock PLL stop<br>USB clock stop  |
|   |  |   |                     | 1300 | 2000                 |  | MB91FV310A<br>Dot clock PLL stop<br>USB clock stop |
|   | I <sub>CCH</sub>   | Main stop mode<br>$T_a = +25\text{ }^\circ\text{C}$ , $f_{clk} = 0$   | —                   | 70   | 150                  | $\mu\text{A}$                                      | MB91F312A  |
|   |  |   |                     | 570  | 650                  |  | MB91FV310A   |
|   |  | $T_a = +70\text{ }^\circ\text{C}$ , $f_{clk} = 0$   | —                   | 500  | 2000                 | $\mu\text{A}$                                      | MB91F312A  |
|   |  |   |                     | 1000 | 2500                 |  | MB91FV310A   |
| I <sub>CCt</sub>                                | Clock mode<br>$T_a = +25\text{ }^\circ\text{C}$ ,<br>$f_{clk} = 32\text{ kHz}$ | —   | 600                 | 1000 | $\mu\text{A}$        | MB91F312A<br>Dot clock PLL stop<br>USB clock stop  |  |
|   |  |   | 1100                | 1500 |                      | MB91FV310A<br>Dot clock PLL stop<br>USB clock stop |  |
| H level input voltage                           | V <sub>IH</sub>  | *1  | $V_{CC} \times 0.8$ | —    | $V_{CC}$             | V  |  |
| L level input voltage                           | V <sub>IL</sub>  | $V_{CC} = 3.3\text{ V}$ , *1  | $V_{SS}$            | —    | $V_{CC} \times 0.2$  | V  |  |
|   |  | $V_{CC} = 2.5\text{ V}$   |                     |      | $V_{CC} \times 0.15$ | V  |  |
| H level output voltage                          | V <sub>OH</sub>  | $V_{DDE} = 3.3\text{ V}$ ,<br>$I_{OH} = -4\text{ mA}$ , *2  | $V_{CC} - 0.5$      | —    | $V_{CC}$             | V  |  |
|   |  | $V_{DDE} = 2.5\text{ V}$ ,<br>$I_{OH} = -4\text{ mA}$ , *3  | $V_{CC} - 0.5$      | —    | $V_{CC}$             | V  |  |
| L level output voltage                          | V <sub>OL</sub>  | $V_{DDE} = 3.3\text{ V}$ ,<br>$I_{OL} = 4\text{ mA}$ , *2, *3   | $V_{SS}$            | —    | 0.4                  | V  |  |
| Input leak current                              | I <sub>IL</sub>  | $T_a = +70\text{ }^\circ\text{C}$   | -5                  | —    | +5                   | $\mu\text{A}$                                      |  |
| I <sup>2</sup> C bus switch connection resistor | RBS  | —   | —                   | —    | 130                  | $\Omega$   | Between SCL3 and SCL4<br>Between SDA3 and SDA4     |

\*1 : P0 to P7, DOCKI, HSYNC, YSYNC

\*2 : P0 to P7

\*3 : B0 to B2, G0 to B2, R0 to R2, VOB1, VOB2, DCK0, FH

# MB91310 Series

## 4. USB

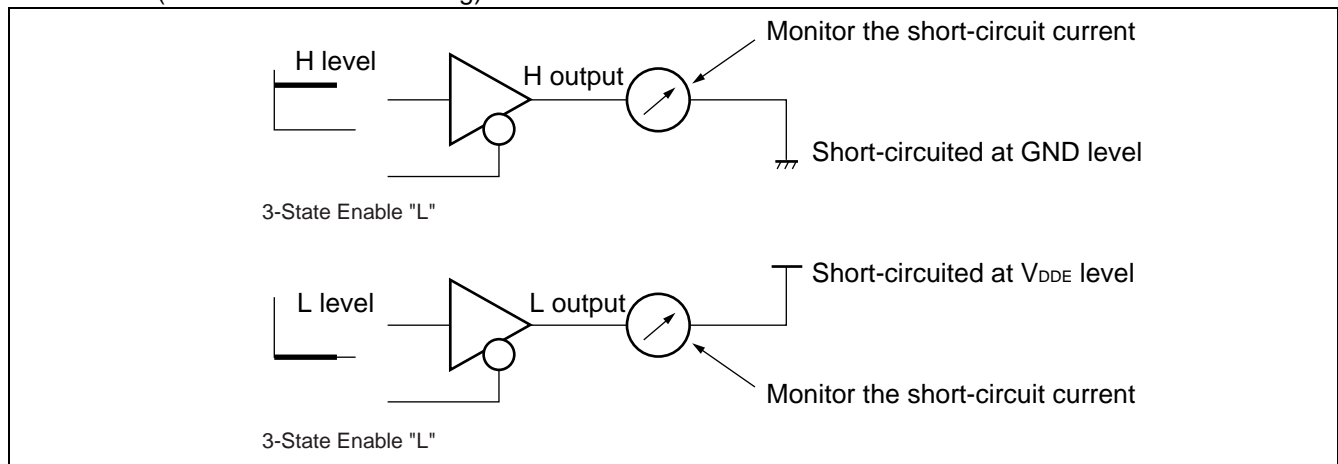
### (1) DC Characteristics

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                    | Symbol   | Pin | Conditions                                      | Value           |     |           | Unit          | Remarks |
|------------------------------|----------|-----|---|-----------------|-----|-----------|---------------|---------|
|                              |          |     |   | Min             | Typ | Max       |               |         |
| H level output voltage       | $V_{OH}$ | —   | $I_{OH} = -100\text{ }\mu\text{A}$              | $V_{DDE} - 0.2$ | —   | $V_{DDE}$ | V             |         |
| Output Level Voltage         | $V_{OL}$ | —   | $I_{OL} = 100\text{ }\mu\text{A}$               | 0               | —   | 0.2       | V             |         |
| H level output current       | $I_{OH}$ | —   | Full Speed<br>$V_{OH} = V_{DDE} - 0.4\text{ V}$ | -20             | —   | —         | mA            |         |
|                              |          |     | Low Speed<br>$V_{OH} = V_{DDE} - 0.4\text{ V}$  | -6              | —   | —         |               |         |
| L level output current       | $I_{OL}$ | —   | Full Speed<br>$V_{OL} = 0.4\text{ V}$           | 20              | —   | —         | mA            |         |
|                              |          |     | Low Speed<br>$V_{OL} = 0.4\text{ V}$            | 6               | —   | —         |               |         |
| output short circuit current | $I_{OS}$ | —   | —   | —               | —   | 300       | mA            | *1      |
| Input leak current           | $I_{LZ}$ | —   | —   | —               | —   | $\pm 5$   | $\mu\text{A}$ | *2      |

\*1 : About the output short-circuit current  $I_{OS}$

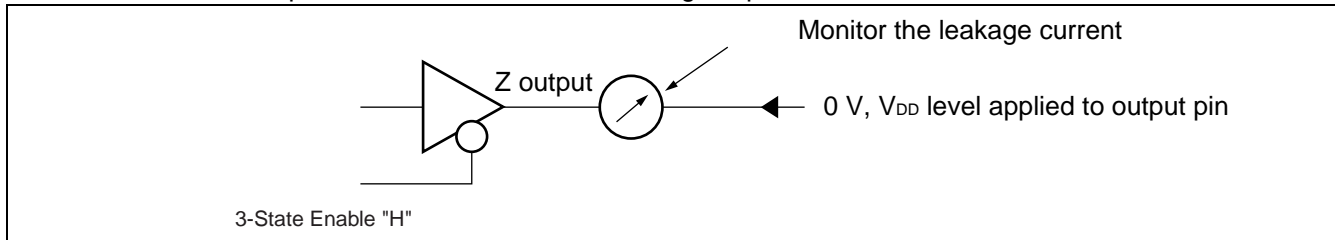
The output short-circuit current  $I_{OS}$  is the maximum current that flows when the output pin is connected to  $V_{DDE}$  or  $V_{SS}$  (within the maximum rating).



About the output short-circuit current: This is the short-circuit current per differential output pin on one side. As this USB I/O buffer is a differential output, consider both of the two pins.

\*2 : About Z leakage current  $I_{LZ}$  measurement

The input leakage current  $I_{LZ}$  indicates the leakage current that flows when the  $V_{DDE}$  or  $V_{SS}$  voltage is applied to the bidirectional pin with the USB I/O buffer in a high impedance state.



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## (2) DC characteristics

Conforming to the USB Specification Revision 1.1.

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                     | Symbol     | Value |       | Unit      | Remarks                      |
|---|------------|-------|-------|-----------|------------------------------|
|   |            | Min   | Max   |           |                              |
| "H" level input voltage (driven)              | $V_{IH}$   | 2.0   | —     | V         | *1                           |
| "L" level input voltage                       | $V_{IL}$   | —     | 0.8   | V         | *1                           |
| Differential Input Sensitivity                | $V_{DI}$   | 0.2   | —     | V         | *2                           |
| Differential Common Mode Range                | $V_{CM}$   | 0.8   | 2.5   | V         | *2                           |
| "H" level output voltage (driven)             | $V_{OH}$   | 2.8   | 3.6   | V         | *3                           |
| "L" level output voltage                      | $V_{OL}$   | 0.0   | 0.3   | V         | *3                           |
| External Output Signal Crossover Voltage      | $V_{CRS}$  | 1.3   | 2.0   | V         | *4                           |
| Bus Pull-Up Resistor on Upstream Port         | RPU        | 1.425 | 1.575 | $k\Omega$ | $1.5\text{ k}\Omega \pm 5\%$ |
| Bus Pull-Down Resistor on Downstream Port     | RPD        | 1.425 | 1.575 | $k\Omega$ | $1.5\text{ k}\Omega \pm 5\%$ |
| Termination voltage for upstream port pull-up | $V_{TERM}$ | 3.0   | 3.6   | V         | *5                           |

\*1 : About input voltages  $V_{IH}$  and  $V_{IL}$

The Single-End-Receiver switching threshold voltage of the USB I/O buffer is set within the range of  $V_{IL}$  (Max) = 0.8 V and  $V_{IH}$  (Min) = 2.0 V (TTL input standard).

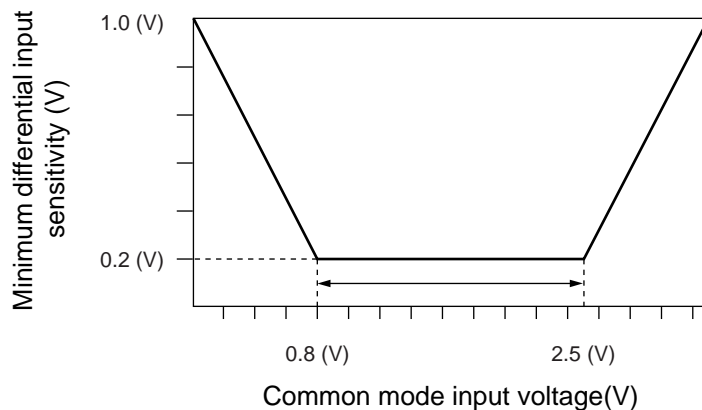
Appropriate hysteresis is provided to reduce noise sensitivity.

\*2 : About input voltages  $V_{DI}$  and  $V_{CM}$

The Differential-Receiver is used to receive USB differential data signals.

The Differential-Receiver has a differential input sensitivity of 200 mV when the differential data input remains in the range of 0.8 to 2.5 V to the local ground reference level.

The above voltage range is referred to as the common mode input voltage range.

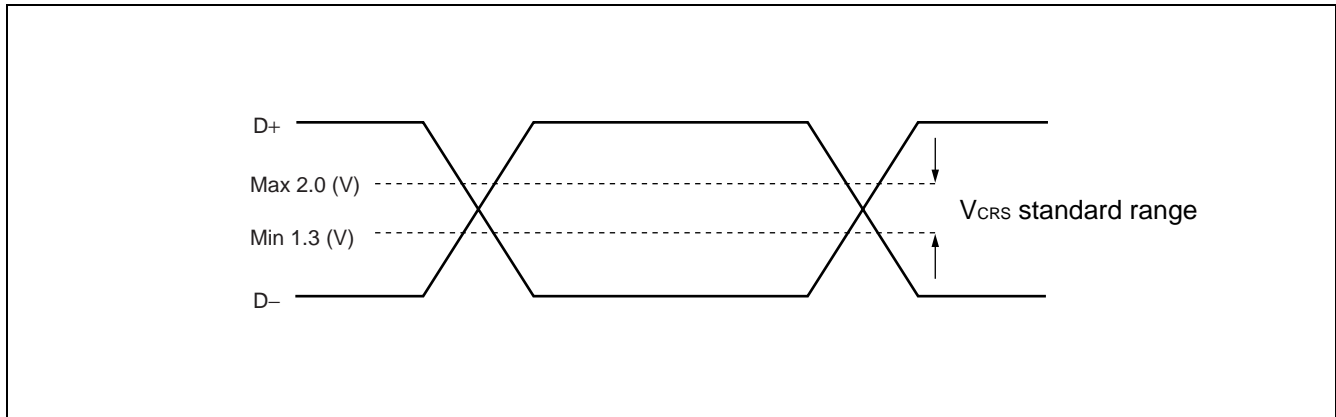


**\*3 : About output voltages  $V_{OL}$  and  $V_{OH}$**

The output drive capabilities of the driver are 0.3 V or less in Low-State ( $V_{OL}$ ) (when 1.5 k $\Omega$  is loaded at 3.6 V) and 2.8 V or more in High-State ( $V_{OH}$ ) (when 15 k $\Omega$  is loaded at the ground).

**\*4 : About output voltages  $V_{CRS}$**

The cross voltage of the external differential output signal (D+/D-) of the USB I/O buffer ranges from 1.3 V to 2.0 V.



**\*5 : About termination  $V_{TERM}$**

$V_{TERM}$  represents the pull-up voltage at the upstream port.

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## 5. AC Characteristics

### (1) Clock Timing

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                          | Symbol           | Pin    | Condi-<br>tions | Value |        |       | Unit | Remarks   |
|------------------------------------|------------------|--------|-----------------|-------|--------|-------|------|---|
|                                    |                  |        |                 | Min   | Typ    | Max   |      |   |
| Clock frequency                    | fc               | X0, X1 | —               | —     | 10.135 | —     | MHz  | PLL system (Operation at a maximum internal speed of 40.54 MHz by quadrupling a self-oscillation frequency of 10.135 MHz via PLL) |
| Internal operating clock frequency | fc <sub>p</sub>  | —      | —               | 2.53  | —      | 40.54 | MHz  | CPU   |
|                                    | fc <sub>pp</sub> | —      | —               | 2.53  | —      | 20.27 | MHz  | Peripheral  |

### (2) Reset

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

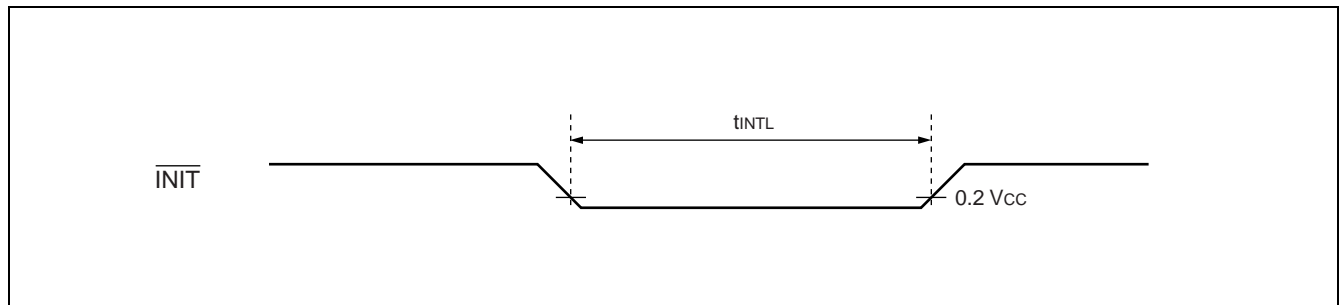
| Parameter                                  | Symbol            | Pin                      | Condi-<br>tions | Value               |     | Unit | Remarks |
|--|-------------------|--------------------------|-----------------|---------------------|-----|------|---------|
|  |                   |                          |                 | Min                 | Max |      |         |
| INIT input time (at power-on)              | t <sub>INTL</sub> | $\overline{\text{INIT}}$ | —               | *                   | —   | ns   |         |
| INIT input time (other than at power - on) |                   |                          |                 | t <sub>CP</sub> × 5 | —   | ns   |         |
| INIT input time (stop recovery time)       |                   |                          |                 | *                   | —   | ns   |         |

\* : INIT input time (at power-on)

FAR, CERLOCK :  $\phi \times 2^{15}$  or greater recommended

Crystal :  $\phi \times 2^{21}$  or greater recommended

$\phi$  : Power on → X0/X1 period × 2



## (3) UART timing

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

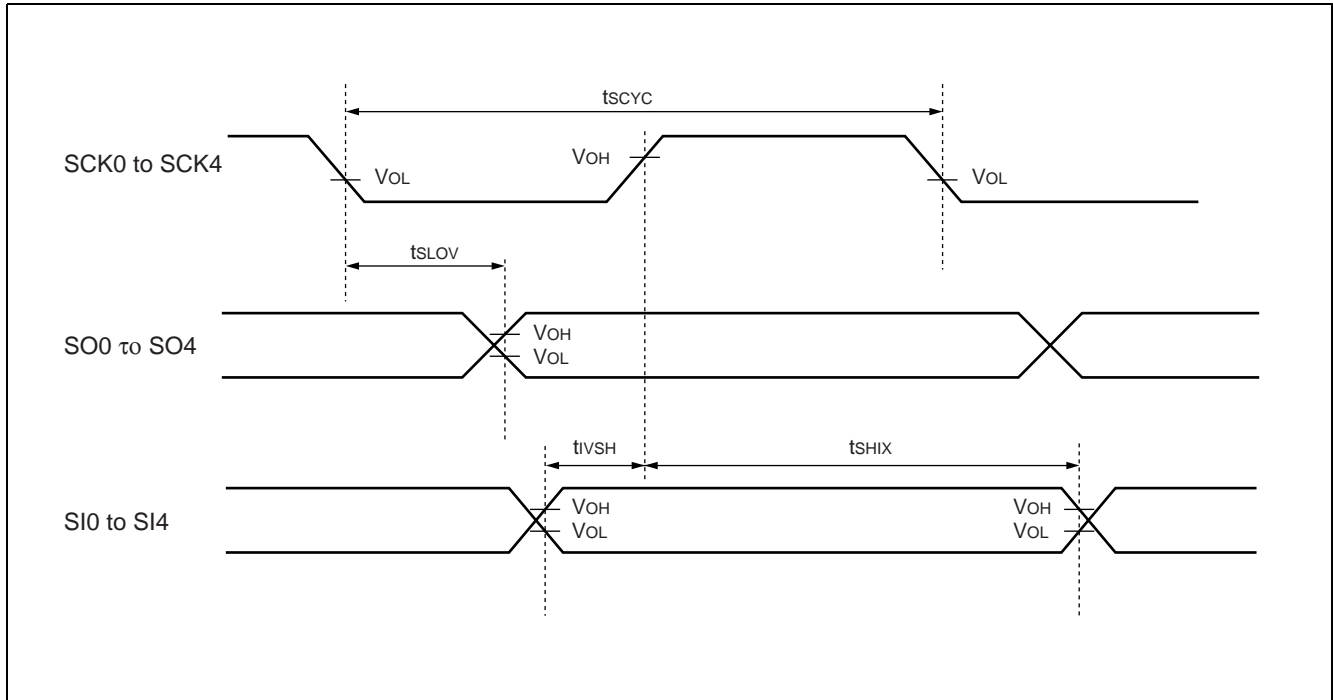
| Parameter                  | Symbol     | Pin                        | Conditions               | Value          |      | Unit | Remarks |
|----------------------------|------------|----------------------------|--------------------------|----------------|------|------|---------|
|                            |            |                            |                          | Min            | Max  |      |         |
| Serial clock cycle time    | $t_{SCYC}$ | SCK0 to SCK4               | internal shift lock mode | $8 t_{CYCP}^*$ | —    | ns   |         |
| SCK↓ → SO delay time       | $t_{SLOV}$ | SCK0 to SCK4<br>SO0 to SO4 |                          | - 80           | + 80 | ns   |         |
| Valid SI → SCK↑            | $t_{IVSH}$ | SCK0 to SCK4<br>SI0 to SI4 |                          | 100            | —    | ns   |         |
| SCK↑ → valid SI hold time  | $t_{SHIX}$ | SCK0 to SCK4<br>SI0 to SI4 |                          | 60             | —    | ns   |         |
| Serial clock H pulse width | $t_{SHSL}$ | SCK0 to SCK4               | external shift lock mode | $4 t_{CYCP}^*$ | —    | ns   |         |
| Serial clock L pulse width | $t_{LSLH}$ | SCK0 to SCK4               |                          | $4 t_{CYCP}^*$ | —    | ns   |         |
| SCK↓ → SO delay time       | $t_{SLOV}$ | SCK0 to SCK4<br>SO0 to SO4 |                          | —              | 150  | ns   |         |
| Valid SI → SCK↑            | $t_{IVSH}$ | SCK0 to SCK4<br>SI0 to SI4 |                          | 60             | —    | ns   |         |
| SCK↑ → valid SI hold time  | $t_{SHIX}$ | SCK0 to SCK4<br>SI0 to SI4 |                          | 60             | —    | ns   |         |

\* :  $t_{CYCP}$  indicates the peripheral clock cycle time.

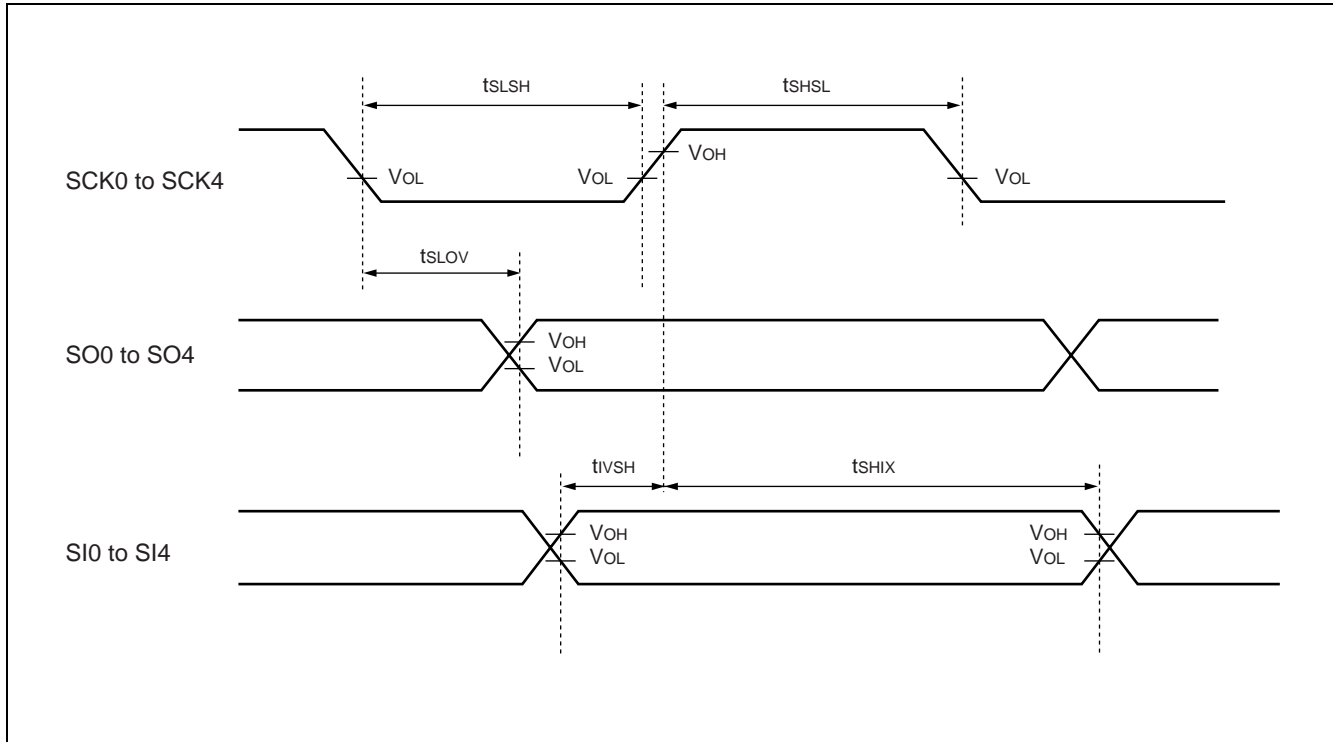
Note : AC characteristic in CLK synchronized mode.

# MB91310 Series

- Internal shift clock mode



- External shift clock mode



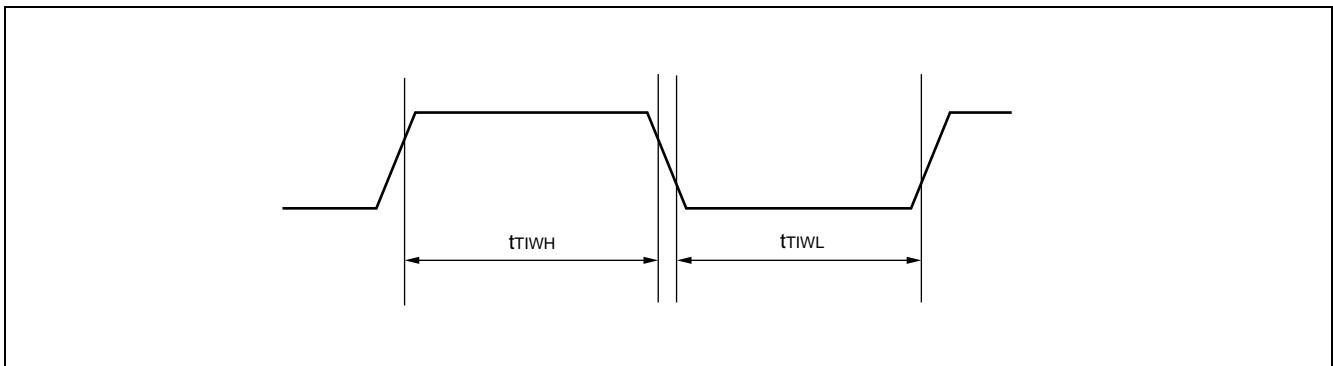


## (4) Reload timer clock, PPG timer input, and multi-function timer input timings

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter         | Symbol                   | Pin  | Conditions | Value          |     | Unit | Remarks |
|-------------------|--------------------------|--|------------|----------------|-----|------|---------|
|                   |                          |  |            | Min            | Max |      |         |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN0 to TIN2<br>PPG0 to PPG3<br>TRG0 to TRG3<br>TI0 to TI3 | —          | $2 t_{CYCP}^*$ | —   | ns   |         |

\* :  $t_{CYCP}$  indicates the peripheral clock cycle time.

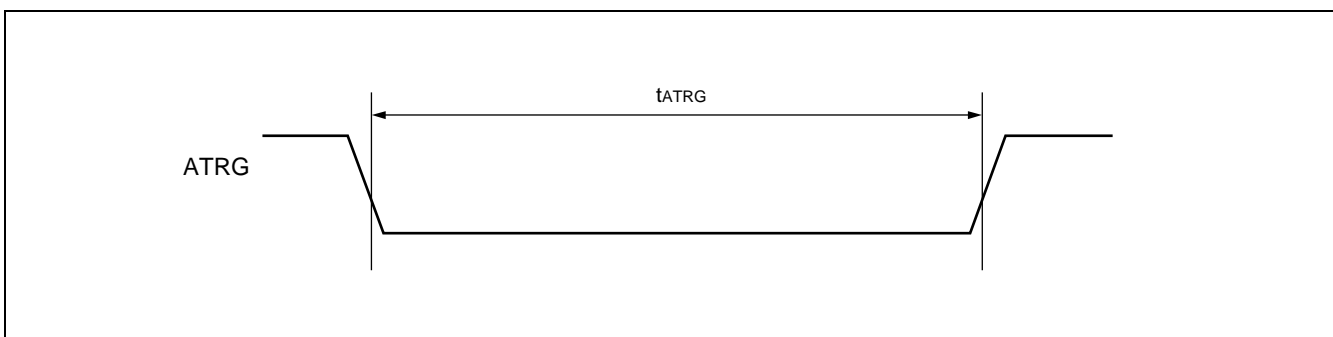


## (5) Trigger Input Timing

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Symbol     | Pin  | Conditions | Value          |     | Unit | Remarks |
|-----------------------------------|------------|------|------------|----------------|-----|------|---------|
|                                   |            |      |            | Min            | Max |      |         |
| A/D activation trigger input time | $t_{ATRG}$ | ATRG | —          | $5 t_{CYCP}^*$ | —   | ns   |         |

\* :  $t_{CYCP}$  indicates the peripheral clock cycle time.

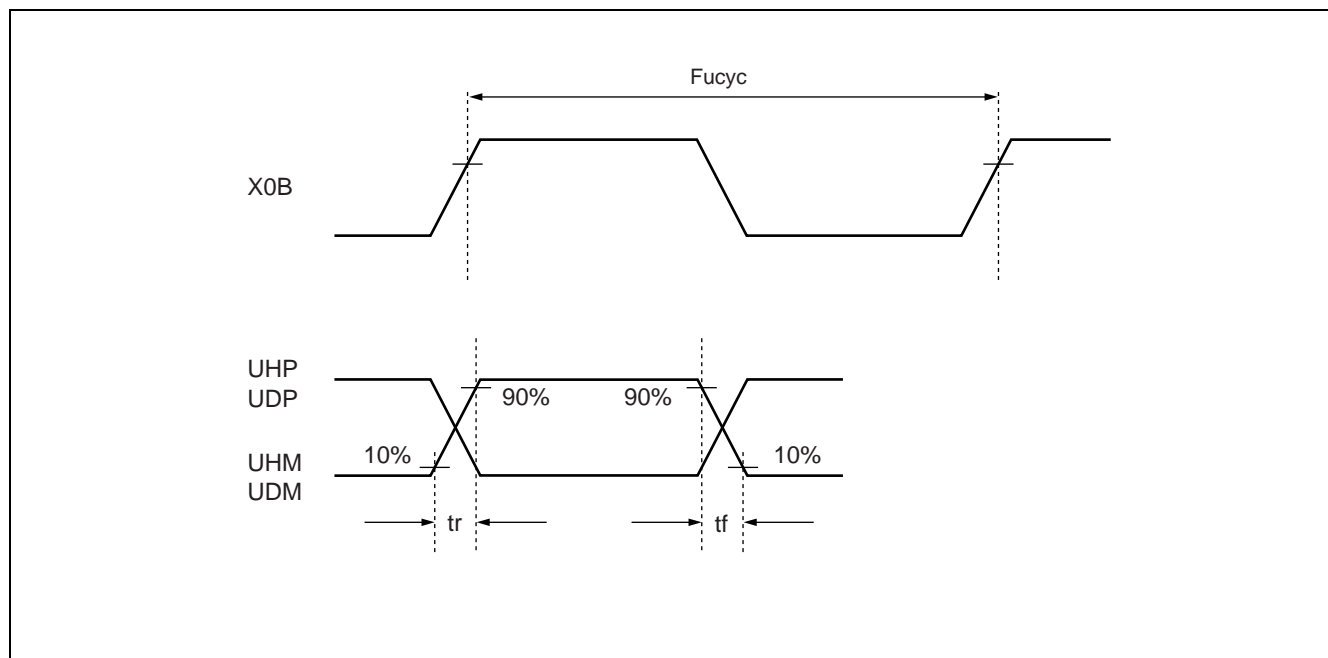


# MB91310 Series

## (6) USB interface

( $T_a = -10\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                     | Symbol | Pin                | Condi-<br>tions | Value |       |        | Unit     | Remarks   |
|---|--------|--------------------|-----------------|-------|-------|--------|----------|---|
|   |        |                    |                 | Min   | Typ   | Max    |          |   |
| Input clock                                   | Fucyc  | X0B, X1B           | —               | —     | 48 *1 | —      | MHz      | Self-oscillation<br>at a precision<br>of 500 ppm *1 |
|   |        | X0B                |                 |       |       |        |          | External input<br>at a precision<br>of 500 ppm *1   |
| Rise Time                                     | tr     | UHP/UHM<br>UDP/UDM | Full Speed      | 4     | —     | 20     | ns       | *2  |
|   |        | UHP/UHM            | Low Speed       | 75    | —     | 300    | ns       | *2  |
| Fall Time                                     | tf     | UHP/UHM<br>UDP/UDM | Full Speed      | 4     | —     | 20     | ns       | *2  |
|   |        | UHP/UHM            | Low Speed       | 75    | —     | 300    | ns       | *2  |
| Differential Rise and<br>Fall Timing Matching | Tfrfm  | UHP/UHM<br>UDP/UDM | Full Speed      | 90    | —     | 111.11 | %        | *2  |
|   |        | UHP/UHM            | Low Speed       | 80    | —     | 125    | %        | *2  |
| Driver Output<br>Resistance                   | Rzdrv  | UDP<br>UDM         | —               | 28    | —     | 44     | $\Omega$ | *3  |



\*1 : The AC characteristics of the USB interface conform to the USB Specification Revision 1.1.

\*2 : About driver characteristics tr, tf, and Tfrfm

These represent the rise (tr) and fall (tf) time standards of the differential data signal.

These are defined as times between 10% and 90% of the output signal voltage.

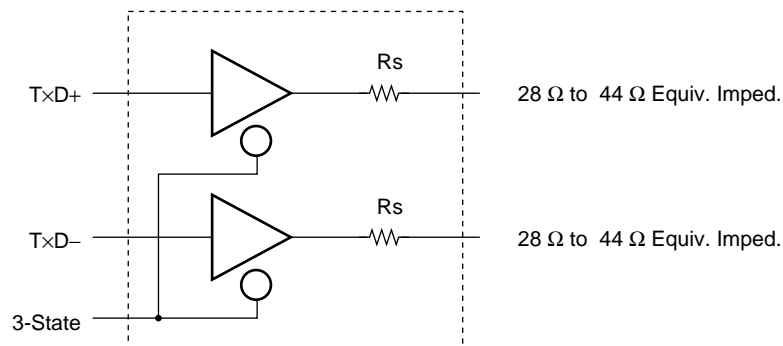
For full-speed buffer, the tr/tf ratio is specified to fall within  $\pm 10\%$  to minimize RFI radiation.

\*3 : About driver characteristic ZDRV

USB full-speed connection is made by the twisted pair cable shielded at a characteristic impedance ( $Z_0$ ) of  $90 \Omega \pm 15\%$ . The USB Specification stipulates that the USB driver output impedance be within the range of  $28 \Omega$  to  $44 \Omega$ . The USB Specification also stipulates that a discrete serial resistor ( $R_s$ ) be added for balancing purposes while satisfying the above standards.

The output impedance of the USB I/O buffer in this LSI is about  $3 \Omega$  to  $19 \Omega$ .

As the serial resistor  $R_s$ , therefore, a  $25 \Omega$  to  $30 \Omega$  type ( $27 \Omega$  type recommended) should be added.



Driver output impedance  $3 \Omega$  to  $19 \Omega$   
 $R_s$   $25 \Omega$  to  $30 \Omega$  (recommended value:  $27 \Omega$ )

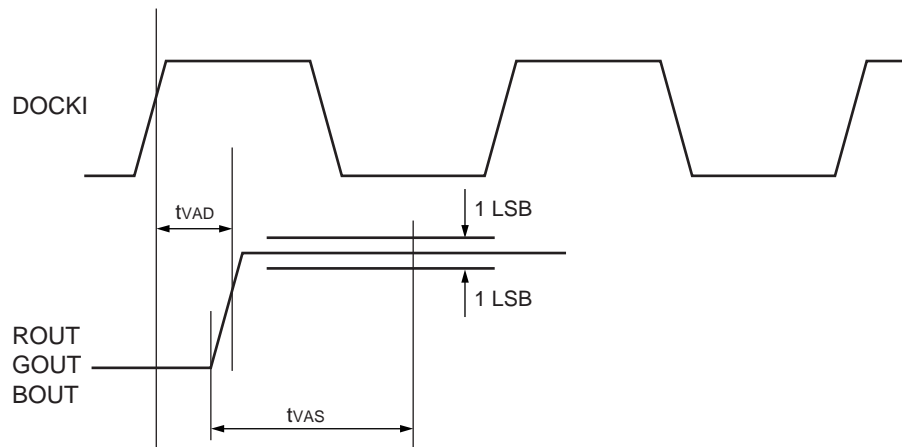
# MB91310 Series

## (7) Analog RGB

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                       | Symbol    | Pin                    | Conditions   | Value |     |     | Unit | Remarks |
|---------------------------------|-----------|------------------------|--|-------|-----|-----|------|---------|
|                                 |           |                        |  | Min   | Typ | Max |      |         |
| Analog RGB output delay         | $t_{VAD}$ | ROUT,<br>GOUT,<br>BOUT | $V_{REF} = 1.1\text{ V}$ ,<br>$V_{DDR} = V_{DDG} = V_{DDB} = 2.5\text{ V}$ ,                 | —     | 5   | —   | ns   | —       |
| Analog RGB output settling time | $t_{VAS}$ | ROUT,<br>GOUT,<br>BOUT | $V_{RO} = 2.7\text{ k}\Omega$ ,<br>$R_{COMP} = G_{COMP} = B_{COMP} = 0.1\text{ }\mu\text{F}$ | —     | 10  | —   | ns   | —       |

### • Display signal output timing



## (8) Digital RGB

Vertical sync, horizontal sync, and display output control signal input timings

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                          | Symbol     | Pin   | Value          |               | Unit          | Remarks |
|------------------------------------|------------|-------|----------------|---------------|---------------|---------|
|                                    |            |       | Min            | Max           |               |         |
| Horizontal sync signal cycle time  | $t_{HCYC}$ | HSYNC | $100 + t_{WH}$ | —             | Dot clock     |         |
| Horizontal sync signal pulse width | $t_{WH}$   | HSYNC | 20             | —             | Dot clock     | *1      |
|                                    |            |       | —              | 6             | $\mu\text{s}$ |         |
| Horizontal sync signal setup time  | $t_{DHST}$ | HSYNC | 4              | —             | ns            |         |
| Horizontal sync signal hold time   | $t_{DHHD}$ |       | 0              | —             | ns            |         |
| Vertical sync signal setup time    | $t_{HVST}$ | VSYNC | 5              | $1H^{*2} - 5$ | Dot clock     |         |
| Vertical sync signal hold time     | $t_{HVHD}$ |       | 3              | —             | $H^{*2}$      |         |
| Input sync signal rise/fall time   | $t_{DR}$   | HSYNC | —              | 5             | ns            |         |
|                                    | $t_{DF}$   | VSYNC |                |               |               |         |

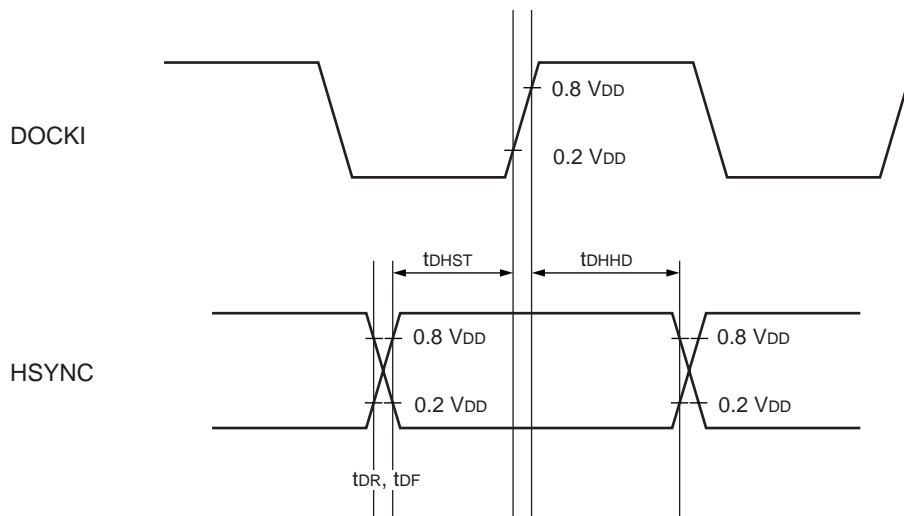
\*1 : During the horizontal sync signal pulse period, the device stops its internal OSDG operation, disabling writing to the internal VRAM. Therefore, set the horizontal sync signal pulse width and VRAM write cycle to ensure that: horizontal sync signal pulse width < VRAM write cycle.

Precisely, adjust the command issuance interval not to issue command 2 or command 4 (VRAM write command) more than once in the horizontal sync signal pulse with period.

If the above condition is not satisfied, the device may fail writing to VRAM.

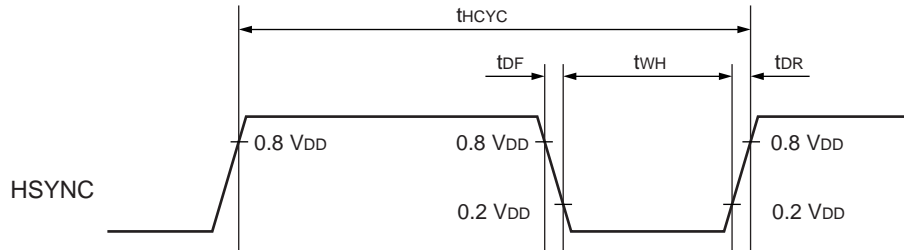
\*2 : 1H is assumed to be one horizontal sync signal period.

### • Horizontal sync, and display output control signal input timings



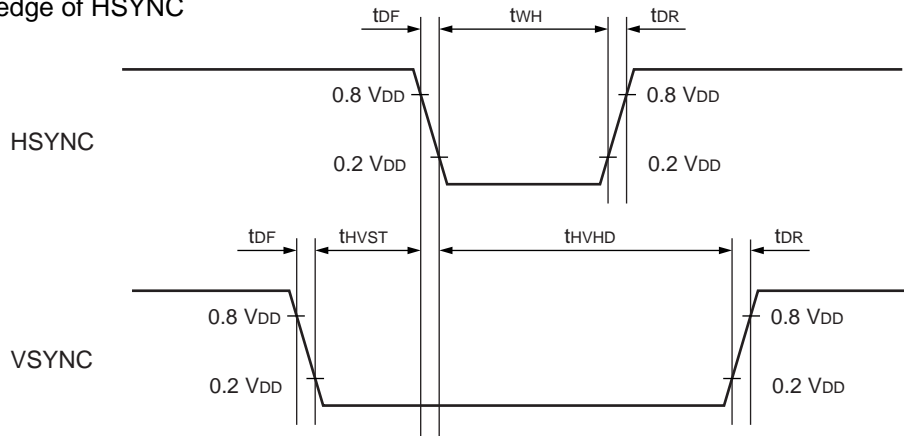
# MB91310 Series

- Horizontal sync signal input

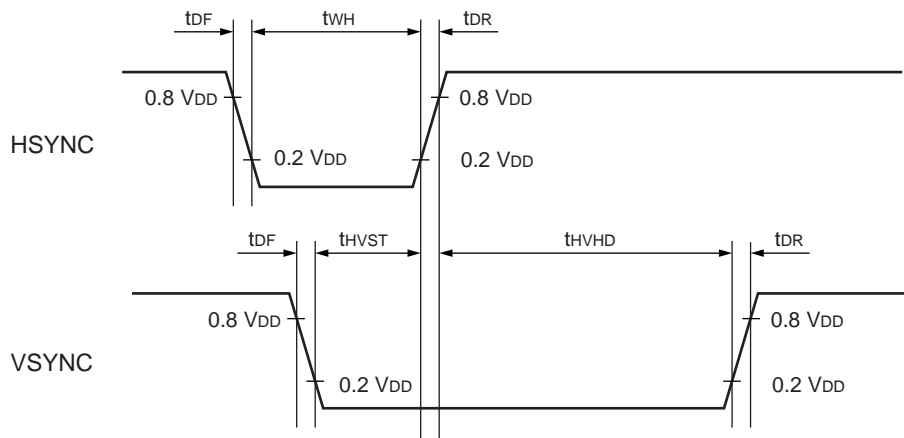


- Vertical sync signal input timing

- Leading edge of HSYNC



- Trailing edge of HSYNC



## Display signal timing

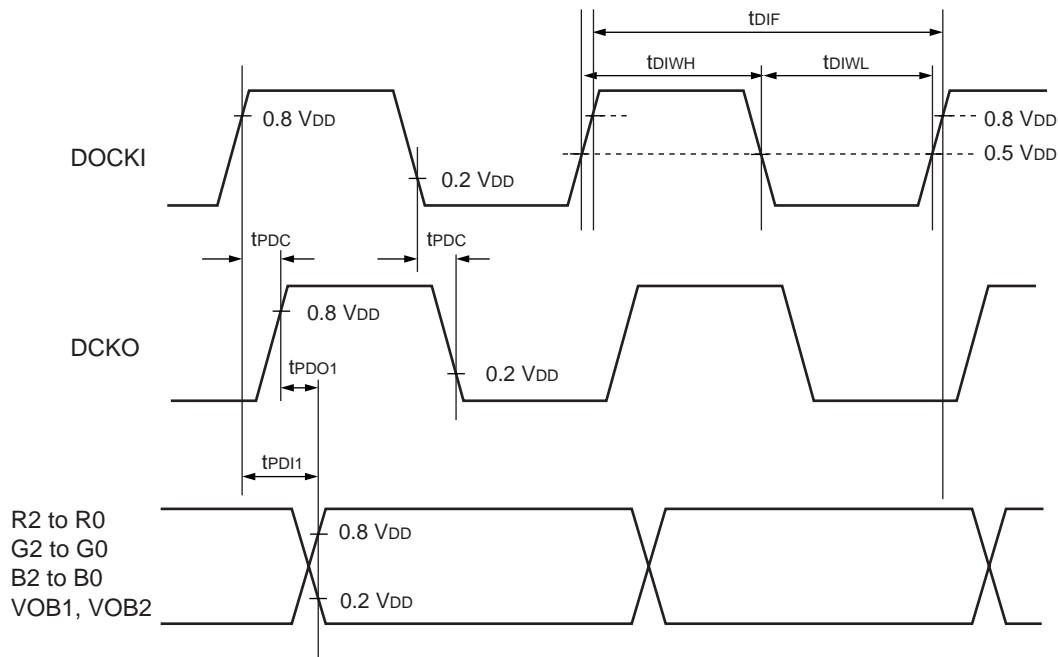
( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                           | Symbol     | Pin   | Value |     | Unit | Remarks |
|-------------------------------------|------------|---|-------|-----|------|---------|
|                                     |            |   | Min   | Max |      |         |
| Dot clock input cycle time          | $t_{DIF}$  | DOCKI   | 11    | 90  | MHz  | *1      |
| Dot clock input pulse width         | $t_{DIWH}$ | DOCKI   | 3.5   | —   | ns   | *1      |
|                                     | $t_{DIWL}$ |   | 3.5   | —   | ns   |         |
| Dot clock output delay time 1       | $t_{PDC}$  | DCKO  | 3     | 8   | ns   | *2      |
| Display signal output delay time I1 | $t_{PDI1}$ | R2 to R0,<br>B2 to B0,<br>G2 to G0,<br>VOB1, VOB2 | 2     | 8   | ns   | *2      |
| Display signal output delay time O1 | $t_{PDO1}$ | R2 to R0,<br>B2 to B0,<br>G2 to G0,<br>VOB1, VOB2 | -4    | 5   | ns   | *2      |

\*1 : Input a continuous dot clock signal without a break.

\*2 : Output load of 16 pF

### • Display signal output timing



# MB91310 Series

## 6. 0.25 μm Technology About the Power-on Sequence for Dual-power-supply Models

- The power supplies must be turned on in the VDDI→AVCC, AVRH→VDDE order and off in the VDDE→AVCC, AVRH→VDDI order.  
When VDDI is turned on earlier, the potential difference between VDDI and VDDE must be within 3.6 V.
- Turn on VDDE before turning on analog power supply AVCC and applying the analog signal.

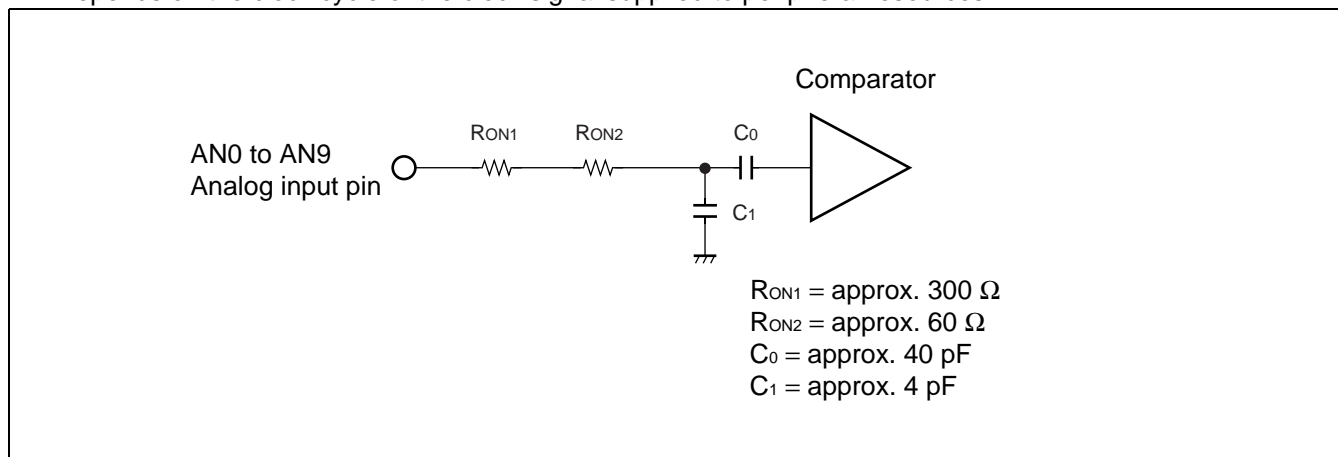
## 7. Electrical Characteristics for the A/D Converter

( $T_a = -10\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $AV_{RH} = 3.0\text{ V}$  to  $3.6\text{ V}$ )

| Parameter   | value      |     |            | Unit | Remarks  |
|---|------------|-----|------------|------|--|
|   | Min        | Typ | Max        |      |  |
| Resolution  | —          | —   | 10         | bit  |  |
| Total error*1   | - 5.5      | —   | + 5.5      | LSB  | AVCC = 3.3 V,<br>AVRH = 3.3 V<br>(CPU in sleep mode) |
| Nonlinear error*1   | - 3.5      | —   | + 3.5      | LSB  |  |
| Differential linear error*1                               | - 2.0      | —   | + 2.0      | LSB  |  |
| Zero transition voltage*1                                 | - 4.0      | —   | + 6.0      | LSB  |  |
| Full transition voltage*1                                 | AVRH - 5.5 | —   | AVRH + 3.0 | LSB  |  |
| Conversion time   | 10 *2      | —   | —          | μs   |  |
| Power supply current<br>(analog + digital)                | —          | 3.6 | —          | mA   |  |
|   | —          | —   | 5          | μA   | Stop converting                                      |
| Reference power supply current<br>(between AVRH and AVRL) | —          | 470 | —          | μA   | AVRH = 3.0 V, AVRL = 0.0 V                           |
|   | —          | —   | 10         | μA   | Stop converting                                      |
| Analog input capacitance                                  | —          | 40  | —          | pF   |  |
| Interchannel disparity                                    | —          | —   | 4          | LSB  |  |

\*1 : Measured in the CPU sleep state

\*2 : Depends on the clock cycle of the clock signal supplied to peripheral resources.





## ■ ORDERING INFORMATION

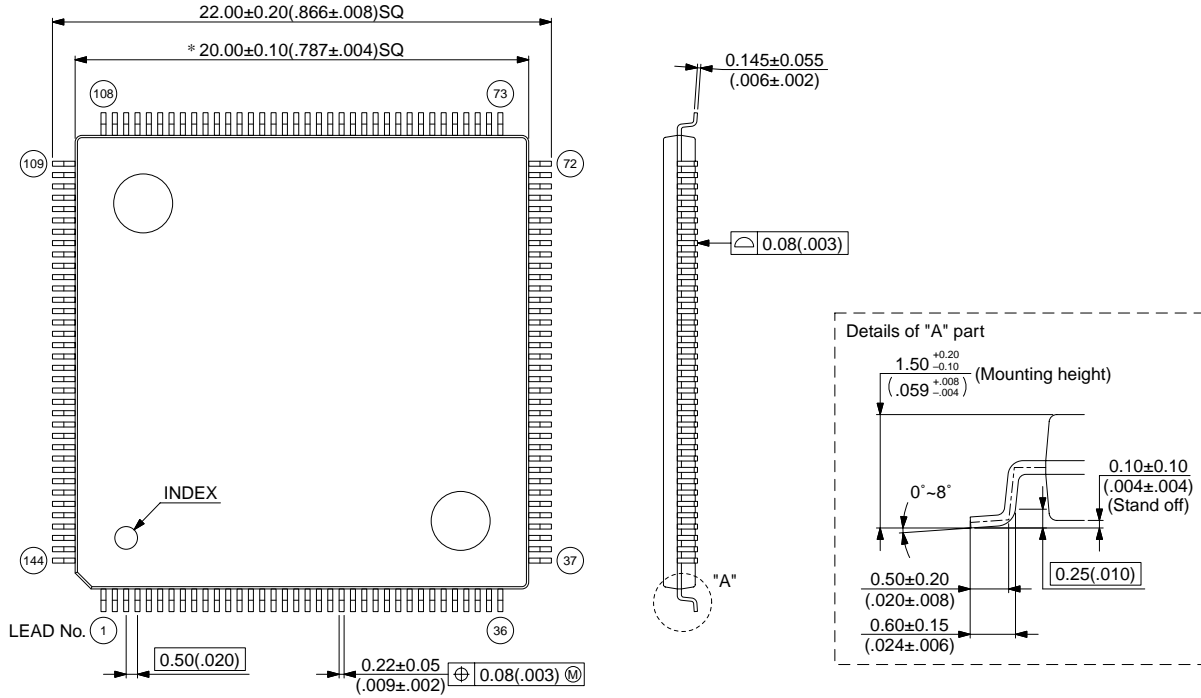
| Part number             | Package                                | Remarks               |
|-------------------------|--|-----------------------|
| MB91F312APFV-1xx-BND-E1 | 144-pin plastic LQFP<br>(FPT-144P-M08) | Lead Free Package     |
| MB91FV310APFV-ES        | 144-pin plastic LQFP<br>(FPT-144P-M08) | For development tools |

# MB91310 Series

## PACKAGE DIMENSION

144-pin plastic LQFP  
(FPT-144P-M08)

- Note 1) \* : Values do not include resin protrusion.  
Resin protrusion is +0.25 (.010) Max (each side) .  
Note 2) Pins width and pins thickness include plating thickness.  
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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