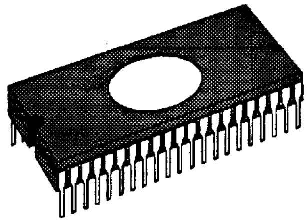
SGS-THOMSON MICROELECTRONICS

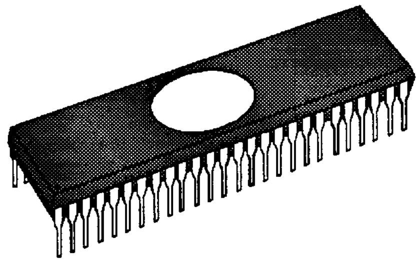
ST72E71
ST72T71

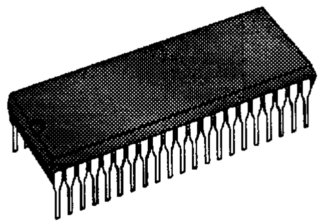
8-BIT EPROM HCMOS MCUs WITH EEPROM AND TV/MONITOR DEDICATED FUNCTIONS

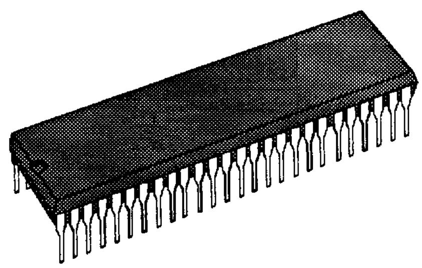
PRELIMINARY DATA

- 5V ± 10% supply operating range
- 4MHz Maximum Internal Clock Frequency
- Fully static operation
- 0 to +70°C Operating Temperature Range
- Run, Wait, and Stop Modes
- User EPROM: up to 15144 bytes
  Data RAM: up to 256 bytes
  EEPROM: up to 512 bytes
  EWPCC EEPROM: 256 bytes
- 56 pin Windowed Ceramic Shrink Dual In line Package (ST7271N)
  42 pin Windowed Ceramic Shrink Dual In Line Package (ST7271J)
- up to 27 I/O lines
  8 I/O Open Drain with 12V capability
- up to 8 lines programmable as interrupt wake-up inputs
- 16-bit timer with 2 input capture and 2 output compare functions
- Sync Processor for video timing analysis
- East/West Pin Cushion Automatic Correction with DAC output.
- Watchdog for system reliability and integrity
- 8-bit Analog to Digital Converter with up to 8 channels
- 16 10-bit PWM/BRM Digital to Analog outputs
- 2 12-bit PWM/BRM Digital to Analog outputs
- Industry Standard Serial Peripheral Interface
- User mask options:
  - SPI Data Rate
  - Watchdog enable/disable after Reset
  - Watchdog enable during WAIT mode
- Master Reset and Power-on reset
- Full Hardware Emulator
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on Real-time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)


CSDIP42W


CSDIP56W


PSDIP42


PSDIP56

(Ordering Information at the end of the datasheet)

Figure 1a. 56 Pin Shrink DIP Pinout

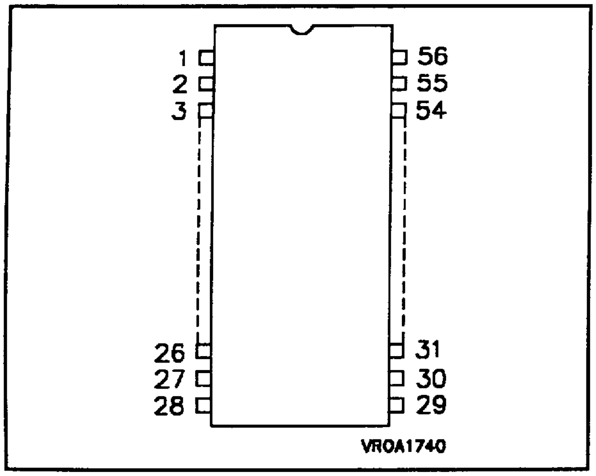
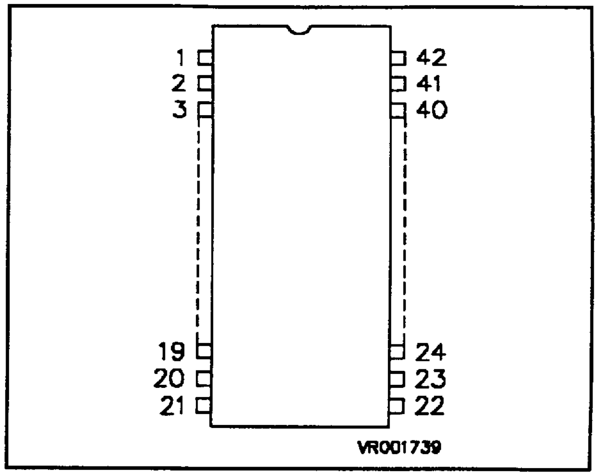


Figure 1b. 42 Pin Shrink DIP Pinout



Pin Description

Pin	Name	Pin	Name
1	V_{DDA}	56	V_{SSA}
2	EWPCC	55	V_{SS}
3	DA0	54	PC5/$\overline{SS}$
4	DA1	53	PC4/SCK
5	DA2	52	PC3/MOSI
6	DA3	51	PC2/MISO
7	DA4	50	PC1
8	DA5	49	PC0/OCMP
9	DA6	48	TEST/V_{PP}
10	DA7	47	DA17
11	DA8	46	DA16
12	DA9	45	DA15
13	PB7	44	DA14
14	PB6	43	PA0
15	PB5	42	PA1
16	PB4	41	PA2
17	PB3	40	PA3
18	PB2	39	PA4
19	PB1	38	PA5
20	VFBACK/PB0	37	PA6
21	PD4	36	PA7
22	CLMPO/PD3	35	DA13
23	DA10	34	DA12
24	DA11	33	OSCIN
25	$\overline{RESET}$	32	OSCOUT
26	VSYNCO/PD2	31	CSYNCI/PDO
27	VSYNCI	30	HSYNCO/PD1
28	V_{DD}	29	HSYNCI

Pin Description

Pin	Name	Pin	Name
1	V_{DDA}	42	V_{SSA}
2	EWPCC	41	V_{SS}
3	DA0	40	PC5/$\overline{SS}$
4	DA1	39	PC4/SCK
5	DA2	38	PC3/MOSI
6	DA3	37	PC2/MISO
7	DA4	36	PC0/OCMP
8	DA5	35	TEST/V_{PP}
9	DA6	34	PA0
10	DA7	33	PA1
11	DA8	32	PA2
12	DA9	31	PA3
13	PB3	30	PA4
14	PB2	29	PA5
15	PB1	28	PA6
16	VFBACK/PB0	27	PA7
17	CLMPO/PD3	26	OSCIN
18	$\overline{RESET}$	25	OSCOUT
19	VSYNCO/PD2	24	CSYNCI/PDO
20	VSYNCI	23	HSYNCO/PD1
21	V_{DD}	22	HSYNCI

1 GENERAL DESCRIPTION

4.1 INTRODUCTION

The ST72E71,T71 is a HCMOS microcontroller unit (MCU) from the ST72 family with dedicated peripherals for TV and Monitor applications.

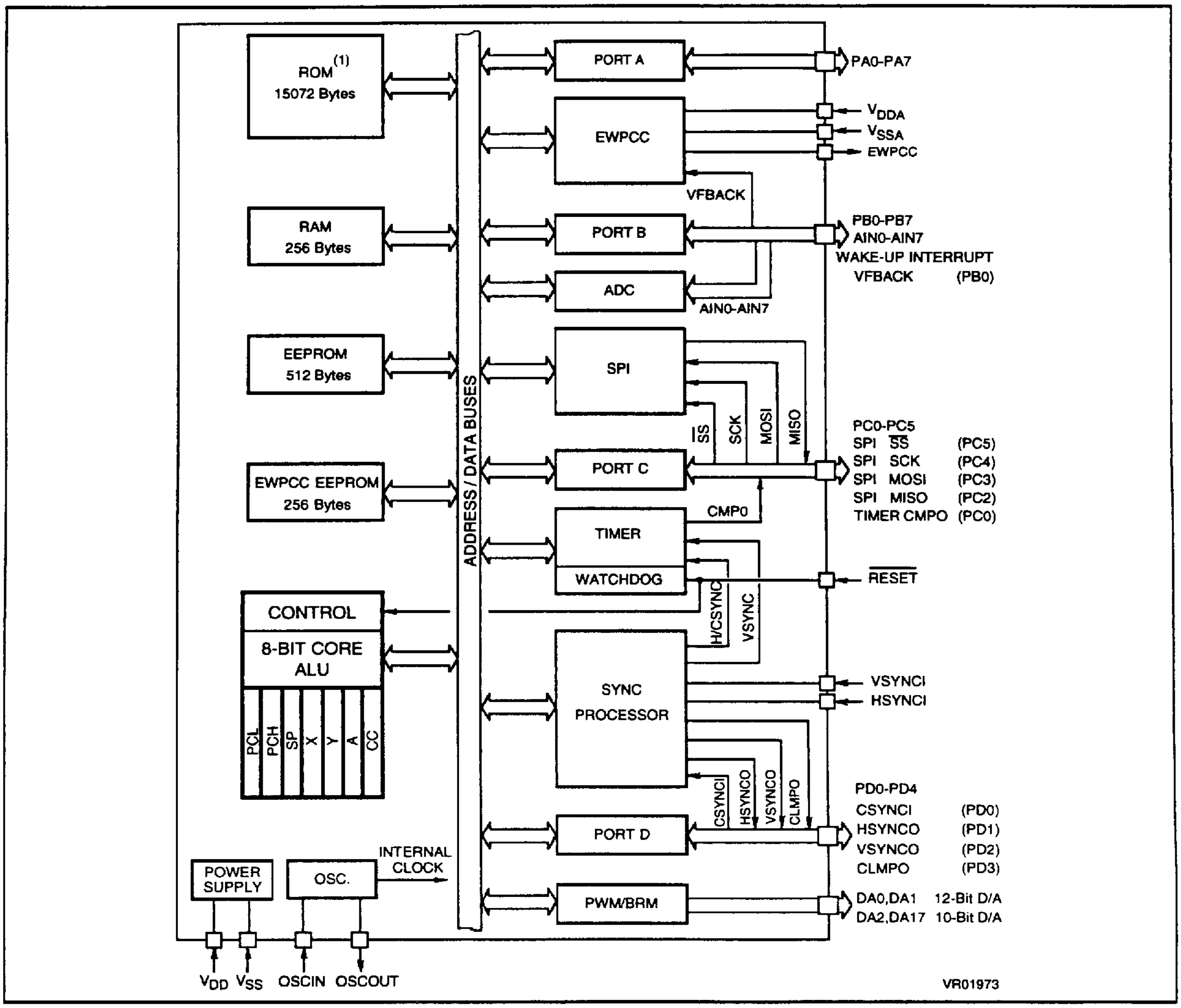
The ST72E71 is the EPROM version of the ST7271 ROM device, suitable for development. The ST72T71 is the OTP version, suitable for product prototyping and low volume production.

It is based around an industry standard 8-bit core and offers an enhanced instruction set. The processor runs with an external clock at 8 MHz with a 5V supply. Due to the fully static design of this device, operation down to DC is possible. Under software control the ST72E71,T71 can be placed in WAIT or STOP mode thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential.

The device includes an on-chip oscillator, CPU, ROM, RAM, EEPROM, I/O, a timer with 2 input capture and 2 output compare signals, an 8-channel Analog to Digital Converter and an industry standard SPI as standard peripherals.

Dedicated functions include a Sync Processor for video timing analysis, East-West Pin Cushion automatic correction and 18 PWM/BRM outputs for analog control of external functions.

Figure 2. ST7271 Block Diagram



Note 1 : ROM is replaced by EPROM for EPROM/OTP versions.

4.2 PIN DESCRIPTION

V_{DD}. Power supply voltage

V_{SS}. Digital and Analog Ground

V_{DDA}. Analog V_{DD} and reference for EWPCC Digital to Analog Converter (DAC, 8 Volts).

V_{SSA}. Analog V_{SS} for EWPCC DAC.

OSCIN, OSCOUT. Oscillator input and output pins. These pins are to be connected to a parallel resonant crystal or ceramic resonator. An external clock source can also be connect to OSCIN.

$\overline{\text{RESET}}$. The active low input signal forces the initialization of the MCU. This event is the top priority non maskable interrupt. This pin is switched low when the Watchdog has triggered. It can be used to reset external peripherals.

TEST/V_{PP}. This pin must be held low for normal application. In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}.

VFBACK (PB0). Vertical Flyback signal (TTL level). This pin accepts the Vertical Flyback signal used for timing correlation for the East-west Pin Cushion correction when this is used or is PB0.

EWPCC. Analog output of correction signal from East-West Pin Cushion controller (2-6V, I_{OUT} = 1mA).

OCMP (PC0). Output compare signal coming from the TIMER. This output signal, according to a register bit option, can be the OCMP pin (for output compare 1 of the timer) or the PC0 pin.

MISO (PC2). SPI Master Out/Slave In Data Output/Input when SPI is enabled or PC2.

MOSI (PC3). SPI Master In/Slave Out Data Input/Output when SPI is enabled or PC3.

SCK (PC4). SPI Serial Clock when SPI is enabled or PC4

$\overline{\text{SS}}$ (PC5). SPI Slave Select when SPI is enabled or PC5.

VSYNCI. Vertical Sychronization Input (TTL level)

HSYNCI. Horizontal Sychronization Input (TTL level)

CSYNCI (PD0). Composite Sychronization Input (TTL level). This pin accepts the composite synchronisation input when the Sync Processor I/O functions are enabled or is PD0.

HSYNCO (PD1). Horizontal Sychronization Output. This pin outputs the horizontal synchronisation output from the Sync Processor (or HSYNCI) when the Sync Processor I/O functions are enabled or is PD1.

VSYNCO (PD2). Vertical Sychronization Output. This pin outputs the vertical synchronisation output from the Sync Processor (or VSYNCI) when the Sync Processor I/O functions are enabled or is PD2.

CLMPO (PD3). Clamp Output. This pin outputs the clamping (back porch) output signal from the Sync Processor (or HSYNCI) when the Sync Processor I/O functions are enabled or is PD3.

DA2-DA17 (56-pin package),
DA2-DA9 (42-pin package), 10-bit PWM/BRM outputs (for Analog controls, after external filtering)

DA0, DA1. 12-bit PWM/BRM outputs (for Analog Controls, after external filtering).

PA0-PA7, PB0-PB7, PC0-PC5, PD0-PD4 (56 pin package). These 27 lines are standard I/O lines, programmable as either input or output.

- **PORT A.** 8 I/O lines, bit programmable, accessed through DDRA and DRA Registers. Each bit can be defined as a standard input port bit without pull-up resistor or as an open drain output port (up to 12V).

- **PORT B**. 8 Standard I/O lines bit programmable accessed through DDRB and DRB Registers. Each bit can be programmed as an analog input (by control bits in the PORT B Configuration register), digital input (with internal pull-up resistor), push-pull digital output or as interrupt wake-up (with pull-up). These negative edge or low-level sensitive interrupt lines can wake-up the ST7271 from WAIT or STOP mode. This feature allows to build low power applications when the ST7271 can be waken-up from keyboard push.
PB0 is used for the East-West Pin cushion controller VFBACK input as shown above when the EWPCC is used.

- **PORT C.** 6 Standard I/O lines accessed through DDRC and DRC Registers. Each bit can be programmed as digital input (with or without pull-up internal resistor), open drain output or SPI control and data signals (as shown for the dedicated SPI signals above) whenever the SPI is active, the outputs are in the pull-pull configuration.
The pull-up resistor is enabled for all bits present by one control bit in the Programmable Input/Output Configuration Register. The resistor is automatically disabled for the pins used for the SPI when the SPI is enabled.

- **PORT D.** 4 Standard I/O lines bit programmable accessed through DDRD and DRD Registers. Each bit can be programmed as an input (with internal pull-up resistor), push-pull output or Synchronization inputs and outputs to/from the Sync Processor. When programmed as inputs, Video Synchronisation signals can be directly inspected. The inputs may also be passed through the Sync Processor to the Timer Input Captures

These pin functions are also summarised in the following table, which also indicates the availability of functions for the 42-pin SDIP package.

PIN DESCRIPTION (Continued)

Table 1. ST72E71,T71 Pin Description

Pin Name	Pin Function(s)	56 Pins	42 Pins
V_{DDA}	Analog V_{DD} for EWPCC	1	1
EWPCC	EWPCC output voltage	2	2
DA0	12-bit PWM/BRM output*	3	3
DA1	12-bit PWM/BRM output	4	4
DA2	10-bit PWM/BRM output*	5	5
DA3	10-bit PWM/BRM output	6	6
DA4	10-bit PWM/BRM output	7	7
DA5	10-bit PWM/BRM output	8	8
DA6	10-bit PWM/BRM output	9	9
DA7	10-bit PWM/BRM output	10	10
DA8	10-bit PWM/BRM output	11	11
DA9	10-bit PWM/BRM output	12	12
PB7	I/O Port PB7	13	
PB6	I/O Port PB6	14	
PB5	I/O Port PB5	15	
PB4	I/O Port PB4	16	
PB3	I/O Port PB3	17	13
PB2	I/O Port PB2	18	14
PB1	I/O Port PB1	19	15
VFBACK/PB0	I/O Port PB0 /VFBACK Input	20	16
PD4	I/O Port PD4	21	
CLMPO/PD3	I/O Port PD3/Clamp Output	22	17
DA10	10-bit PWM/BRM output 10	23	
DA11	10-bit PWM/BRM output 11	24	
$\overline{\text{RESET}}$	Reset Input/Output	25	18
VSYNCO/PD2	I/O Port PD2/VSYNC Output	26	19
VSYNCI	VSYNC Input to Sync Processor	27	20
V_{DD}	Power Supply	28	21
HSYNCI	HSYNC Input to Sync Processor	29	22
HSYNCO/PD1	I/O Port PD1/HSYNC Output	30	23
CSYNCI/PDO	I/O Port PD0/CSYNC Input	31	24
OSCOUT	Oscillator Output	32	25
OSCIN	Oscillator Input	33	26
DA12	10-bit PWM/BRM output 12	34	
DA13	10-bit PWM/BRM output 13	35	
PA7	I/O Port PA7	36	27
PA6	I/O Port PA6	37	28
PA5	I/O Port PA5	38	29
PA4	I/O Port PA4	39	30
PA3	I/O Port PA3	40	31
PA2	I/O Port PA2	41	32
PA1	I/O Port PA1	42	33
PA0	I/O Port PA0	43	34
DA14	10-bit PWM/BRM output 14	44	
DA15	10-bit PWM/BRM output 15	45	
DA16	10-bit PWM/BRM output 16	46	
DA17	10-bit PWM/BRM output 17	47	
TEST/V_{PP}	TEST pin must be held low. EPROM Prog. voltage input	48	35
PC0/OCMP	I/O Port PC0, Timer Output Compare	49	36
PC1	I/O Port PC1	50	
PC2/MISO	I/O Port PC2, SPI Data	51	37
PC3/MOSI	I/O Port PC3, SPI Data	52	38
PC4/SCK	I/O Port PC4, SPI Clock output	53	39
PC5/$\overline{\text{SS}}$	I/O Port PC5, SPI Slave Select	54	40
V_{SS}	Digital ground	55	41
V_{SSA}	Analog ground for EWPCC	56	42

Note * : Open Drain

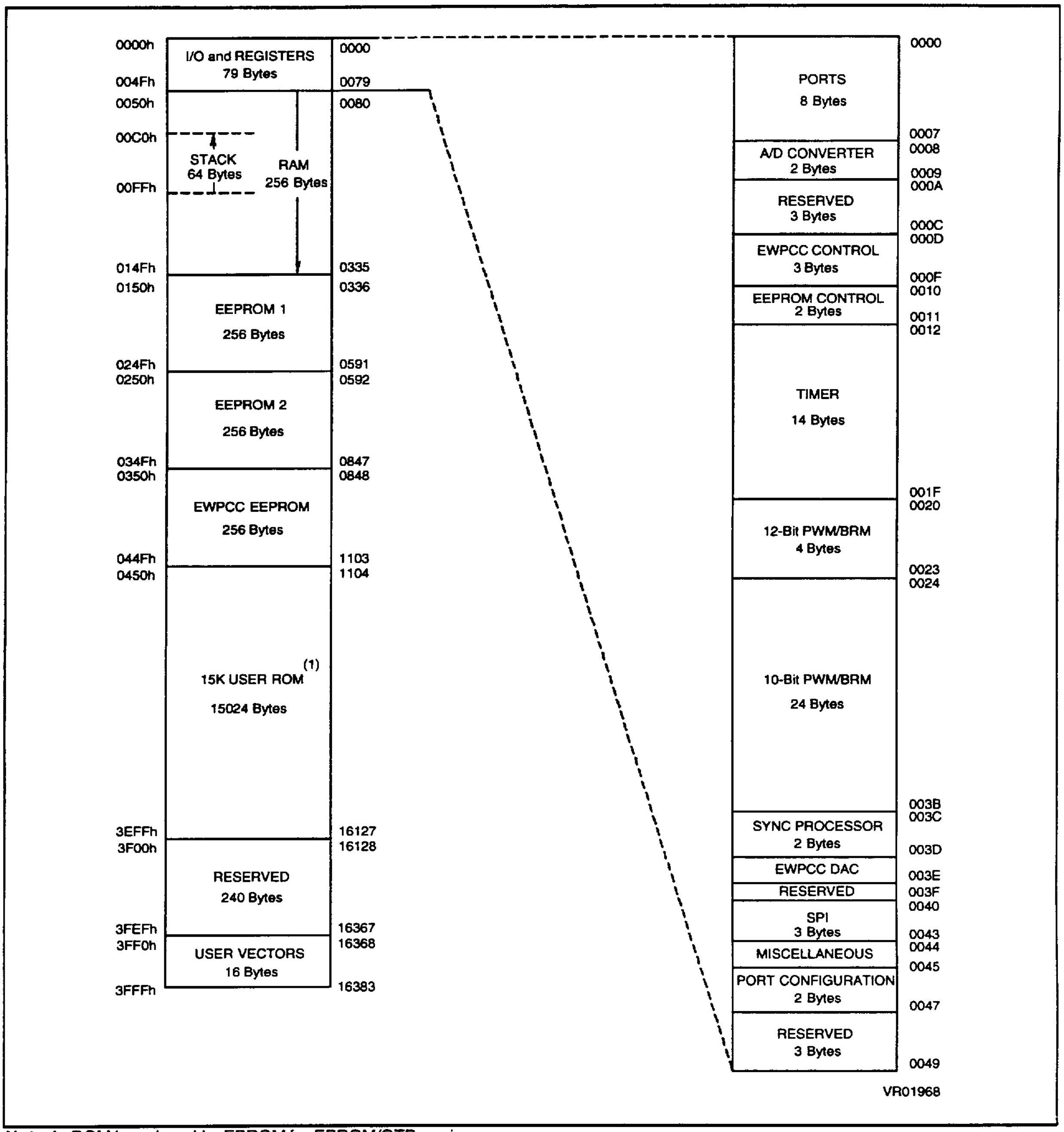
4.3 MEMORY MAP

As shown in Figure 3, the MCU is capable of addressing 16K bytes of memory and I/O registers. In the ST72E71,T71, 16383 of these bytes are user accessible.

The available memory locations consist of 80 bytes of I/O registers, 256 bytes of RAM, 512 bytes of EEPROM, 256 bytes of EWPCC EEPROM and 15Kbytes of user EPROM. The RAM space includes 64 bytes for the stack from 014Fh to 010Fh.

The highest address bytes contain the user defined reset and interrupt vectors.

Figure 3. Memory Map



Note 1 : ROM is replaced by EPROM for EPROM/OTP versions.

4.4 I/O and REGISTER MAP

Address	Register Name
0000h	PORT A DATA REGISTER
0001h	PORT B DATA REGISTER
0002h	PORT C DATA REGISTER
0003h	PORT D DATA REGISTER
0004h	PORT A DATA DIRECTION REGISTER
0005h	PORT B DATA DIRECTION REGISTER
0006h	PORT C DATA DIRECTION REGISTER
0007h	PORT D DATA DIRECTION REGISTER
0008h	A/D DATA REGISTER
0009h	A/D CONTROL/STATUS REGISTER
000Ah-000Ch	Reserved
000Dh	EWPCC0 REGISTER
000Eh	EWPCC1 REGISTER
000Fh	EWPCC EEPROM CONTROL REGISTER
0010h	EEPROM 1 CONTROL REGISTER
0011h	EEPROM 2 CONTROL REGISTER
0012h	TIMER CONTROL REGISTER
0013h	TIMER STATUS REGISTER
0014h	INPUT CAPTURE REGISTER 1, High
0015h	INPUT CAPTURE REGISTER 1, Low
0016h	OUTPUT COMPARE REGISTER 1, High
0017h	OUTPUT COMPARE REGISTER 1, Low
0018h	COUNTER REGISTER, High
0019h	COUNTER REGISTER, Low
001Ah	ALTERNATE COUNTER REGISTER, High
001Bh	ALTERNATE COUNTER REGISTER, Low
001Ch	INPUT CAPTURE REGISTER 2, High
001Dh	INPUT CAPTURE REGISTER 2, Low
001Eh	OUTPUT COMPARE REGISTER 2, High
001Fh	OUTPUT COMPARE REGISTER 2, Low
0020h	PWM0 - 12 bit PWM/BRM
0021h	BRM0 - 12 bit PWM/BRM
0022h	PWM1 - 12 bit PWM/BRM
0023h	BRM1 - 12 bit PWM/BRM
0024h	PWM2 - 10 bit PWM/BRM
0025h	BRM2+BRM3

Address	Register Name
0026h	PWM3
0027h	PWM4
0028h	BRM4+BRM5
0029h	PWM5
002Ah	PWM6
002Bh	BRM6+BRM7
002Ch	PWM7
002Dh	PWM8
002Eh	BRM8+BRM9
002Fh	PWM9
0030h	PWM10
0031h	BRM10+BRM11
0032h	PWM11
0033h	PWM12
0034h	BRM12+BRM13
0035h	PWM13
0036h	PWM14
0037h	BRM14+BRM15
0038h	PWM15
0039h	PWM16
003Ah	BRM16+BRM17
003Bh	PWM17
003Ch	SYNC MUX CONTROL REGISTER
003Dh	SYNC COUNTER CONTROL REGISTER
003Eh	EWPCC DAC REGISTER
003Fh	Reserved
0040h	SPI DATA I/O REGISTER
0041h	Reserved
0042h	SPI CONTROL REGISTER
0043h	SPI STATUS REGISTER
0044h	MISCELLANEOUS REGISTER
0045h	PORT B CONFIGURATION REGISTER
0046h	PROGRAMMABLE INPUT/OUTPUT CONFIGURATION REGISTER
0047h	Reserved
0048h	Reserved
0049h	Reserved

4.5 ST72E71,T71 EPROM/OTP DESCRIPTION

The ST72E71 is the EPROM version of the ST7271 ROM product. The ST72T71 OTP has the same characteristics. Both include EPROM memory instead of the ROM memory of the ST7271, and so the program and constants of the program can be easily modified by the user with the ST72E71 EPROM Programming Board from SGS-THOMSON.

From a user point of view the products have exactly the same software and hardware features of the ROM version. An additional mode is used to configure the part for programming of the EPROM, this is set by a +12.5V voltage applied to the TEST/V_{PP} pin. The programming is described in the User Manual of the EPROM Programming board.

Other than this additional mode, the ST72E71,T71 parts are fully compatible with the ROM ST7271 equivalent, this datasheet thus provides only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST7271 ROM-BASED DEVICE FOR FURTHER DETAILS.

4.5.1 EPROM ERASING

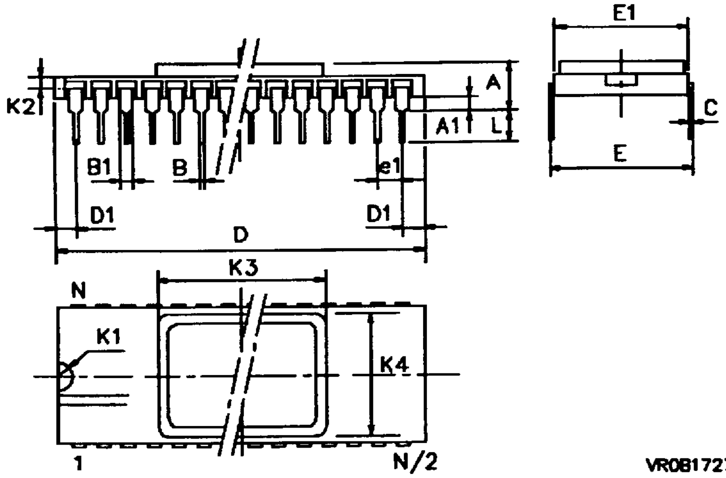
The EPROM of the windowed package of the ST72E71 may be erased by exposure to Ultra Violet light.

The erasure characteristic of the ST72E71 EPROM is such that erasure begins when the memory is exposed to light with wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range3000-4000Å. It is thus recommended that the window of the ST72E71 package be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the ST72E71 EPROM is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST72E71 should be placed within 2.5 cm (1 inch) of the lamp tubes during erasure.

4.6 PACKAGE MECHANICAL DATA

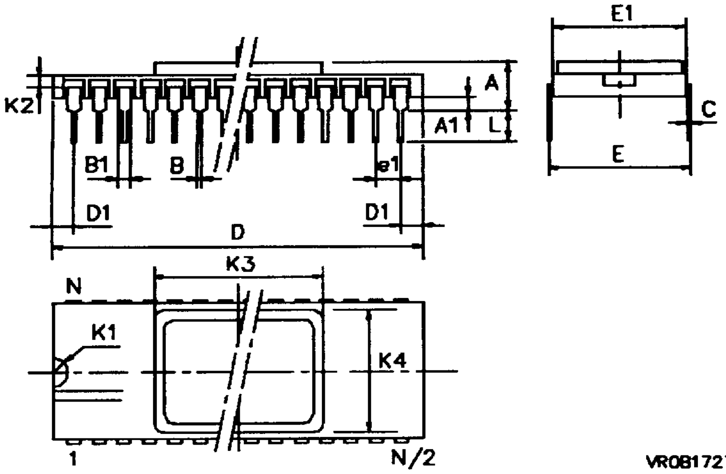
56-Pin Ceramic Shrink Dual-In-line Package, 600 Mil Width with Window



VR0B1727

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D						
D1	–	–	–	–	–	–
E	15.2 BSD			0.600 BSD		
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

42-Pin Ceramic Shrink Dual-In-line Package, 600 Mil Width with Window



VR0B1727

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D	36.32		39.12	1.430		1.540
D1	–	–	–	–	–	–
E	15.2 BSD			0.600 BSD		
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	.100		0.150
e1		1.78			0.070	
Number of Pins						
N	42					

ST72E71/T71 MICROCONTROLLER OPTION LIST

Customer ....
Address: ....
Contact: ....
Phone No: ....
Reference: ....

SGS-THOMSON Microelectronics references

Device:	EPROM	OTP
SDIP56	[ ] ST72E71N5	[ ] ST72T71N5
SDIP42	[ ] ST72E71J1	[ ] ST72T71J1

Temperature Range [ ] 0 to 70°C

OPTION LIST:

Watchdog State After Reset	[ ] Enable	[ ] Disable
Watchdog during WAIT mode	[ ] Active	[ ] Suspend
Input Clock to SPI (8MHz osc)	[ ] 2MHz	[ ] 4MHz

Signature ....

Date ....

4.7 ORDERING INFORMATION

Ordering Information Table

Sales Type	EPROM (Bytes)	OTP ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Temperature Range	Package
ST727E1N5D1 ST727E1J1D1	16K 8K		256 192	512 384	-0 to + 70°C	CSDIP56W CSDIP42W
ST72T71N5B1 ST72T71J1B1		16K 8K	256 192	512 384	-0 to + 70°C	PSDIP56 PSDIP42