P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a, e]
- 20	0.041 at V_{GS} = - 4.5 V	- 7.1
	0.055 at V_{GS} = - 2.5 V	- 6.1

FEATURES

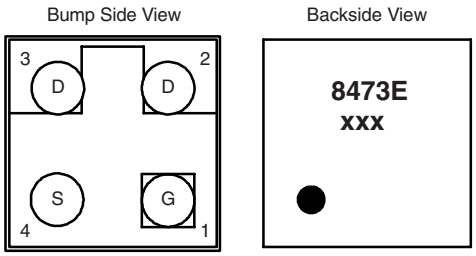
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Typical ESD Protection: 3000 V
- Gate-Source OVP
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

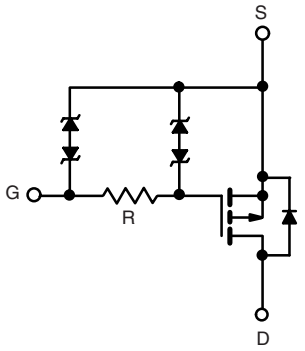
- Load Switch
- Battery Switch
- Charger Switch
- Gate-Source Over Voltage Protection (see page 3)

MICRO FOOT®



Device Marking: 8473E
xxx = Date/Lot Traceability Code

Ordering Information: Si8473EDB-T1-E1 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	- 7.1[a]	A
	T_A = 70 °C		- 5.7[a]	
	T_A = 25 °C		- 4.5[b]	
	T_A = 70 °C		- 3.6[b]	
Pulsed Drain Current		I_{DM}	- 25	
Continuous Source-Drain Diode Current	T_A = 25 °C	I_S	- 2.3[a]	
	T_A = 25 °C		- 0.92[b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	2.7[a]	W
	T_A = 70 °C		1.8[a]	
	T_A = 25 °C		1.1[b]	
	T_A = 70 °C		0.73[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions[c]	VPR		260	
	IR/Convection		260	

Notes:
a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on T_A = 25 °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	t = 5 s	R_{thJA}	35	45	°C/W
Maximum Junction-to-Ambient[c, d]	t = 5 s	R_{thJA}	85	110	

Notes:
a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Maximum under steady state conditions is 85 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
d. Maximum under steady state conditions is 175 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

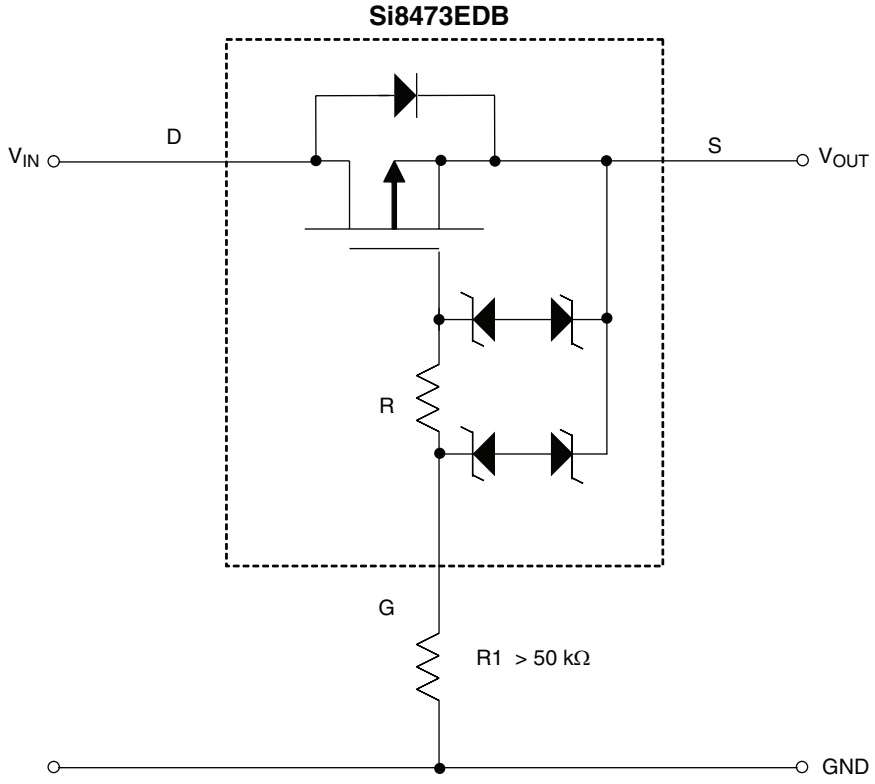
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 14		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.6		- 1.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V			± 5	µA
		V_{DS} = 0 V, V_{GS} = ± 12 V			± 1	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 70 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.034	0.041	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.046	0.055	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		11		S
Dynamic[b]						
Gate Resistance	R_g	V_{GS} = - 0.1 V, f = 1 MHz		3.6		kΩ
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		15	25	µs
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			55	85	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 1 Ω		7	15	
Rise Time	t_r			18	30	
Turn-Off Delay Time	$t_{d(off)}$			155	235	
Fall Time	t_f			110	165	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_A = 25 °C			- 2.3[c]	A
Pulse Diode Forward Current	I_{SM}				- 25	
Body Diode Voltage	V_{SD}	I_S = - 1 A, V_{GS} = 0 V		- 0.85	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 1 A, dI/dt = 100 A/µs, T_J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	35	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			17		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.

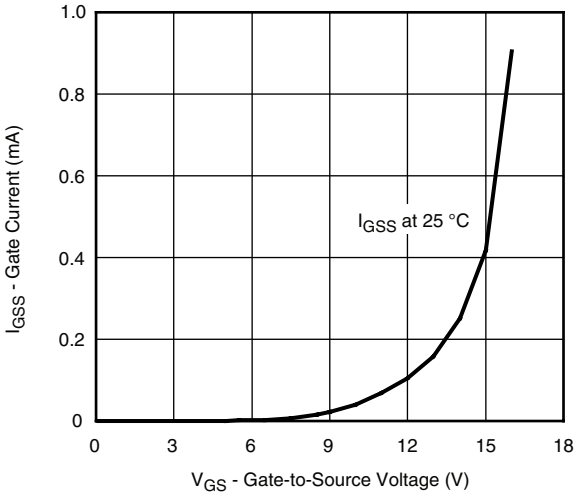
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

APPLICATION CIRCUIT EXAMPLE

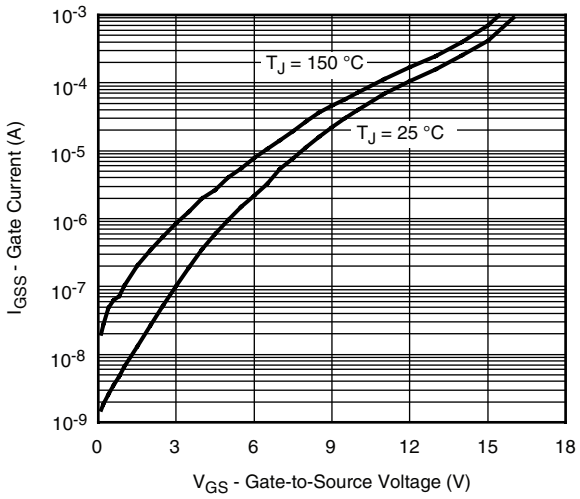
Gate-Source protection from Over-Voltage in Reverse Polarity Protection Circuit



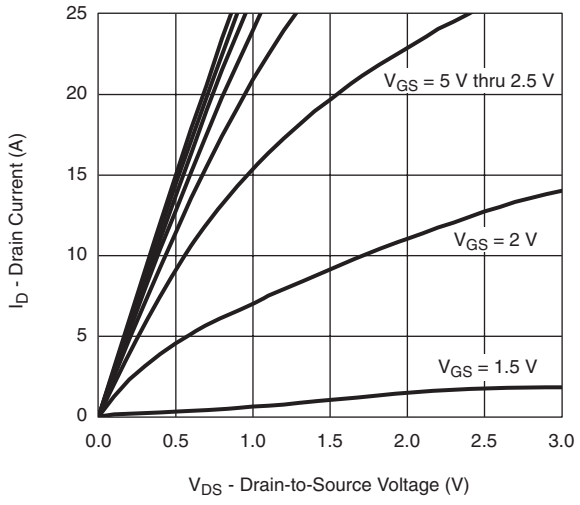
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



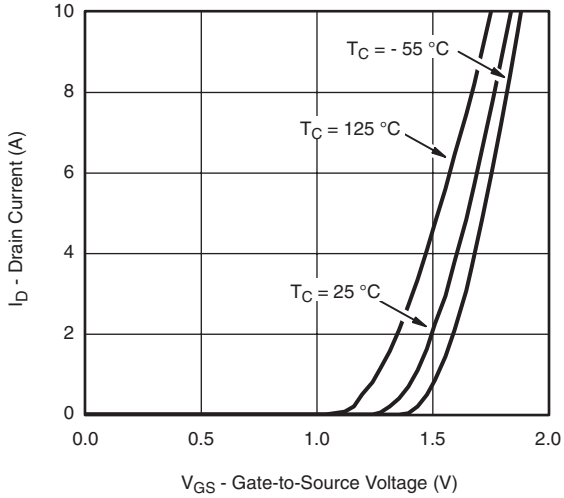
Gate Current vs. Gate-Source Voltage



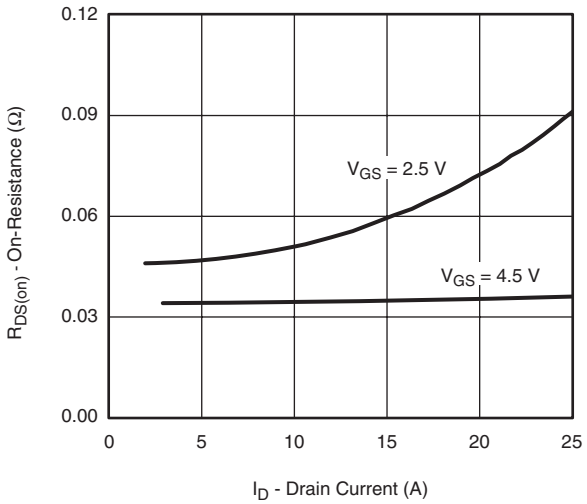
Gate Current vs. Gate-Source Voltage



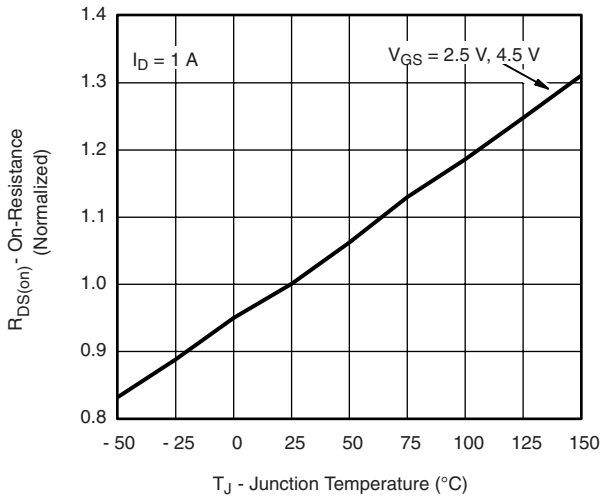
Output Characteristics



Transfer Characteristics

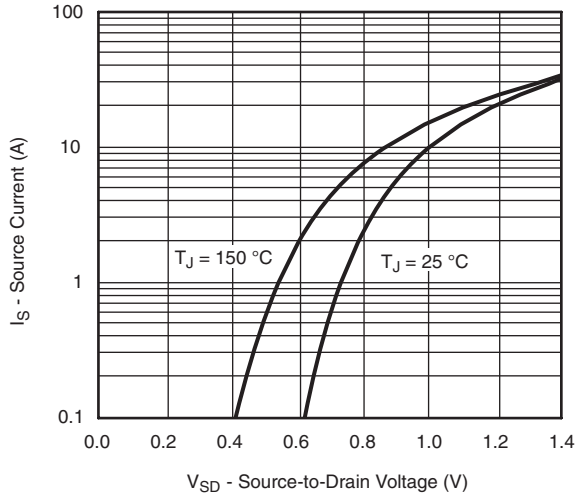


On-Resistance vs. Drain Current

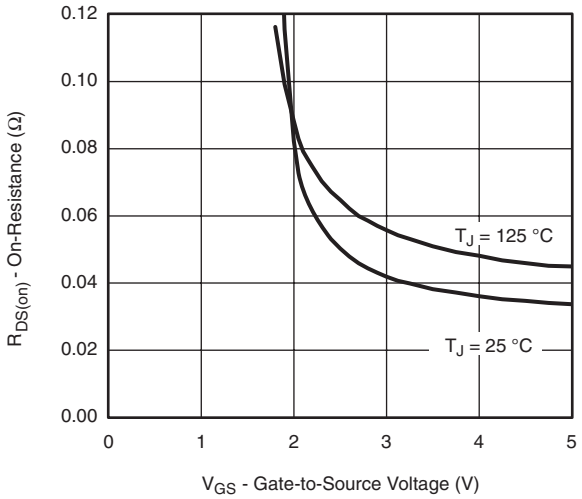


On-Resistance vs. Junction Temperature

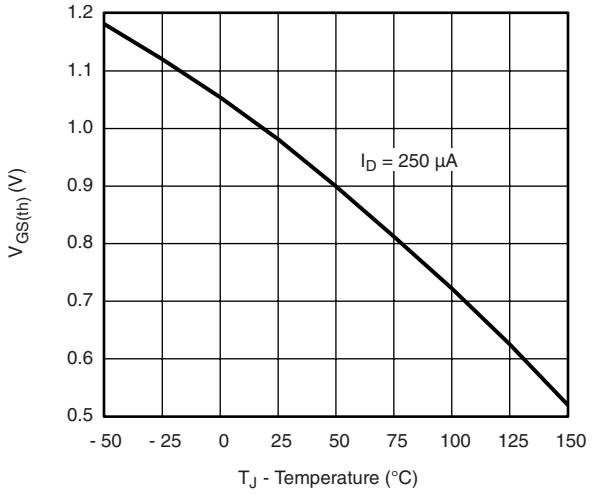
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



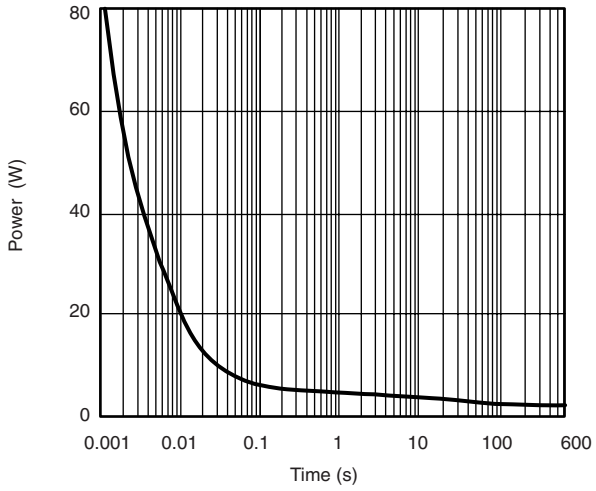
Source-Drain Diode Forward Voltage



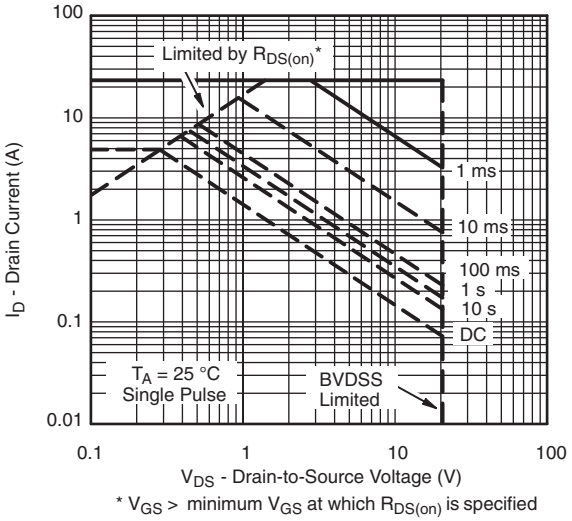
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



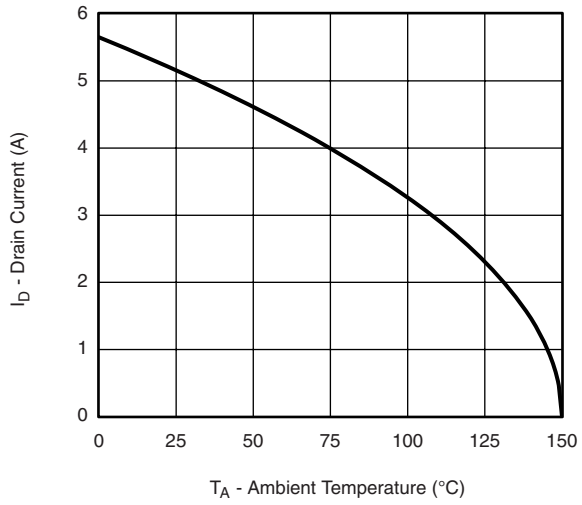
Single Pulse Power, Junction-to-Ambient



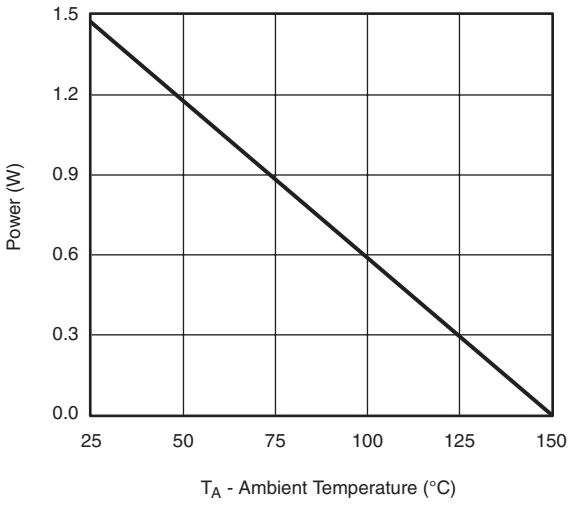
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*

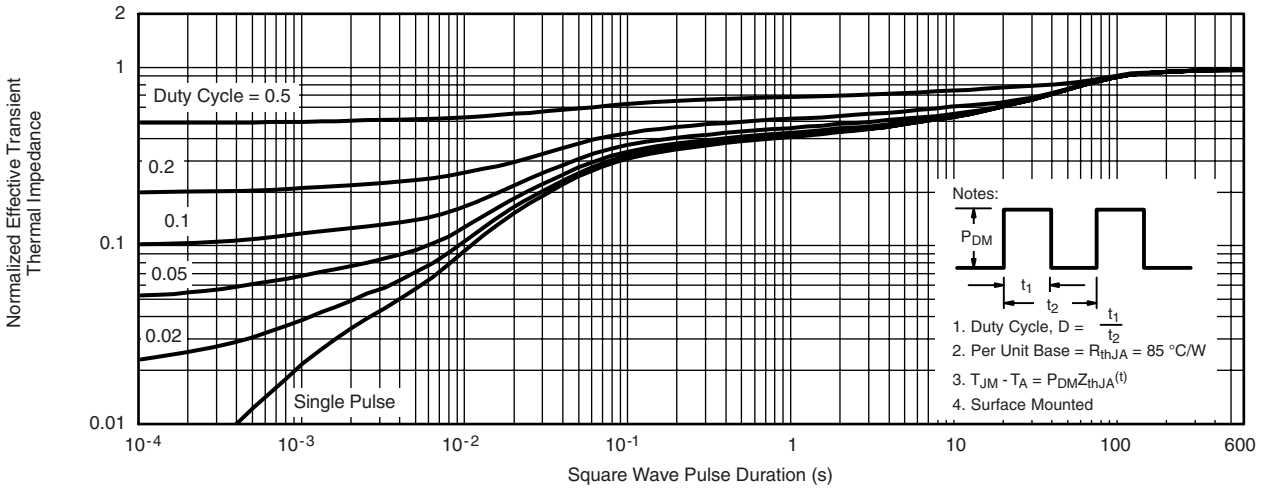


Power Derating

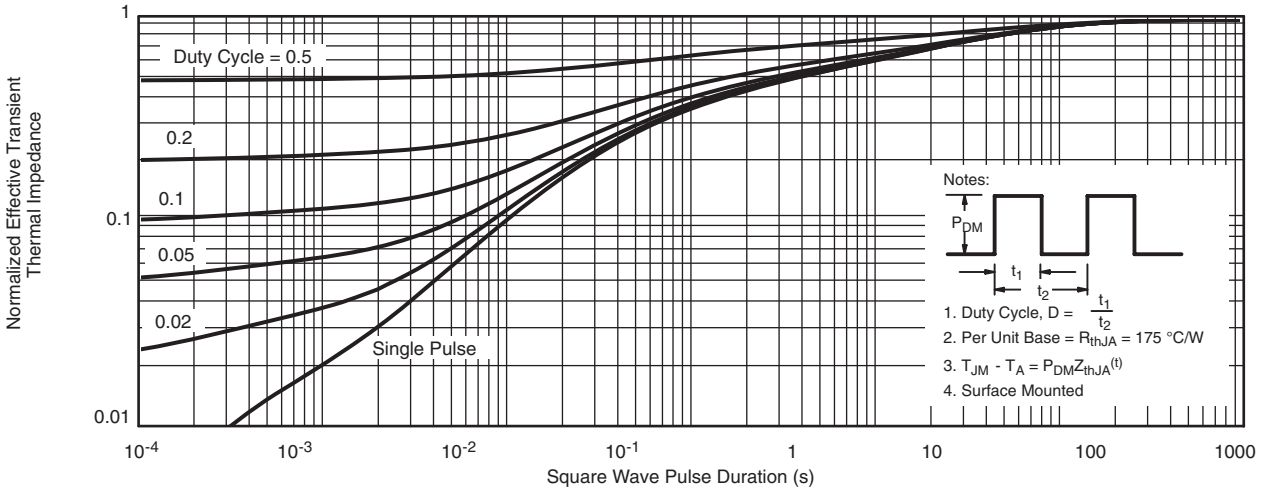
Notes:
When Mounted on 1" x 1" FR4 with full Copper.

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



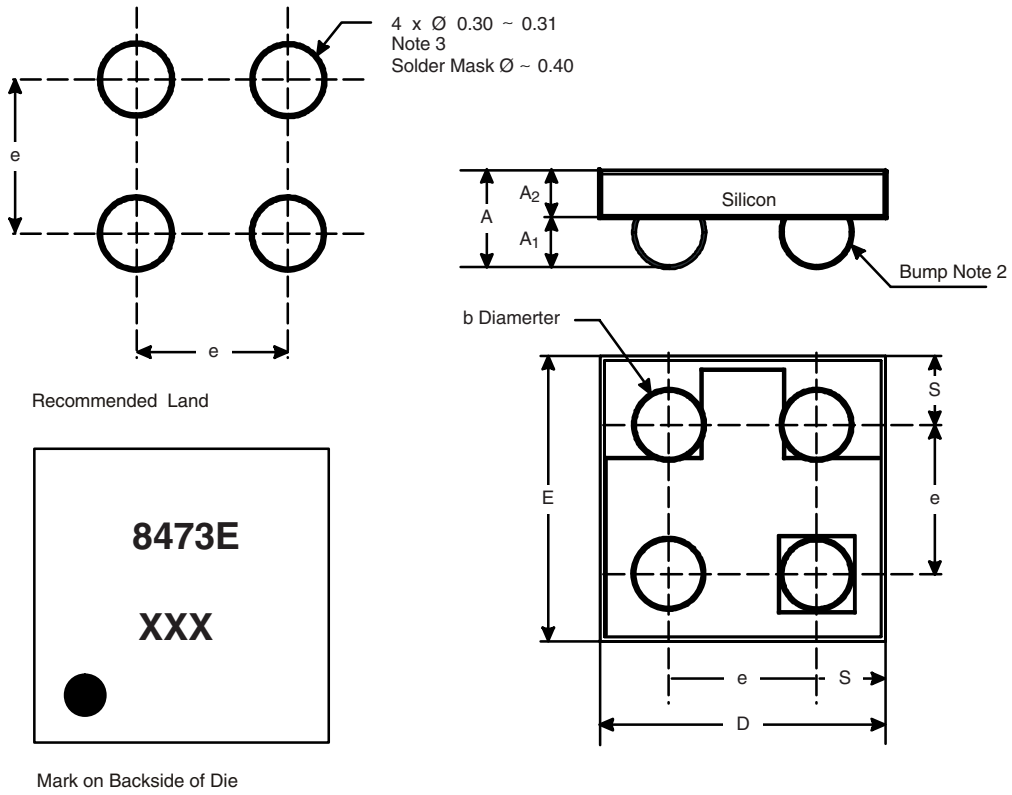
Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.8 mm PITCH)



Notes (Unless otherwise specified):
1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Eutectic solder 63/57 Sn/Pb.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters[a]		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.0102	0.0114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

Notes:
a. Use millimeters as the primary measurement.

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