5V PRECISION DATA ACQUISITION SUBSYSTEMS

FEATURES

- **Precision (up to 17 Bits) A/D Converter**
- **3 Wire Serial Port**
- **Flexible: User Can Trade-Off Conversion Speed Against Resolution**
- **Single Supply Operation**
- **–5V Output Pin**
- **4 Input, Differential Analog MUX (TC534)**
- **Automatic Input Polarity and Overrange Detection**
- **Low Operating Current ..... 5mA Max**
- **Wide Analog Input Range ..... ±4.2V Max**
- **Cost Effective**

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC530COI	28-Pin SOIC	0°C to +70°C
TC530CPJ	28-Pin Plastic DIP (300 Mil.)	0°C to +70°C
TC534CKW	44-Pin PQFP	0°C to +70°C
TC534CPL	40-Pin Plastic DIP	0°C to +70°C
TC530EV	***Evaluation Kit for TC530/534***	

GENERAL DESCRIPTION

The TC530/534 are serial analog data acquisition subsystems ideal for high precision measurements (up to 17 bits plus sign). The TC530 consists of a dual slope integrating A/D converter, negative power supply generator and 3 wire serial interface port. The TC534 is identical to the TC530, but adds a four channel differential input multiplexer. Key A/D converter operating parameters (Auto Zero and Integration time) are programmable, allowing the user to trade-off conversion time for resolution.

Data conversion is initiated when the RESET input is brought low. After conversion, data is loaded into the output shift register and $\overline{EOC}$ is asserted indicating new data is available. The converted data (plus Overrange and polarity bits) is held in the output shift register until read by the processor, or until the next conversion is completed allowing the user to access data at any time.

The TC530/534 timebase can be derived from an external crystal of 2MHz (max), or from an external frequency source. The TC530/534 requires a single 5V power supply and features a – 5V, 10mA output which can be used to supply negative bias to other components in the system.

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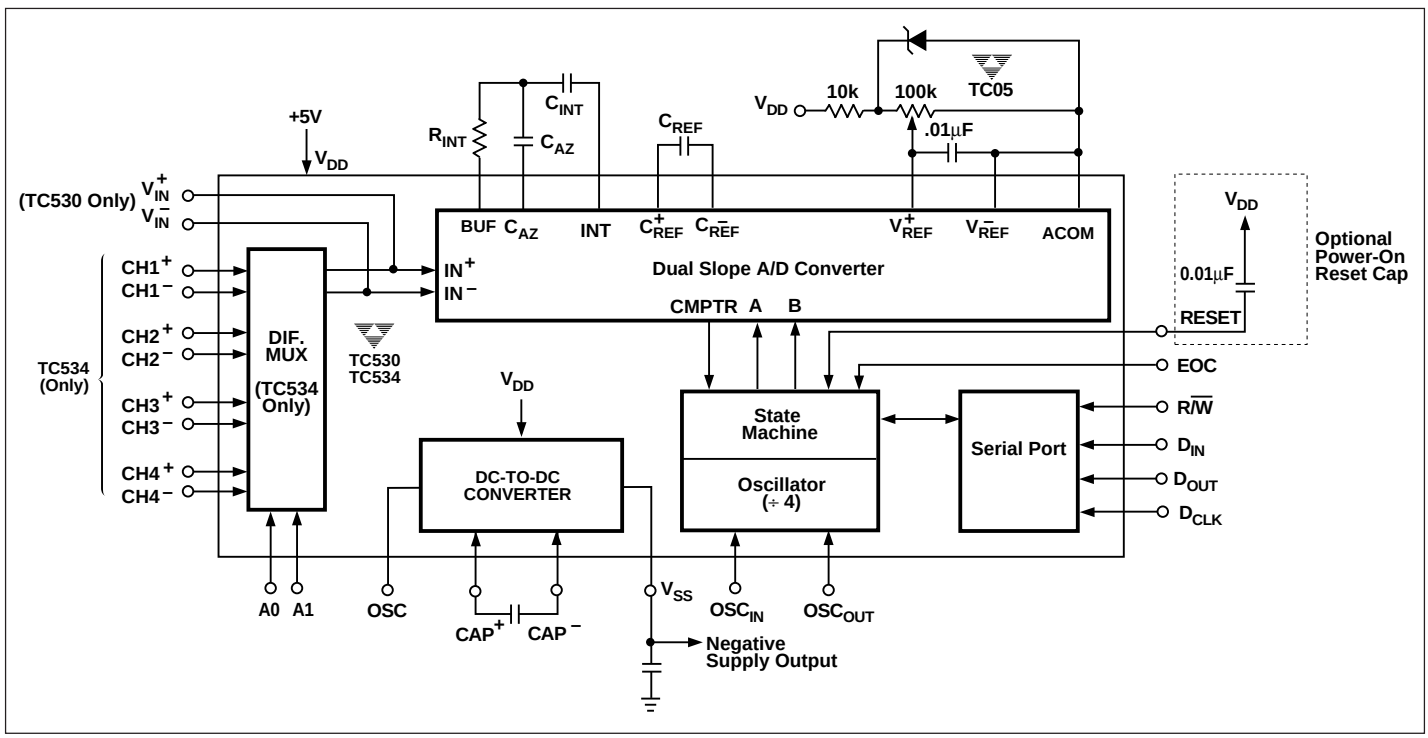
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +6V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) ..... V_{DD} to V_{SS}
Logic Input Voltage ..... (V_{DD} + 0.3V) to (GND – 0.3V)
Ambient Operating Temperature Range
Plastic DIP Package ..... (C)
0°C to +70°C
SOIC Package (C) ..... 0°C to +70°C
PQFP Package (C) ..... 0°C to +70°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{DD}	Analog Power Supply Voltage		4.5	5.0	5.5	4.5	—	5.5	V
V_{CCD}	Digital Power Supply Voltage		4.5	5.0	5.5	4.5	—	5.5	V
P_D	TC530/534 Total Power Dissipation	V_{DD} = V_{CCD} = 5V	—	—	25	—	—	—	mW
I_S	Supply Current (V_S + P_{IN})		—	1.8	2.5	—	—	3.0	mA
I_{CCD}	Supply Current (V_{CCD} P_{IN})	f_{OSC} = 1MHz	—	—	1.5	—	—	1.7	mA

ELECTRICAL CHARACTERISTICS: V_{DD} = V_{CCD}, C_{AZ} = C_{REF} = 0.47µF, unless otherwise specified.

			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Analog									
R	Resolution	Note 1	—	—	±17	—	—	±17	Bits
ZSE	Zero-Scale Error with Auto Zero Phase		—	—	0.5	—	0.005	0.012	% F.S.
ENL	End Point Linearity	Note 1 and 2	—	0.015	0.030	—	0.015	0.045	% F.S.
NL	Max Deviation from Best Straight Line Fit	Notes 1 and 2	—	0.008	0.015	—	—	—	% F.S.
ZS_{TC}	Zero-Scale Temperature Coefficient		—	—	—	—	1	2	µV/°C
SYE	Roll-Over Error	Note 3	—	.012	—	—	.03	—	% F.S.
FS_{TC}	Full-Scale Temperature Coefficient	Ext. V_{REF} TC = 0ppm/°C	—	—	—	—	10	—	ppm/°C
I_{IN}	Input Current	V_{IN} = 0V	—	6	—	—	—	—	pA
V_{CMR}	Common-Mode Voltage Range		V_{SS} + 1.5	—	V_{DD} – 1.5	V_{SS} + 1.5	—	V_{DD} – 1.5	V
V_{INT}	Integrator Output Swing		V_{SS} + 0.9	—	V_{DD} – 0.9	V_{SS} + 0.9	—	V_{DD} – 0.9	V
V_{IN}	Analog Input Signal Range		V_{SS} + 1.5	—	V_{DD} – 1.5	V_{SS} + 1.5	—	V_{DD} – 1.5	V
V_{REF}	Voltage Reference Range		V_{SS} + 1	—	V_{DD} – 1	V_{DD} + 1	—	V_{DD} – 1	V
t_D	Zero Crossing Comparator		—	2.0	—	—	3.0	—	µsec

ELECTRICAL CHARACTERISTICS:

Serial Port Interface: V_{CCD} = +5V, unless otherwise specified.

			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Input Logic HIGH Level		2.5	—	—	2.5	—	—	V
V_{IL}	Input Logic LOW Level		—	—	0.8	—	—	0.8	V
I_{IN}	Input Current (DI, DO, D_{CLK})		—	—	10	—	—	—	µA
V_{OL}	Logic LOW Output Voltage ($\overline{EOC}$)	I_{OUT} = 250µA	—	0.2	0.3	—	—	0.35	V

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ELECTRICAL CHARACTERISTICS:

Serial Port Interface: V_{CCD} = +5V, unless otherwise specified.

			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
tR, tF	Rise and Fall Times ($\overline{EOC}$, DI, DO)	C_L = 10pF	—	—	250	—	250	—	nsec
F_{XTL}	Crystal Frequency		—	—	2.0	—	—	2.0	MHz
F_{EXT}	External Frequency on OSC_{IN}		—	—	4.0	—	—	4.0	MHz
t_{RS}	Read Setup Time		1	—	—	—	1	—	µsec
t_{RD}	Read Delay Time		250	—	—	—	250	—	nsec
t_{DRS}	D_{CLK} to D_{OUT} Delay		450	—	—	—	450	—	nsec
t_{PWL}	D_{CLK} LOW Pulse Width		150	—	—	—	150	—	nsec
t_{PWH}	D_{CLK} HIGH Pulse Width		150	—	—	—	150	—	nsec
t_{DR}	Data Ready Delay		200	—	—	—	200	—	nsec

ELECTRICAL CHARACTERISTICS:

DC/DC Converter Section: V_{DD} = +5V, unless otherwise specified.

			T_A = +25°C			T_A = 0°C To +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
R_{OUT}	Output Resistance	I_{OUT} = 10mA	—	65	85	—	—	100	Ω
f_{CLK}	Oscillator Frequency	C_{OSC} = 0	—	100	—	—	—	—	kHz
I_{OUT}	V_{SS} Output Current		—	—	10	—	—	10	mA

ELECTRICAL CHARACTERISTICS:

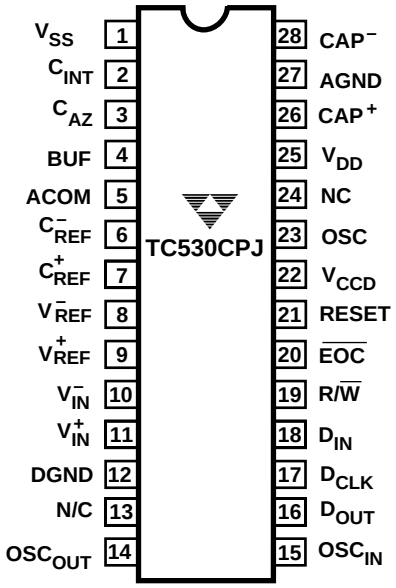
Multiplexer: V_{DD} = +5V (Note 4), unless otherwise specified.

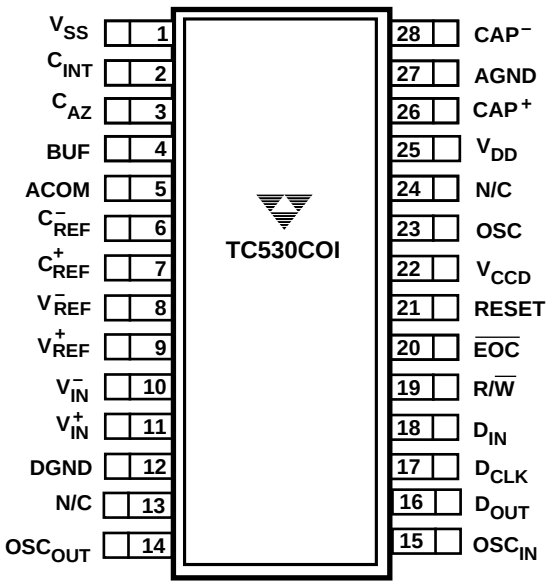
			T_A = +25°C			T_A = 0°C to +70°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{INMAX}	Maximum Input Voltage		– 2.5	—	2.5	–2.5	—	2.5	V
R_{DSON}	Drain/Source ON Resistance		—	6	10	—	—	—	kΩ

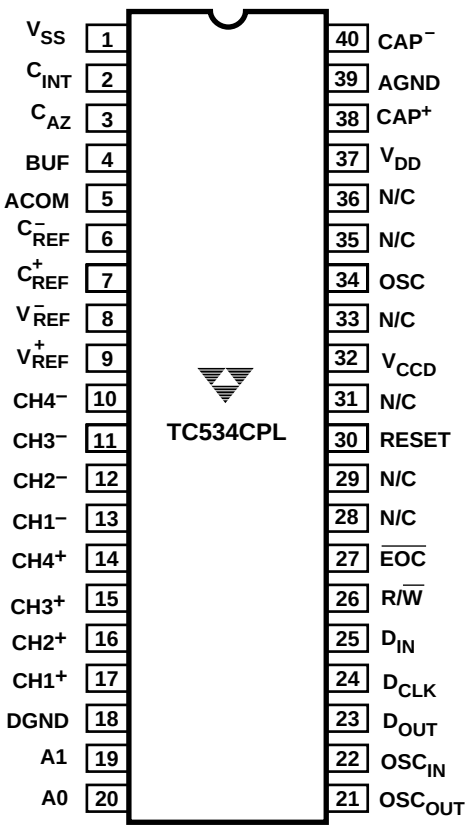
Notes:
1. Integrate time ≥ 66msec, Auto Zero time ≥ 66msec, V_{INT} (pk) = 4V.
2. End point linearity at ±¼, ±½, ±¾ F.S. after full scale adjustment.
3. Roll-over error is related to capacitor used for C_{INT} (See "Recommended Suppliers for C_{INT}", Table 2).
4. TC534 Only.

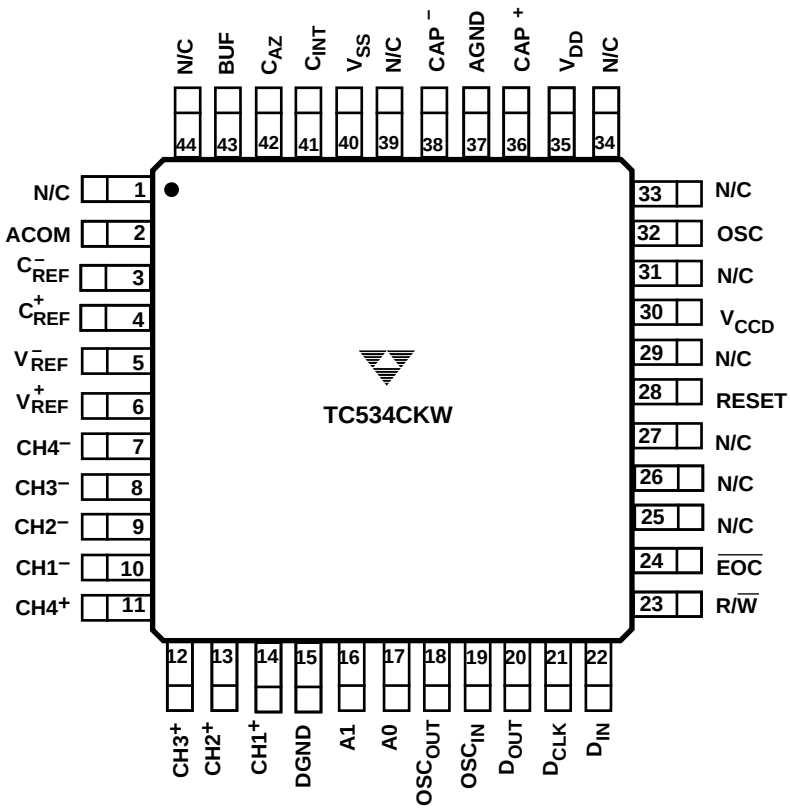
TC530
TC534

PIN CONFIGURATIONS









PIN DESCRIPTION

Pin No. (TC530 28-Pin PDIP, 300 Mil.)	Pin No. (TC530 28-Pin SOIC)	Pin No (TC534 40-Pin PDIP)	Pin No. (TC534 44-Pin PQFP)	Symbol	Description
1	1	1	40	V_{SS}	Analog Output. Negative power supply converter output and reservoir capacitor connection. This output can be used to provide negative bias to other devices in the system.
2	2	2	41	C_{INT}	Analog Output. Integrator capacitor connection and integrator output.
3	3	3	42	C_{AZ}	Analog Input. Auto Zero capacitor connection.
4	4	4	43	BUF	Analog Output. Integrator capacitor connection and voltage buffer output.
5	5	5	2	ACOM	Analog Input. This pin is ground for all of the analog switches in the A/D converter. It is grounded for most applications. ACOM and the input common pin (V_{IN}^- or Chx^-) should be within the common mode range, CMR.
6	6	6	3	C_{REF}^-	Analog Input. Reference cap negative connection.
7	7	7	4	C_{REF}^+	Analog Input. Reference cap positive connection.
8	8	8	5	V_{REF}^-	Analog Input. External voltage reference negative connection.
9	9	9	6	V_{REF}^+	Analog Input. External voltage reference positive connection.
Not Used	Not Used	10	7	$CH4^-$	Analog Input. Multiplexer channel 4 negative differential analog input.
Not Used	Not Used	11	8	$CH3^-$	Analog Input. Multiplexer channel 3 negative differential analog input.
Not Used	Not Used	12	9	$CH2^-$	Analog Input. Multiplexer channel 2 negative differential analog input.
Not Used	Not Used	13	10	$CH1^-$	Analog Input. Multiplexer channel 1 negative differential analog input.
Not Used	Not Used	14	11	$CH4^+$	Analog Input. Multiplexer channel 4 positive differential analog input.
Not Used	Not Used	15	12	$CH3^+$	Analog Input. Multiplexer channel 3 positive differential analog input.
Not Used	Not Used	16	13	$CH2^+$	Analog Input. Multiplexer channel 2 positive differential analog input.
Not Used	Not Used	17	14	$CH1^+$	Analog Input. Multiplexer channel 1 positive differential analog input.
10	10	Not Used	Not Used	V_{IN}^-	Analog Input. Negative differential analog voltage input.
11	11	Not Used	Not Used	V_{IN}^+	Analog Input. Positive differential analog voltage input.
12	12	18	15	DGND	Analog Input. Ground connection for serial port circuit.
Not Used	Not Used	19	16	A1	Logic Level Input. Multiplexer address MSB.
Not Used	Not Used	20	17	A0	Logic Level Input. Multiplexer address LSB.
14	14	21	18	OSC_{OUT}	Analog Input. Timebase for state machine. This pin connects to one side of an AT-cut crystal having an effective series resistance of 100Ω (typ) and a parallel capacitance of 20pF If an external frequency source is used to clock the TC530/534, this pin must be left floating.

PIN DESCRIPTION (Cont.)

Pin No. (TC530 28-Pin PDIP, 300 Mil.)	Pin No. (TC530 28-Pin SOIC)	Pin No (TC534 40-Pin PDIP)	Pin No. (TC534 44-Pin PQFP)	Symbol	Description
15	15	22	19	OSC_{IN}	Analog Input. This pin connects to the other side of the crystal described in OSC_{OUT} above. The TC530/534 may also be clocked from an external frequency source connected to this pin. The external frequency source must be a pulse wave form with a minimum 30% duty cycle and rise and fall times 15nsec (Max). If an external frequency source is used, OSC_{OUT} must be left floating. A maximum operating frequency of 2MHz (crystal) or 4MHz (external clock source) is permitted.
16	16	23	20	D_{OUT}	Logic Level Output. Serial port data output pin. This pin is enabled only when R/$\overline{W}$ is high.
17	17	24	21	D_{CLK}	Logic Input, Positive and Negative Edge Triggered. Serial port clock. When R/$\overline{W}$ is high, serial data is clocked out of the TC530/534A (on D_{OUT}) at each HIGH-to-LOW transition of D_{CLK}. A/D initialization data (LOAD VALUE) is clocked into the TC530/534 (on D_{IN}) at each LOW-to-HIGH transition of D_{CLK}. A maximum serial port D_{CLK} frequency of 3MHz is permitted.
18	18	25	22	D_{IN}	Logic Level Input. Serial port input pin. The A/D converter integration time (T_{INT}) and Auto Zero time (T_{AZ}) values are determined by the LOAD VALUE byte clocked into this pin. This initialization must take place at power up, and can be rewritten (or modified and rewritten) at any time. The LOAD VALUE is clocked into D_{IN} MSB first.
19	19	26	23	R/$\overline{W}$	Logic Level Input. This pin must be brought low to perform a write to the serial port (e.g. initialize the A/D converter). The D_{OUT} pin of the serial port is enabled only when this pin is high.
20	20	27	24	$\overline{EOC}$	Open Drain Output. End-of-Conversion ($\overline{EOC}$) is asserted any time the TC530/534 is in the AZ phase of conversion. This occurs when either the TC530/534 initiates a normal AZ phase, or when RESET is pulled high. $\overline{EOC}$ is returned high when the TC530/534 exits AZ. Since $\overline{EOC}$ is driven low immediately following completion of a conversion cycle, it can be used as a DATA READY processor interrupt.
21	21	30	28	RESET	Logic Level Input. It is necessary to force the TC530/534 into the Auto Zero phase when power is initially applied. This is accomplished by momentarily taking RESET high. Using an I/O port line from the microprocessor, or by applying an external system reset signal, or by connecting a 0.01µF capacitor from the RESET input to V_{SS}. Conversions are performed continuously as long as RESET is low and conversion is halted when RESET is high. RESET may therefore be used in a complex system to momentarily suspend conversion (for example while the address lines of an input multiplexer are changing state). In this case, RESET should be pulled high only when the $\overline{EOC}$ is LOW to avoid excessively long integrator discharge times which could result in erroneous conversion (see *Applications* Section).

PIN DESCRIPTION (Cont.)

Pin No. (TC530 28-Pin PDIP, 300 Mil.)	Pin No. (TC530 28-Pin SOIC)	Pin No (TC534 40-Pin PDIP)	Pin No. (TC534 44-Pin PQFP)	Symbol	Description
22	22	32	30	V_{CCD}	Analog Input. Power supply connection for digital logic and serial port. Proper power-up sequencing is critical, see the *Applications* section.
23	23	34	32	OSC	Input. The negative power supply converter normally runs at a frequency of 100kHz. This frequency can be slowed down to reduce quiescent current by connecting an external capacitor between this pin and V_S^+. (See *Typical Characteristics*).
25	25	37	35	V_{DD}	Analog Input. Power supply connection for the A/D analog section and DC-DC converter. Proper power-up sequencing is critical, see the *Applications* section.
26	26	38	36	CAP^+	Analog Input. Storage capacitor positive connection for the DC/DC converter.
27	27	39	37	AGND	Analog Input. Ground connection for DC/DC converter.
28	28	40	38	CAP^-	Analog Input. Storage capacitor negative connection for the DC/DC converter.
13, 24	13, 24	28, 29, 31, 33, 35, 36	1, 25, 26, 27 29, 31, 33, 34, 39, 44,	NC	No connect. Do not connect any signal to these pins.

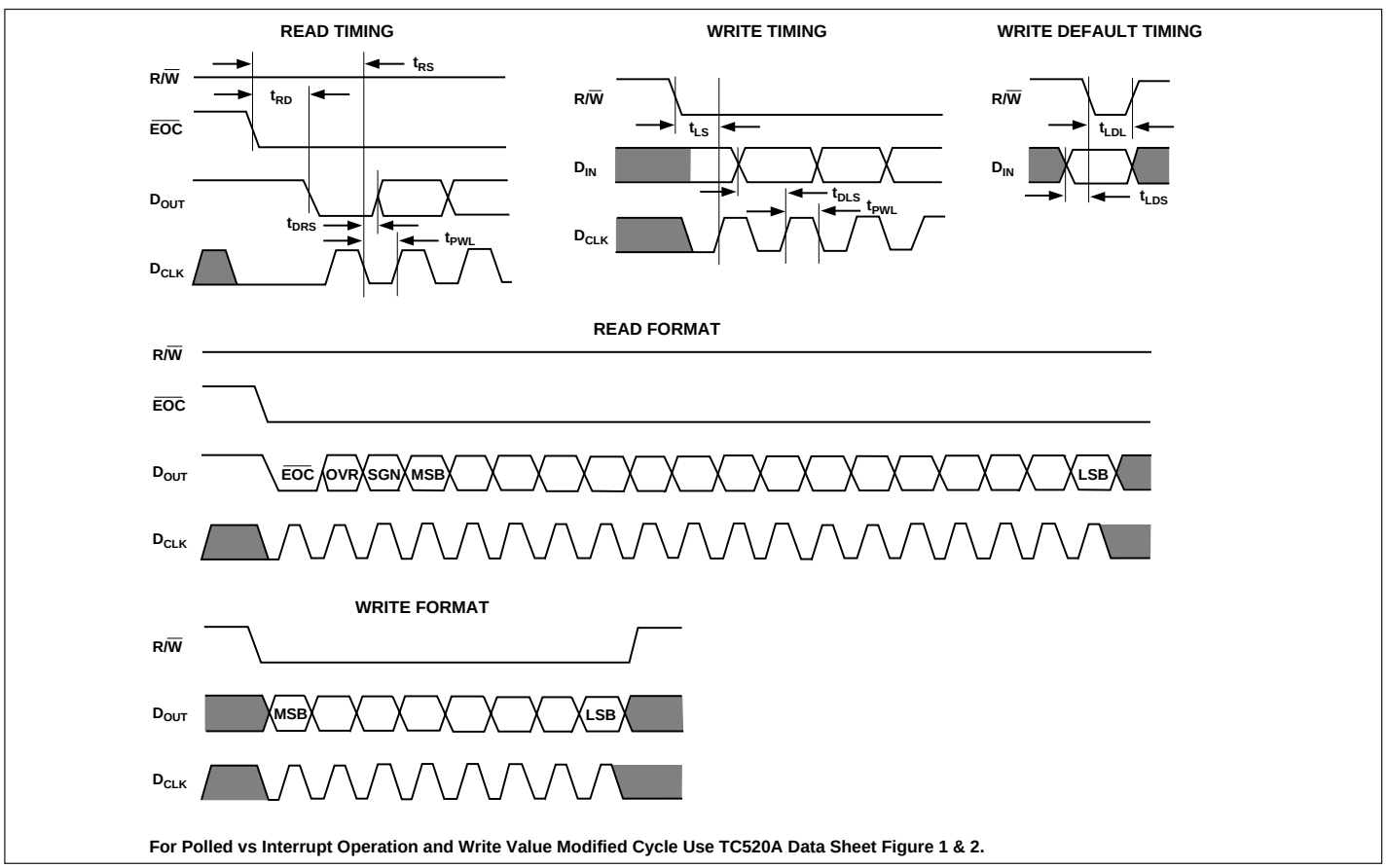


Figure 1. Serial Port Timing

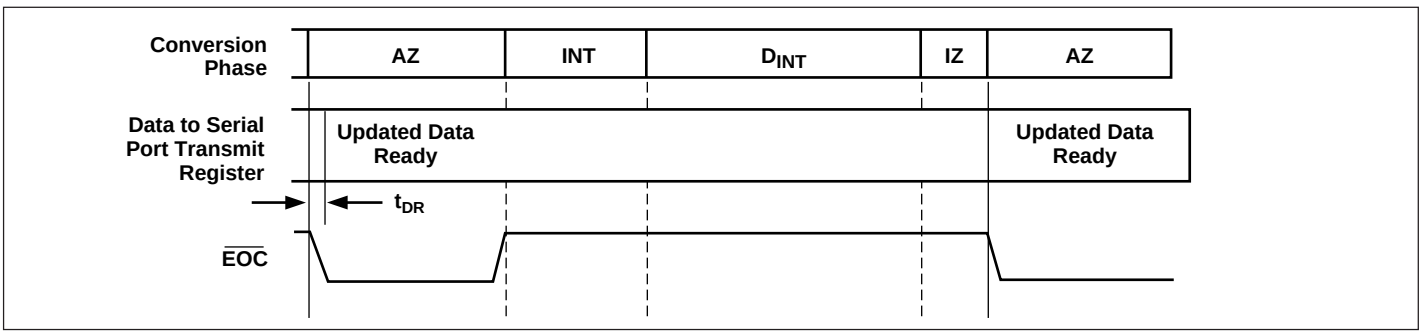


Figure 2. A/D Converter Timing

DETAILED DESCRIPTION

Dual Slope Integrating Converter

The TC530/534 dual slope converter operates by integrating the input signal for a fixed time period, then applying an opposite polarity reference voltage while timing the period (counting clocks pulses) for the integrator output to cross 0V (deintegrating). The resulting count is read as conversion data.

A simple mathematical expression that describes dual slope conversion is:

(1) Integrate Voltage = Deintegrate Voltage

$$(2)\quad 1/R_{INT}C_{INT}\int_0^{t_{INT}} V_{IN}(t)dt = 1/R_{INT}C_{INT}\int_0^{t_{DINT}} V_{REF}$$

from which:

$$(3)\quad (V_{IN})\left[\frac{(t_{INT})}{(R_{INT})(C_{INT})}\right] = (V_{REF})\left[\frac{(t_{DINT})}{(R_{INT})(C_{INT})}\right]$$

and therefore:

$$(4)\quad V_{IN} = V_{REF}\left[\frac{t_{DINT}}{t_{INT}}\right]$$

where: V_{REF} = Reference Voltage
t_{INT} = Integrate Time
t_{DINT} = Reference Voltage Deintegrate Time

Inspection of equation (4) shows dual slope converter accuracy is unrelated to integrating resistor and capacitor values, as long as they are stable throughout the measurement cycle. This measurement technique is inherently ratiometric (i.e., the ratio between the t_{INT} and t_{DINT} times is equal to the ratio between V_{IN} and V_{REF}).

Another inherent benefit is noise immunity. Input noise spikes are integrated (or averaged to zero) during the integration period. The integrating converter has a noise immunity with an attenuation rate of at least –20dB per decade. Interference signals with frequencies at integral multiples of the integration period are, for the most part, completely removed. For this reason, the integration period of the converter is often established to reject 50/60Hz line noise. The ability to reject such noise is shown by the plot of Figure 3.

In addition to the two phases required for dual slope measurement (Integrate and Deintegrate), the TC530/534 performs two additional adjustments to minimize measurement error due to system offset voltages. The resulting four internal operations (conversion phases) performed each measurement cycle are: Auto Zero (AZ), Integrator Output Zero (IZ), Input Integrate (INT) and Reference Deintegrate (D_{INT}). The AZ and IZ phases compensate for system offset errors and the INT and D_{INT} phases perform the actual A/D conversion.

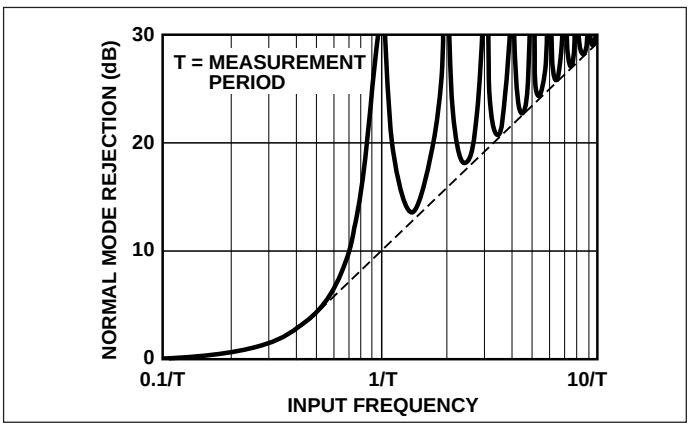


Figure 3. Integrating Converter Normal Mode Rejection

Auto Zero Phase (AZ)

This phase compensates for errors due to buffer, integrator and comparator offset voltages. During this phase, an internal feedback loop forces a compensating error voltage on auto zero capacitor (C_{AZ}). The duration of the AZ phase is programmable via the serial port (see also Programming AZ and INT Phase Duration paragraph of this document).

Input Integrate Phase (INT)

In this phase, a current directly proportional to differential input voltage is sourced into integrating capacitor C_{INT}. The amount of voltage stored on C_{INT} at the end of the INT phase is directly proportional to the applied differential input voltage. Input signal polarity (sign bit) is determined at the end of this phase. Converter resolution and conversion speed is a function of the duration of the INT phase, which is programmable by the user via the serial port (see also Programming AZ and INT Phase Duration paragraph of this document). The shorter the integration time, the faster the speed of conversion, but the lower the resolution. Conversely, the longer the integration time, the greater the resolution, but at slower the speed of conversion.

Reference Deintegrate Phase (DINT)

This phase consists of measuring the time for the integrator output to return (at a rate determined by the external reference voltage) from its initial voltage to 0V. The resulting timer data is stored in the output shift register as converted analog data.

Integrator Output Zero Phase (IZ)

This phase guarantees the integrator output is at zero volts when the AZ phase is entered so that only true system offset voltages will be compensated for.

All internal converter timing is derived from the frequency source at OSC_{IN} and OSC_{OUT}. This frequency source must be either an externally provided clock signal, or an external crystal. If an external clock is used, it must be connected to the OSC_{IN} pin and the OSC_{OUT} pin must remain floating. If a crystal is used, it must be connected between OSC_{IN} and OSC_{OUT} and physically located as close to the OSC_{IN} and OSC_{OUT} pins as possible. In either case, the incoming clock frequency is divided by four and the resulting clock serves as the internal TC530/534 timebase.

APPLICATIONS

Programming the TC530/534

AZ and INT Phase Duration:

These two phases have equal duration determined by the crystal (or external) frequency and the timer initialization byte (LOAD VALUE). Timing is selected as follows:

(1) **Select Integration Time**
Integration time must be picked as a multiple of the period of the line frequency. For example, t_{INT} times of 33msec, 66msec and 132msec maximize 60Hz line rejection.

(2) **Estimate Crystal Frequency**
Crystal frequencies as high as 2MHz are allowed. Crystal frequency is estimated using:

$$F_{IN} = \frac{2(R)}{t_{INT}}$$

where: R = Desired Converter Resolution (in counts)
F_{IN} = Input Frequency (in MHz)
INT = Integration Time (in seconds)

(3) **Calculate LOAD VALUE**

$$[\text{LOAD VALUE}]_{10} = 256 - \frac{(t_{INT})(F_{IN})}{1024}$$

F_{IN} can be adjusted to a standard value during this step. The resulting base -10 LOAD VALUE must be converted to a hexadecimal number, then loaded into the serial port prior to initiating A/D conversion.

D_{INT} and IZ Phase Timing

The duration of the D_{INT} phase is a function of the amount of voltage stored on the integrator capacitor during INT, and the value of V_{REF}. The D_{INT} phase is initiated immediately following INT and terminated when an integrator output zero-crossing is detected. In general, the maximum number of counts chosen for D_{INT} is twice that of INT (with V_{REF} chosen at V_{IN}(max)/2).

System RESET

The TC530/534 must be forced into the AZ state when power is first applied. A .01µF capacitor connected from RESET to V_{CC} (or external system reset logic signal) can be used to momentarily drive RESET high for a minimum of 100msec.

Selecting Component Values for the TC530/534

(1) **Calculate Integrating Resistor (R_{INT})**
The desired full-scale input voltage and amplifier output current capability determine the value of R_{INT}. The buffer and integrator amplifiers each have a full-scale current of 20µA.

The value of R_{INT} is therefore directly calculated as follows:

$$R_{INT}\ (M\Omega) = \frac{V_{INMAX}}{20}$$

where: V_{INMAX} = Maximum Input Voltage (full count voltage)
R_{INT} = Integrating Resistor (in MΩ)

For loop stability, R_{INT} should be ≥ 50kΩ.

(2) **Select Reference** (C_{REF}) **and Auto Zero** (C_{AZ}) **Capacitors**
C_{REF} and C_{AZ} must be low leakage capacitors (such as polypropylene). The slower the conversion rate, the larger the value C_{REF} must be. Recommended capacitors for C_{REF} and C_{AZ} are shown in Table 1. Larger values for C_{AZ} and C_{REF} may also be used to limit roll-over errors.

Table 1. C_{REF} and C_{AZ} Selection

Conversions Per Second	Typical Value of C_{REF}, C_{AZ} (μF)	Suggested * Part Number
>7	0.1	WIMA MK12 .1/63/20
2 to 7	0.22	WIMA MK12 .22/63/20
2 or less	0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

3. **Calculate Integrating Capacitor** (C_{INT})
The integrating capacitor must be selected to maximize integrator output voltage swing. The integrator output voltage swing is defined as the absolute value of V_{DD} (or V_{SS}) less 0.9V (i.e. $|V_{DD} - 0.9V|$ or $|V_{SS} + 0.9V|$). Using the 20μA buffer maximum output current, the value of the integrating capacitor is calculated using the following equation:

$$C_{INT}\ (\mu F) = \frac{(t_{INT})(20)}{(V_S - 0.9)}$$

where: t_{INT} = Integration Period
V_S = Applied Supply Voltage
C_{INT} = Integrator Capacitor Value (in μF)

It is critical that the integrating capacitor have a very low dielectric absorption. PPS capacitors are an example of one such chemistry. Table 2 summarizes various capacitors suitable for C_{INT}.

Table 2. Recommend Capacitor for C_{INT}

Value	Suggested Part Number*
0.1	WIMA MK12 .1/63/20
0.22	WIMA MK12 .22/63/20
0.33	WIMA MK12 .33/63/20
0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

4. **Calculate V_{REF}**
The reference deintegration voltage is calculated using:

$$V_{REF}\ (\text{in Volts}) = \frac{(V_S - 0.9)(C_{INT})(R_{INT})}{2(t_{INT})}$$

Serial Port

Communication with the TC530/534 is accomplished over a 3 wire serial port. Data is clocked into D_{IN} on the rising edge of D_{CLK} and clocked out of D_{OUT} on the falling edge of D_{CLK}. R/$\overline{W}$ must be HIGH to read converted data from the serial port and LOW to write the LOAD VALUE to the TC530/534.

Load Value Write Cycle (Figure 4)

Following the power-up reset pulse, the LOAD VALUE (which sets the duration of AZ and INT) must next be transmitted to the serial port. To accomplish this, the processor monitors the state of $\overline{EOC}$ (which is available as a hardware output or at D_{OUT}). R/$\overline{W}$ is taken low to initiate the write cycle only when $\overline{EOC}$ is low (during the AZ phase). (Failure to observe $\overline{EOC}$ low may cause an offset voltage to be developed across C_{INT} resulting in erroneous readings). The 8 bit LOAD VALUE data on D_{IN} is clocked in by D_{CLK}. The processor then terminates the write cycle by taking R/$\overline{W}$ high. (Data is transferred from the serial input shift register to the time base counter on the rising edge of R/$\overline{W}$, and data conversion is initiated).

Data Read Cycle (Figure 5)

Data is shifted out of the serial port in the following order: End of Conversion ($\overline{EOC}$), Overrange (OVR), Sign (SGN), conversion data (MSB first). When R/$\overline{W}$ is high, the state of the $\overline{EOC}$ bit can be polled by simply reading the state of D_{OUT}. This allows the processor to determine if new data is available without connecting an additional wire to the $\overline{EOC}$ output pin (this is especially useful in a polled environment).

Input Multiplexer (TC534 Only)

A 4 input, differential multiplexer is included in the TC534. The states of channel address lines A0 and A1 determine which differential V_{IN} pair is routed to the con-

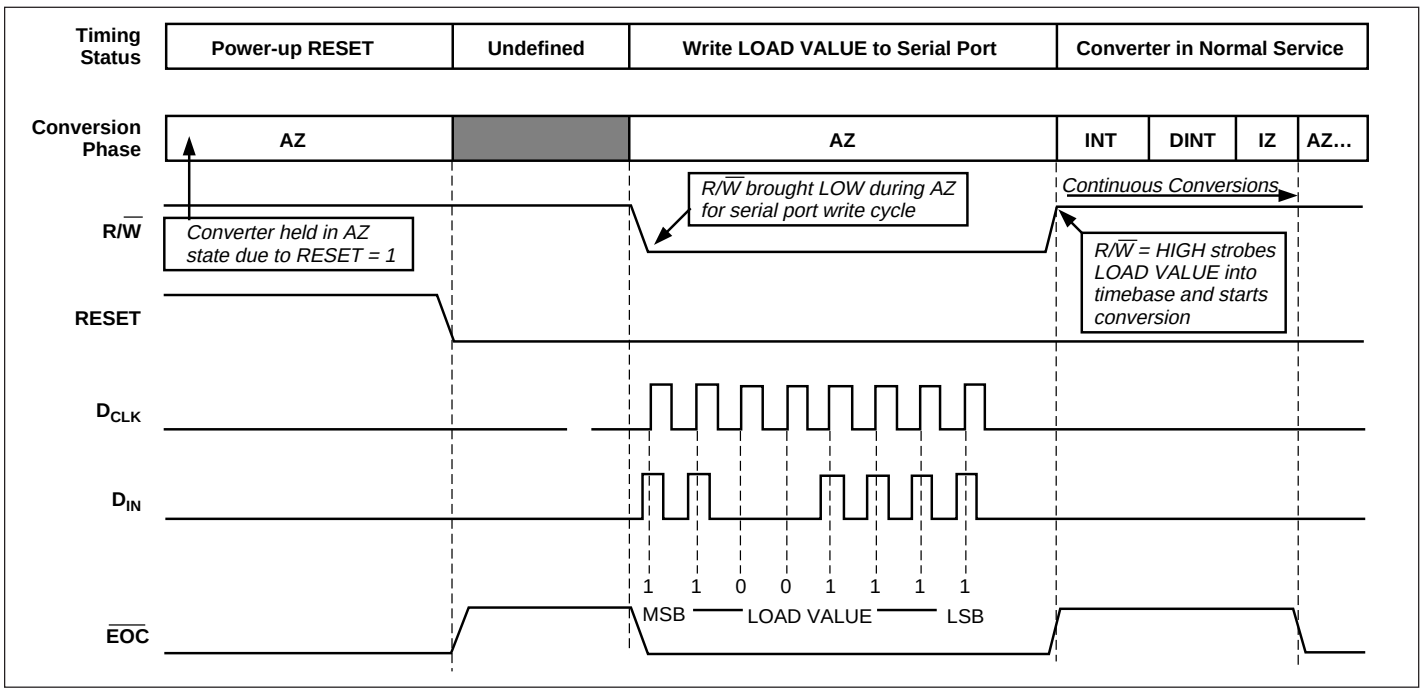


Figure 4. TC530/534 Initialization and Load Value Write Cycle

verter input. A0 is the least significant address bit (i.e., channel 1 is selected when A0 = 1 and A1 = 0). The multiplexer is designed to be operated in a differential mode. For single-ended inputs, the CHx⁻ input for the channel under selection must be connected to the ground reference associated with the input signal.

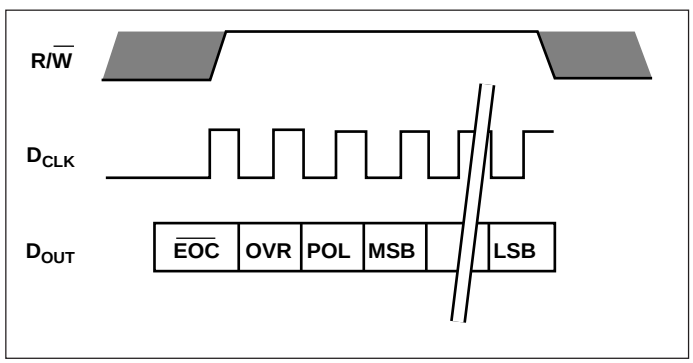


Figure 5. Serial Port Data Read Cycle

DC/DC Converter

An on-board, TC7660H-type charge pump supplies negative bias to the converter circuitry, as well as to external devices. The charge pump develops a negative output voltage by moving charge from the power supply to the reservoir capacitor at V_{SS} by way of the commutating capacitor connected to the CAP^+ and CAP^- inputs.

The charge pump clock operates at a typical frequency of 100kHz. If lower quiescent current is desired, the charge pump clock can be slowed by connecting an external capacitor from the OSC pin to V_{DD}. Reference typical characteristics curves.

APPLICATIONS

Design Example

Figure 6 shows a typical TC534 interrupt-driven application. Timing and component values are calculated from equations and recommendations made in the Dual Slope Integrating Converter and Programming the TC530/534 sections of this document. The EOC connection to the processor INT input is for interrupt-driven applications only. (In polled systems, the EOC output is available on D_{OUT}).

GIVEN

REQUIRED RESOLUTION: 16 Bits (65,536 counts.)
MAXIMUM V_{IN}: ±2V
POWER SUPPLY VOLTAGE: +5V
60Hz SYSTEM

1. **Pick Integration time (t_{INT})**
   66msec

2. **Estimate crystal frequency**
   $F_{IN} = 2R/t_{INT} = 2 \times 65536/66 \times 10^{-3} = 1.98MHz$
   (use 2MHz)

3. **Calculate LOAD VALUE**
   LOAD VALUE = $256 - (t_{INT})(F_{IN})/1024 = [128]_{10}$
   $[128]_{10}$ = 80 hex

4. **Calculate R_{INT}**
   R_{INT} (in MΩ) = $V_{INMAX}/20 = 2/20 =$ 100kΩ

5. **Calculate C_{INT} for maximum (4V) integrator output swing**
   C_{INT} (in µF) = $(t_{INT})(20 \times 10^{-6})/(V_S - 0.9)$
   $= (.066)(20 \times 10^{-6})/(4.1)$
   = .32µF (use closest value: 0.33µF)

   NOTE: TelCom recommended capacitor:
   WIMA p/n: MK12 .33/63/10

6. **Choose C_{REF} and C_{AZ} based on conversion rate**
   Conversions/sec = $1/(t_{AZ} + t_{INT} + 2t_{INT} + 2msec)$
   = 1/(66msec + 66msec + 132msec + 2msec)
   = 3.7 conversions/sec

   from which $C_{AZ} = C_{REF} =$ 0.22µF (see Table 1)

   NOTE: TelCom recommended capacitor:
   WIMA p/n: MK12 .22/63/10

7. **Calculate V_{REF}**

$$V_{REF} \text{ (in Volts } = (V_S - 0.9)(C_{INT})(R_{INT})$$

$$\frac{2(t_{INT})}{}$$

$$= (4.1)(0.33 \times 10^{-6})(10^5)/2(.066)$$

$$= 1.025V$$

Power Supply Sequencing

Improper sequencing of the power supply inputs (V_{DD} vs. V_{CCD}) can potentially cause an improper power-up sequence to occur. See *Circuit Design/Layout Considerations* below. Failing to insure a proper power-up sequence can cause spurious operation.

Ciruit Design/Layout Considerations

(1) Separate ground return paths should be used for the analog and digital circuitry. Use of ground planes and trace fill on analog circuit sections is highly recommended *EXCEPT* for in and around the integrator section and C_{REF}, C_{AZ}. (C_{INT}, C_{REF}, C_{AZ}, R_{INT}). Stray capacitance between these nodes and ground appears in parallel with the components themselves and can affect measurement accuracy.

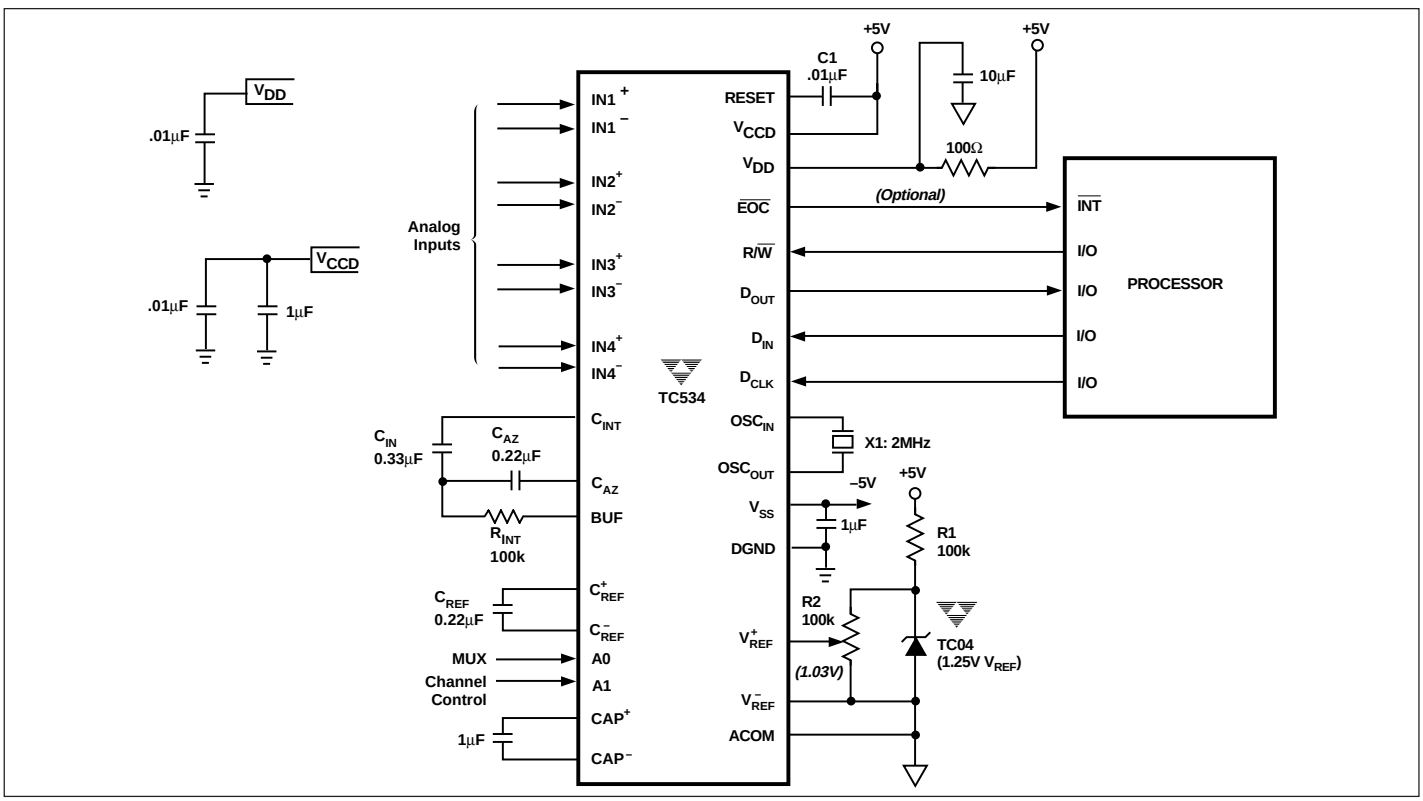


Figure 6. TC530/534 Typical Application

(2) Improper sequencing of the power supply inputs (V_{DD} vs. V_{CCD}) can potentially cause an improper power-up sequence to occur in the internal state machines. It is recommended that the digital supply, V_{CCD}, be powered up first. One method of insuring the correct power-up sequence is to delay the analog supply using a series resistor and a capacitor. See Figure 6, TC530/534 Typical Application.

(3) Decoupling capacitors, preferably a higher value electrolytic or tantulum in parallel with a small ceramic or tantalum, should be used liberally. This includes bypassing the supply connections of all active components and the voltage reference.

(4) Critical components should be chosen for stability and low noise. The use of a metal-film resistor for R_{INT} and Polypropylene or Polyphenelyne Sulfide (PPS) capacitors for C_{INT}, C_{AZ}, and C_{REF} is highly recommended.

(5) The inputs and integrator section are very high impedance nodes. Leakage to or from these critical nodes can contribute measurement error. A guard-ring should be used to protect the integrator section from stray leakage.

(6) Circuit assemblies should be scrupulously clean to prevent the presence of contamination from assembly, handling, or the cleaning itself. Minutely conductive trace contaminates, easily ignored in most applications, can adversely affect the performance of high impedance circuits. The input and integrator sections should be made as compact and close to the TC53x as possible.

(7) Digital and other dynamic signal conductors should be kept as far from the TC53x's analog section as possible. The microcontroller or other host logic should be kept quiet during a measurement cycle. Background activites such as keypad scanning, display refreshing, and power switching can introduce noise.

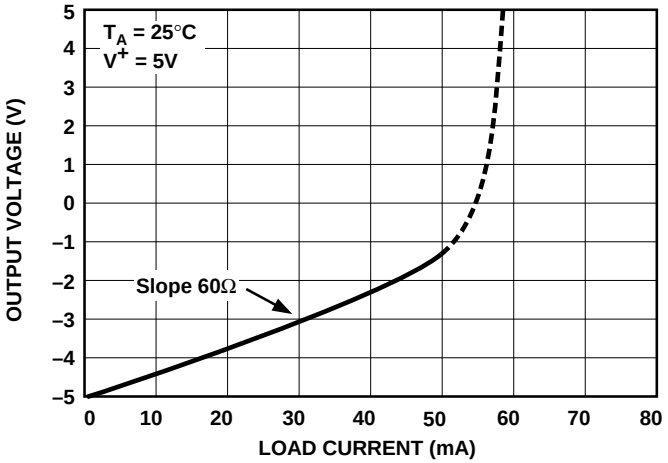
TC530EV Evaluation Kit

The TC530EV consists of a 4" x 6" pre-assembled circuit board that connects to the serial port of any PC or dumb terminal. Also included is a Windows™* Excel™*-based design utility that calculates component and LOAD values based on user input, and prints a finished circuit schematic. Please contact your local TelCom representative for more information, or point your web browser to http://www.telcom-semi.com.

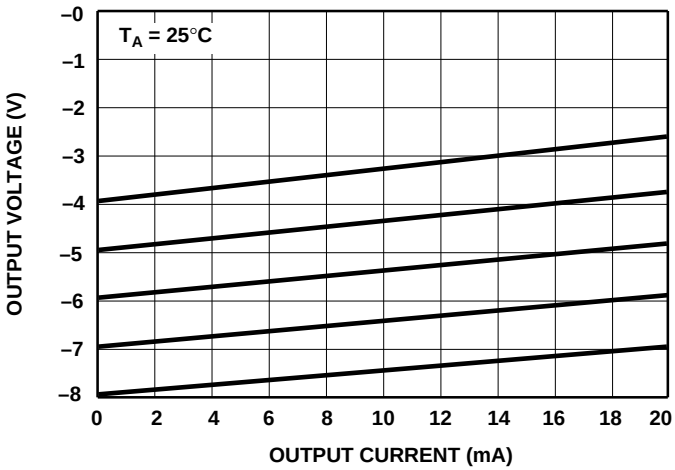
*All trademarks are the property of their respective owners.

TYPICAL CHARACTERISTICS

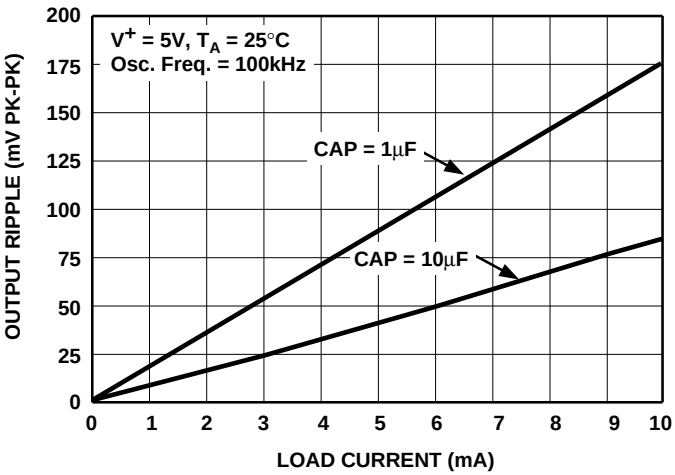
Output Voltage vs Load Current



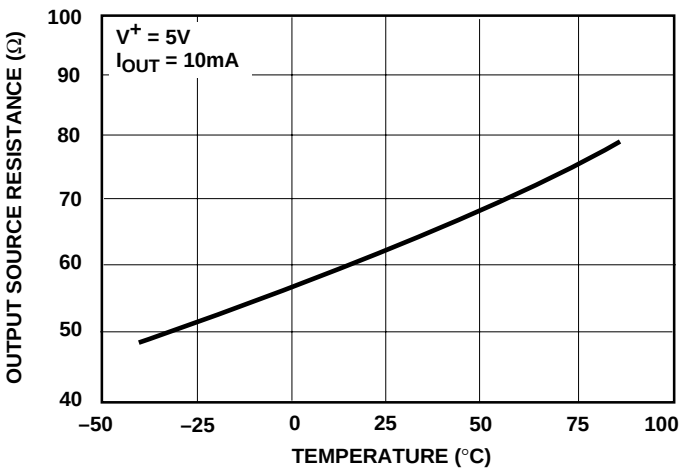
Output Voltage vs. Output Current



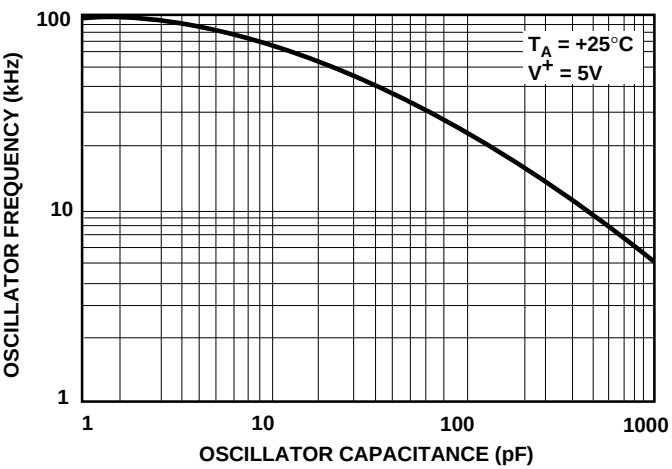
Output Ripple vs. Load Current



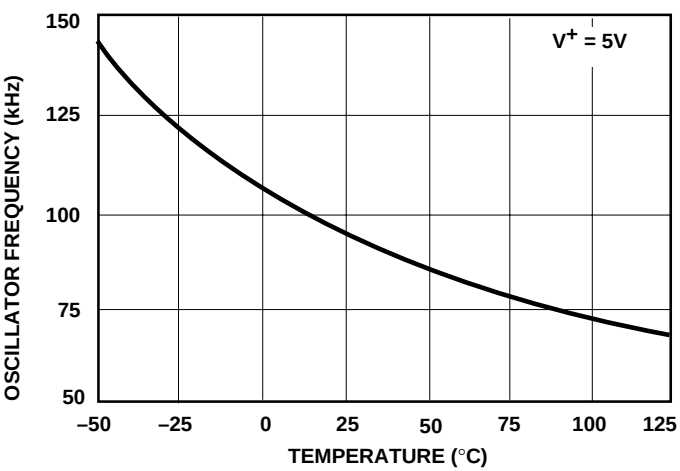
Output Source Resistance vs. Temperature



Oscillator Frequency vs. Capacitance



Oscillator Frequency vs. Temperature



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Fax: 3-7 61 41 61

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Fax: 9 05-8 90-16 28

Hong Kong:
REALTRONICS CO. LTD.
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Fax: 28 06 84 74

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SUSAN AGENCIES
P.O. Box 2138
Srirampuram P.O.
Bangalore-560 021
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Fax: 0 80-3 32 43 38

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Rehavot 76121
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