Introduction

The Supertex HV302DB1 demo board contains all circuitry necessary to demonstrate the features of the HV302 hotswap controller. Intended primarily as a negative hotswap controller, the HV302 controls the negative supply path. Four sequenced power-good signals are provided, with timing controlled via 3 resistors.

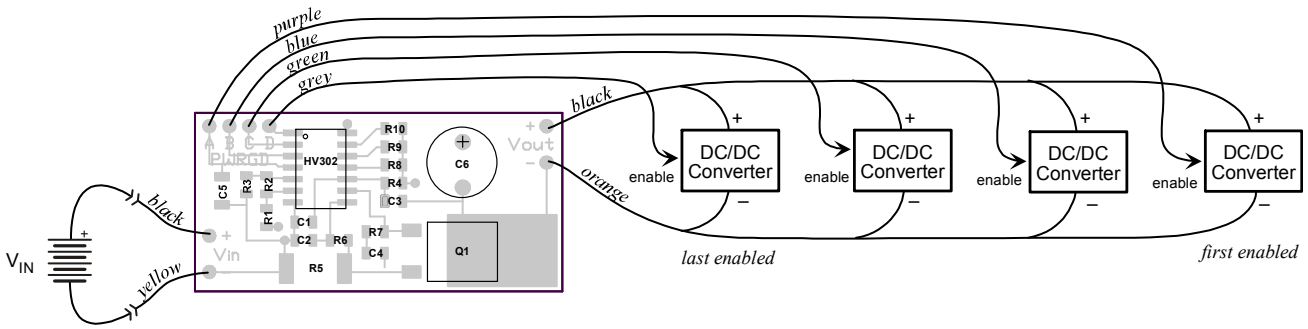
Included on board is a 100µF capacitor to provide a capacitive load for testing. Additional capacitance may be connected to the V_{OUT} terminals. Or the 100µF may be removed altogether

The board may be modified to meet custom requirements. Instructions are provided on the next page for modifications.

Specifications

Input Voltage	10V to 90V
Inrush Limit	1A ±20%
Circuit Breaker Trip	6.7A ±20%
Retry Interval	16sec typ
On Resistance	40mΩ max
Undervoltage Trip	38.0V on, 32.2V off
Overvoltage Trip	64.5V on, 70.0V off
Power Good Signals	Active High
PWRGD A	~5ms after C_{LOAD} charged
PWRGD B	~200ms after 'A'
PWRGD C	~100ms after 'B'
PWRGD D	~5ms after 'C'

Board Layout and Connections



V_{IN}

Connect the supply voltage to these terminals. Supply voltage may range from 10 volts to 90 volts.

A high source impedance may cause oscillations when the input voltage is near the undervoltage trip point. A high source impedance results in a large voltage drop when loaded, causing undervoltage lockout to kick in, disconnecting the load. With the load removed, input voltage rises, causing undervoltage to release and reconnecting the load. The cycle repeats, resulting in oscillations. Source impedance must be less than the following to avoid oscillations:

$$R_{SOURCE} < \frac{3V}{I_{LOAD}}$$

V_{OUT}

Connect the power supply or other load to these terminals. V_{OUT+} is connected to V_{IN+}, it is V_{OUT-} that is switched.

Application of a DC load during start-up extends the time inrush limiting is active. If this time exceeds 100ms, the HV302 shuts off, retrying as quickly as 12s later. For this reason, DC load at start-up should be less than 900mA. Note that DC start-up load limitation decreases with added load capacitance.

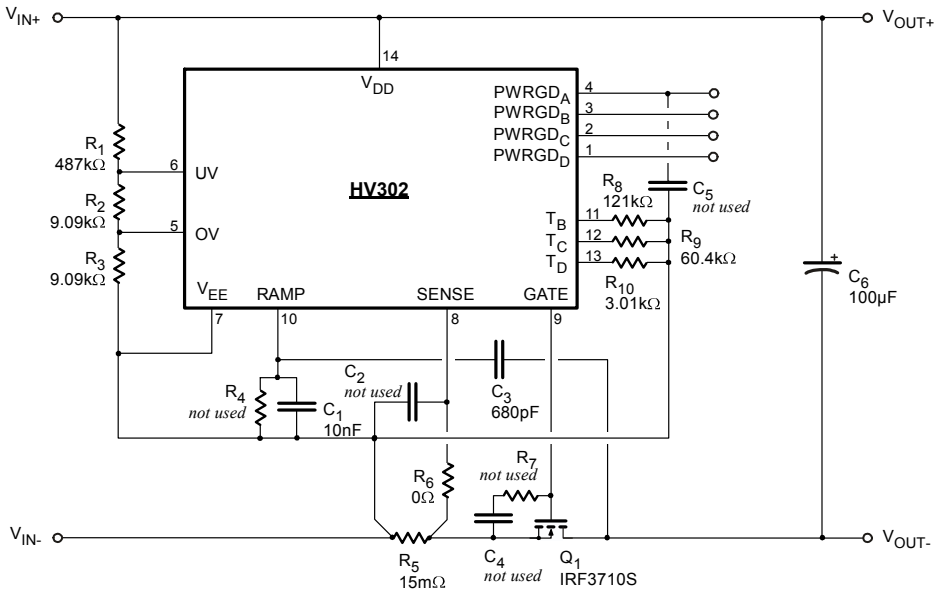
Connecting additional load capacitance alters the inrush current limit. See the HV302/312 data sheet for details.

PWRGD

Connect to the power supply's ENABLE inputs. Depending on the power supply, it may be necessary to level-translate this signal via opto-isolator or discrete circuit. Refer to the HV302/312 data sheet for a description of PWRGD and related application circuits.

PWRGD is an open-drain output. During start-up and whenever V_{IN} is lower than the undervoltage trip point or greater than the overvoltage trip point, PWRGD is pulled down to V_{IN-}. Once V_{IN} is within the proper range and the load capacitance has fully charged, PWRGD assumes a high impedance state.

Schematic



Inrush Limit

As supplied, the inrush current limit is set at 1 amp. To set inrush limit to another value, please refer to the HV302/312 data sheet.

The circuit breaker trip point is set at 6.7 Amps. To set at a different level, change R_5 according to the following equation:

$$I_{CB} = \frac{100\text{mV}}{R_5}$$

The power rating of R_5 should be selected based on maximum current during normal operation, which could be just under the circuit breaker trip point.

$$P_5 = 100\text{mV} \cdot I_{CB}$$

Timing

Timing capacitor C_1 determines start-up delay, rise time, and circuit breaker retry interval,. Changing C_1 will alter these timings. Refer to the HV302/312 datasheet for the equations that relate these timings to the value of C_1. For use in the equations, the nominal gate threshold voltage (V_{GS}) of the supplied IRFR3710 is 3V and transconductance is about 10 siemens.

Resistors R_8, R_9, and R_{10} set the delays for PWRGDs B, C, and D according to the following equation:

$$t_D = 1.67\mu\text{F} \cdot R_X$$

Circuit Breaker Transient Immunity

The HV302 has built-in transient immunity of 2–5µs. To increase transient immunity, an RC low-pass filter (R_6C_2) may be placed on the SENSE input. (The demo board is supplied with no filtering.)

Be aware that filtering the sense input will cause the inrush current limit to overshoot at turn-on – the greater the filtering, the greater the overshoot.

Undervoltage/Overvoltage Lockout

Resistors R_1, R_2, and R_3 set the undervoltage and overvoltage trip points. New trip points may be programmed by changing the values of these resistors. Refer to the HV302/312 data sheet for more information.

Additional Components

The RC network (R_7C_4) across the gate-source of the external FET provides control loop compensation which prevents inrush current peaking.

If the PWRGD A signal is used and experiences large voltage swings, a 10nF capacitor should be installed at C_5. This limits dV/dt which may otherwise cause undesirable coupling to internal circuits.

To defeat the circuit breaker auto-retry, install a 2.4MΩ resistor at location R_4.

For servo-mode inrush control, remove C_3. Inrush limit will then be 3.3 Amps. See the HV302/312 data sheet for details.