



AKD4388-SB

AK4388 Evaluation board Rev.1

General Description

The AKD4388-SB is an evaluation board for AK4388, which is 192kHz sampling 24Bit $\Delta\Sigma$ DAC. The AKD4388-SB includes a LPF which can add differential analog outputs from the AK4388 and also has a digital interface. Therefore, it is easy to evaluate the AK4388.

■ Ordering Guide

AKD4388-SB --- Evaluation board for AK4388

Function

- On-board Analog output buffer circuit
- On-board digital audio interface. (AK4113)

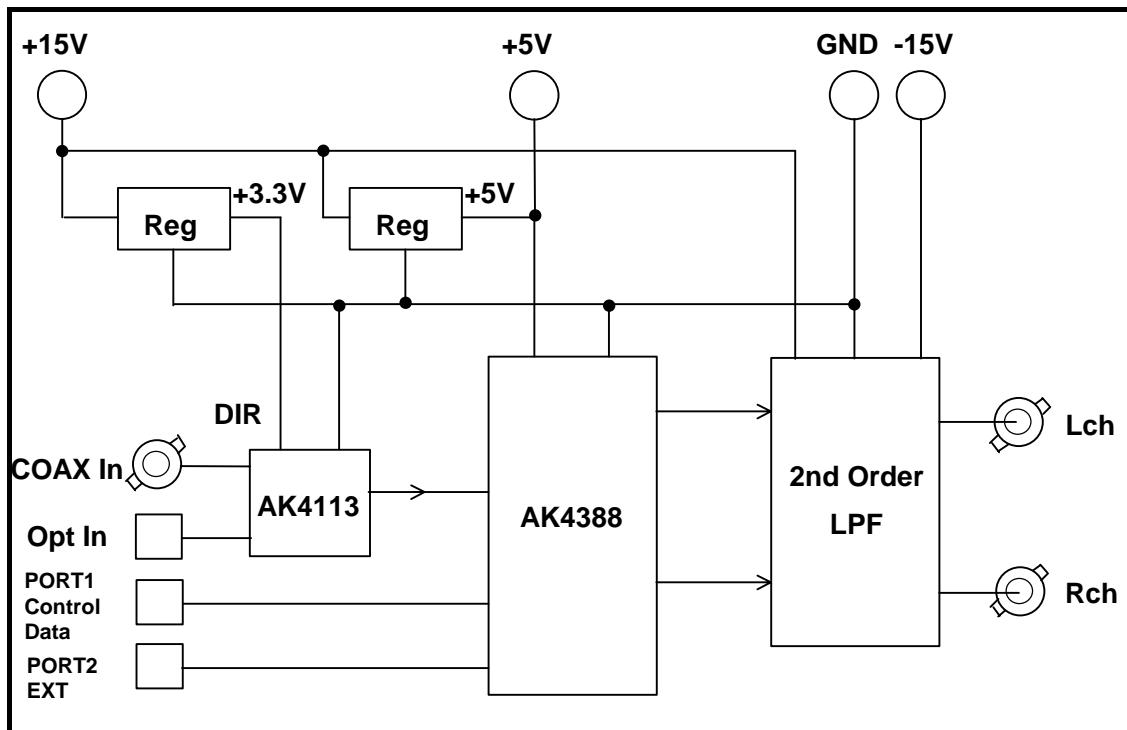


Figure 1. AKD4388-SB Block diagram

* Circuit diagram are attached at the end of this manual.

COAX is recommended for an evaluation of the Sound quality.

■ Operation sequence

- 1) Set up the power supply lines. (See “Other jumpers set-up”.)

Name	Color	Voltage	Comments	Attention
+15V	Green	+12~+15V	For regulator and op-amps.	This jack should be always connected to power supply.
-15V	Blue	-12~-15V	For op-amps.	This jack should be always connected to power supply.
5V	Red	+4.75~+5.25V	For AK4388.	This jack should be always connected to power supply.
AGND	Black	0V	GND	This jack should be always connected to power supply.

Table 1. Set up of power supply lines

Each supply line should be distributed from the power supply unit.

- 2) Set-up the jumper pins
- 3) Set-up the DIP switches. (See the followings.)
- 4) Power on

The AK4388 should be reset once by bringing SW4 (PDN) “L” upon power-up.

■ Evaluation mode

1. DIR (COAX) (default)

It is possible to evaluate the AK4388 by using CD disk. The DIR generates MCLK, BICK, LRCK and SDATA from the received data through RCA connector (J3). Setting of jumper is shown below.

COAX is recommended for an evaluation of the Sound quality.

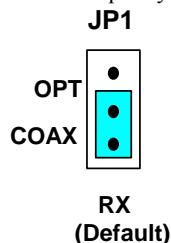


Figure 2. Jumper setting, when using DIR

2. DIR (Optical Link)

It is possible to evaluate the AK4388 by using CD disk. The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT3: TORX173). Setting of jumper is shown below.

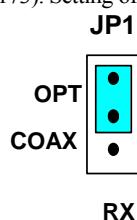


Figure 3. Jumper setting, when using DIR

3. All clocks are fed through the PORT2.

R1, R2, R3, R4 : open

R26, R27, R28, R30 : 100Ω or short (0Ω)

■ DIP Switch setting

[SW1]: AK4388 setting

No.	Pin	SW1 OFF	SW1 ON	Default
1	SMUTE	Soft Mute : "Disable"	Soft Mute : "Enable"	OFF
2	P/S	Always ON for Parallel Control mode only		ON
3	ACKS	Manual setting mode	Auto setting mode	ON
4	DIF0	Audio Data Formats Refer to Table7		OFF

Table 2. SW1 setting

[SW2]: AK4388 setting

No.	Pin		Default
1	-	NC	OFF
2	-	NC	OFF
3	DEM	De-emphasis Control setting Refer to Table6	OFF
4	DIF1	Audio Data Formats Refer to Table7	ON

Table 3. SW2 setting

[SW3]: AK4113 setting

No.	Pin	OFF	ON	Default
1	OCKS1	AK4113 Master Clock setting Refer to Table 5.		ON
2	OCKS0			OFF

Table 4. SW3 setting

The frequency of the master clock output is set by OCKS0 and OCKS1 as shown in Table 5.

OCKS1	OCKS0	MCLK Frequency	Default
0	0	256fs @fs=88.2/96kHz	
1	0	512fs @32/44.1/48kHz	
1	1	128fs @176.4/192kHz	

Table 5. MCLK Clock

The digital de-emphasis filter is set by DEM pin as follows.

DEM SW	DEM pin state	De-emphasis Filter	Default
OFF	1	ON	
ON	0	OFF	

Table 6. De-emphasis Filter Control

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-1 as shown in Table 7 can select four serial data modes.

Mode	DIF1 SW	DIF0 SW	DIF1 pin state	DIF0 pin state	SDTI Format	BICK	Default
0	ON	ON	0	0	16bit LSB justified	$\geq 32fs$	
1	ON	OFF	0	1	24bit LSB justified	$\geq 48fs$	
2	OFF	ON	1	0	24bit MSB justified	$\geq 48fs$	
3	OFF	OFF	1	1	16/24bit I ² S Compatible	$\geq 48fs$ or 32fs	

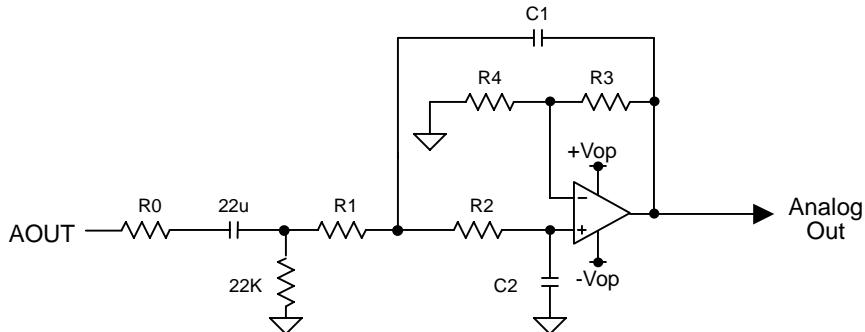
Table 7. Audio Data Formats

■ Toggle switch setting

[SW4](PDN): Reset of AK4388. Select “H” during operation.

■ External Analog Circuit

The 2nd order LPF ($f_c=125.6\text{kHz}$, $Q=0.753$) which adds differential outputs of the AK4388 is implemented on the board. When the further attenuation of the out-band noise is needed, some additional LPF is required. Analog signal is output through BNC connectors on the board. And the output level of the AK4388 is $5.67\text{Vpp}@5\text{V}$.



$f_c=125.6\text{kHz}$, $Q=0.753$, $g=0.060\text{dB}$ at 40kHz

Figure 4. External Analog Filter

R ₀	R ₁	R ₂	R ₃	R ₄	C ₁	C ₂
910	1.8k	3.9k	3.3k	3.9k	390p	390p

Table 8. The value of R,C on this board

fin	20kHz	40kHz	80kHz
Frequency Response	0.023dB	0.060dB	-0.288dB

Table 9. Frequency Response of LPF

<Calculation>

$$\text{Amplitude} = 20 \log \frac{K}{\sqrt{[1-(f/f_c)^2]^2 + [(1/Q)(f/f_c)]^2}} [\text{dB}],$$

$$K = \frac{R_3 + R_4}{R_4},$$

$$f_c = \frac{\omega_0}{2\pi},$$

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}},$$

$$Q = 2\pi f c \frac{1}{\frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1-k}{C_2 R_2}}$$

Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (44.1kHz), 256fs (96kHz), 128fs (192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : VDD=5V
- Interface : Internal DIR (44.1kHz, 96kHz, 192kHz)
- Temperature : Room

fs=44.1kHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	94.8dB	96.3dB
	1kHz, -60dB	20kLPF	102.6dB	102.6dB
DR	1kHz, -60dB	22kLPF, A-weighted	104.6dB	104.6dB
S/N	“0” data	20kLPF	103.9dB	103.9dB
	“0” data	22kLPF, A-weighted	105.3dB	105.3dB

fs=96kHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	93.3dB	94.5dB
	1kHz, -60dB	40kLPF	102.6dB	102.1dB
DR	1kHz, -60dB	22kLPF, A-weighted	104.6dB	103.9dB
S/N	“0” data	40kLPF	103.2dB	103.2dB
	“0” data	22kLPF, A-weighted	105.3dB	104.6dB

fs=192kHz

Parameter	Input signal	Measurement filter	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	92.3dB	93.5dB
	1kHz, -60dB	40kLPF	102.0dB	101.5dB
DR	1kHz, -60dB	22kLPF, A-weighted	104.5dB	103.9dB
S/N	“0” data	40kLPF	103.2dB	102.6dB
	“0” data	22kLPF, A-weighted	105.3dB	105.3dB

Plots

(fs=44.1kHz)

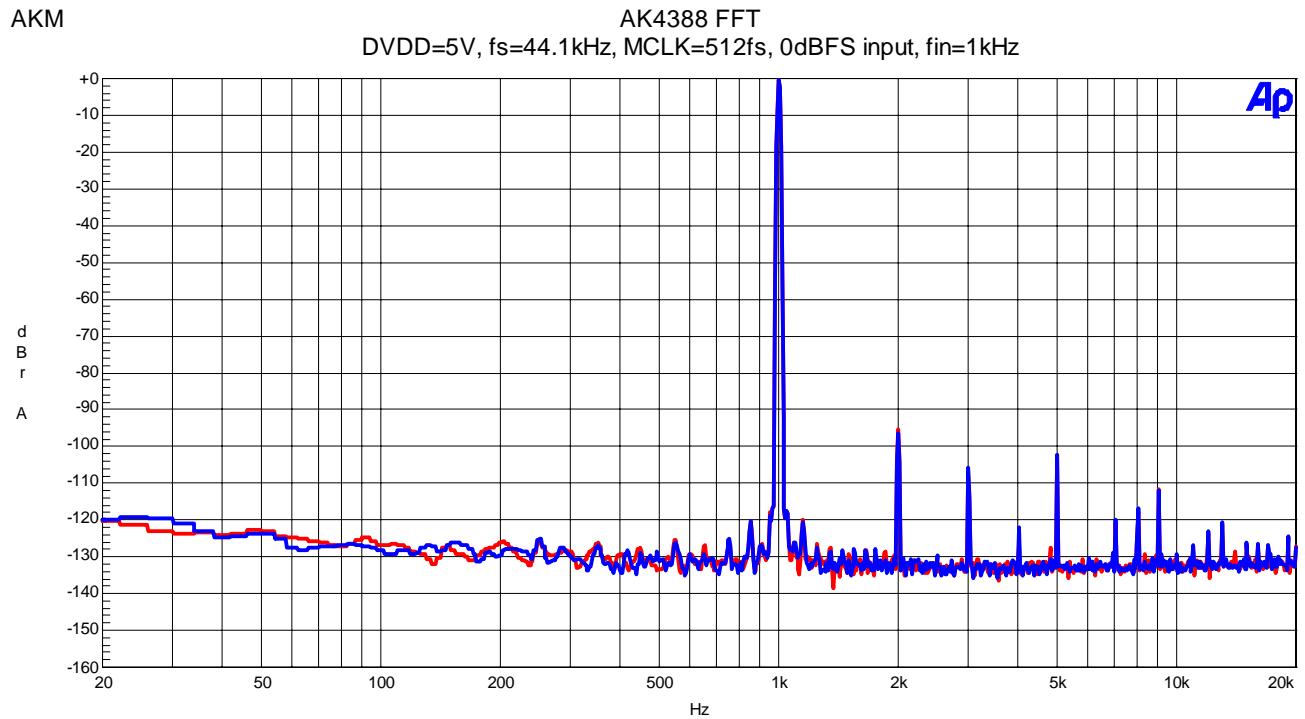


Figure 5. FFT (fin=1kHz, 0dBFS input)

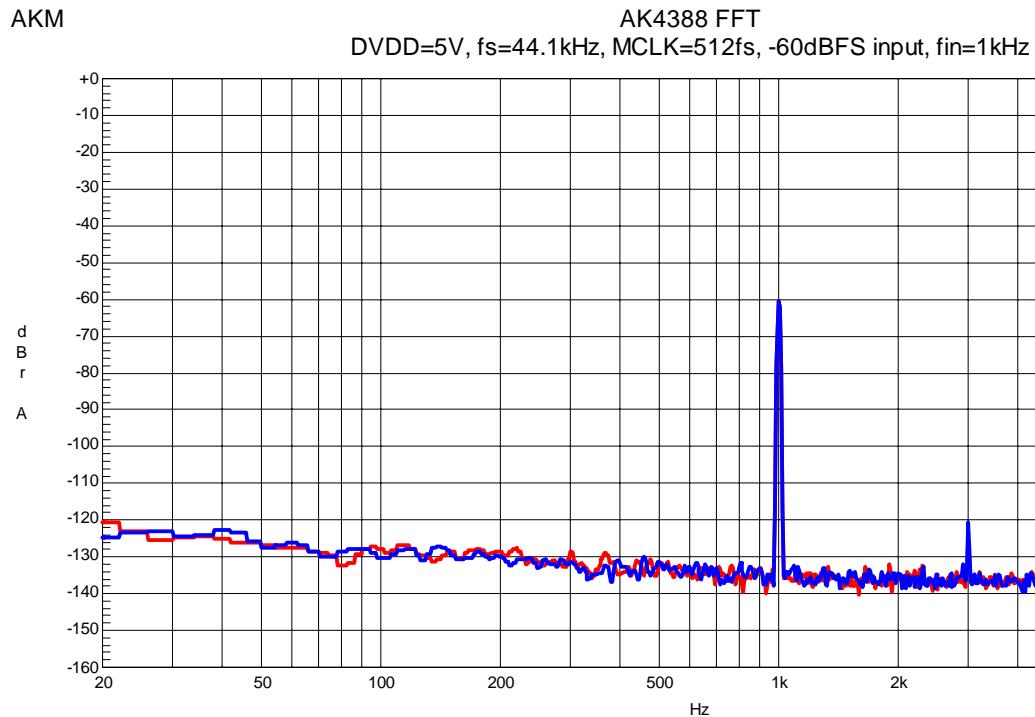


Figure 6. FFT (fin=1kHz, -60dBFS input)

(fs=44.1kHz)

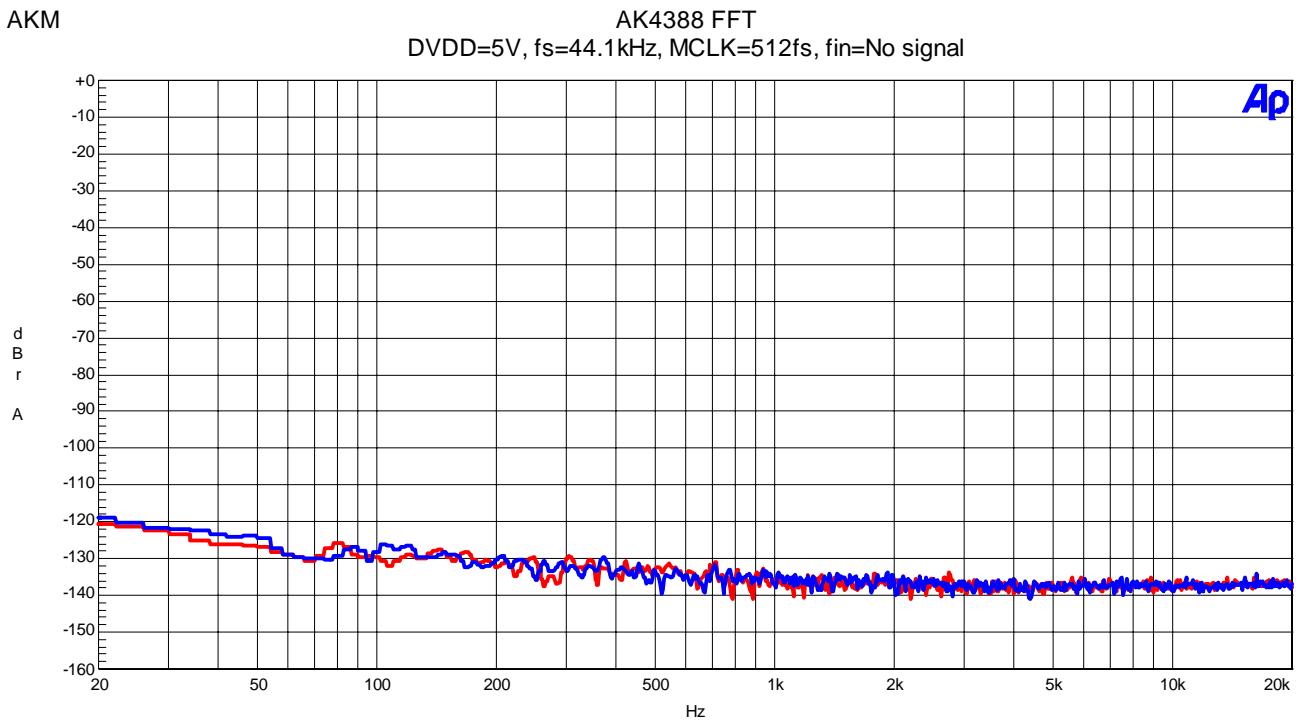


Figure 7. FFT (Noise Floor)

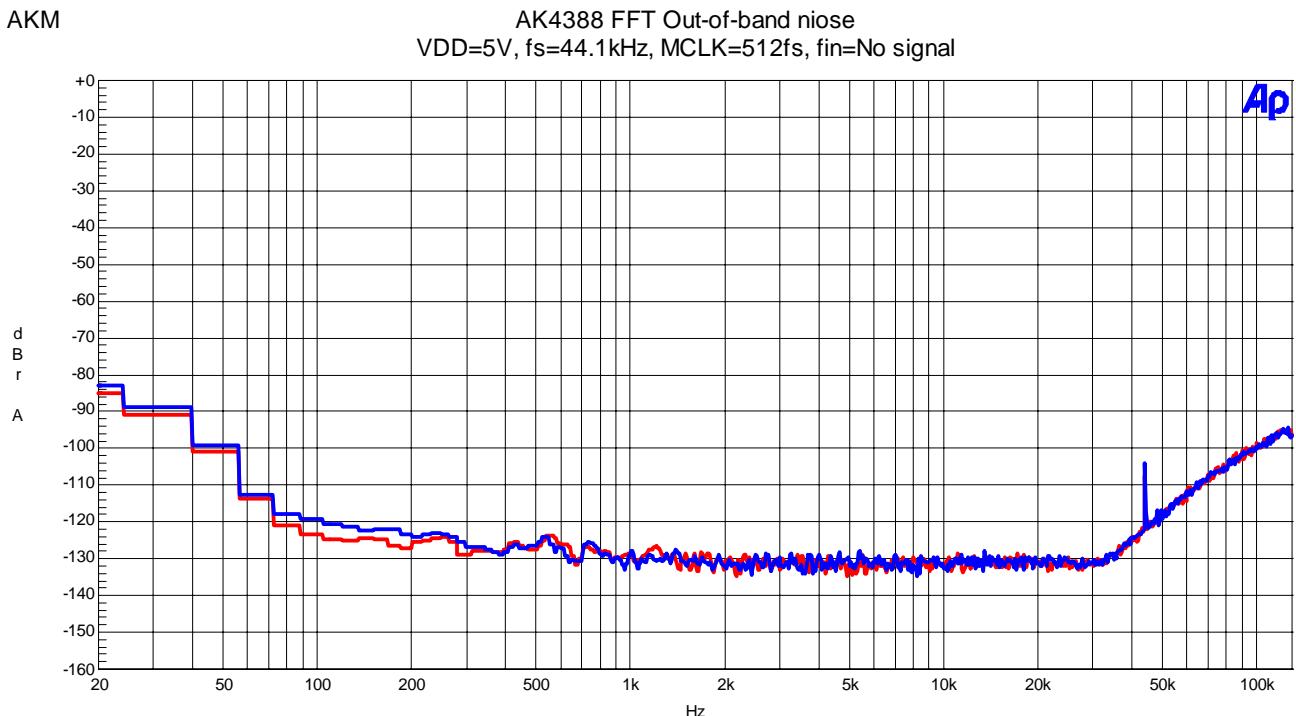


Figure 8. FFT (Out of band noise)

(fs=44.1kHz)

AKM

AK4388 THD+N vs. Input Level
VDD=5V, fs=44.1kHz, MCLK=512fs, fin=1kHz

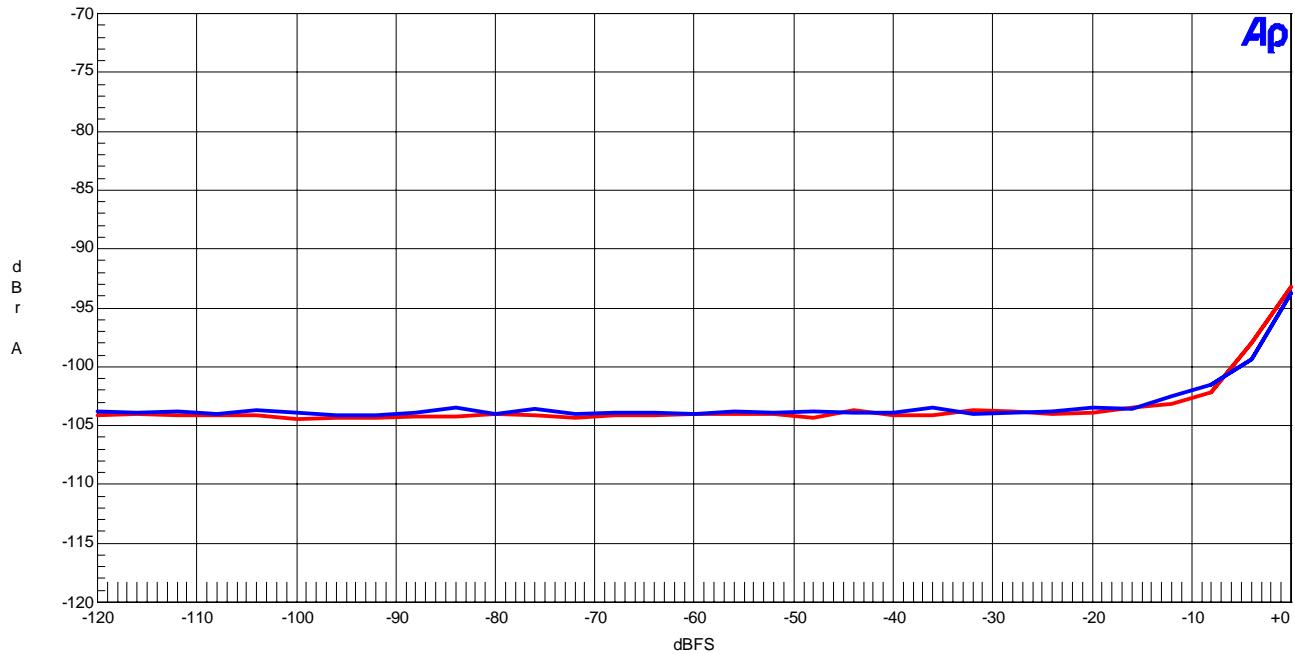


Figure 9 . THD+N vs. Input level (fin=1kHz)

AKM

AK4388 THD+N vs. Input Frequency
VDD=5V, fs=44.1kHz, MCLK=512fs, 0dBFS input

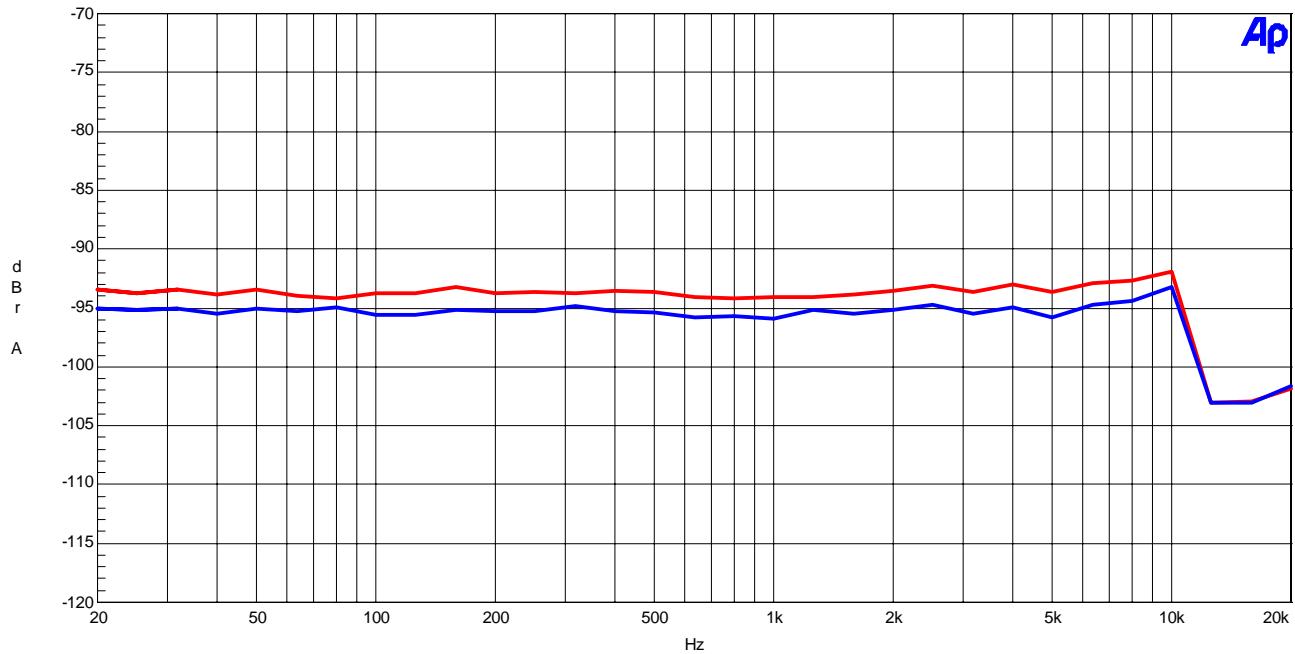


Figure 10 . THD+N vs. Input Frequency (0dBFS input)

(fs=44.1kHz)

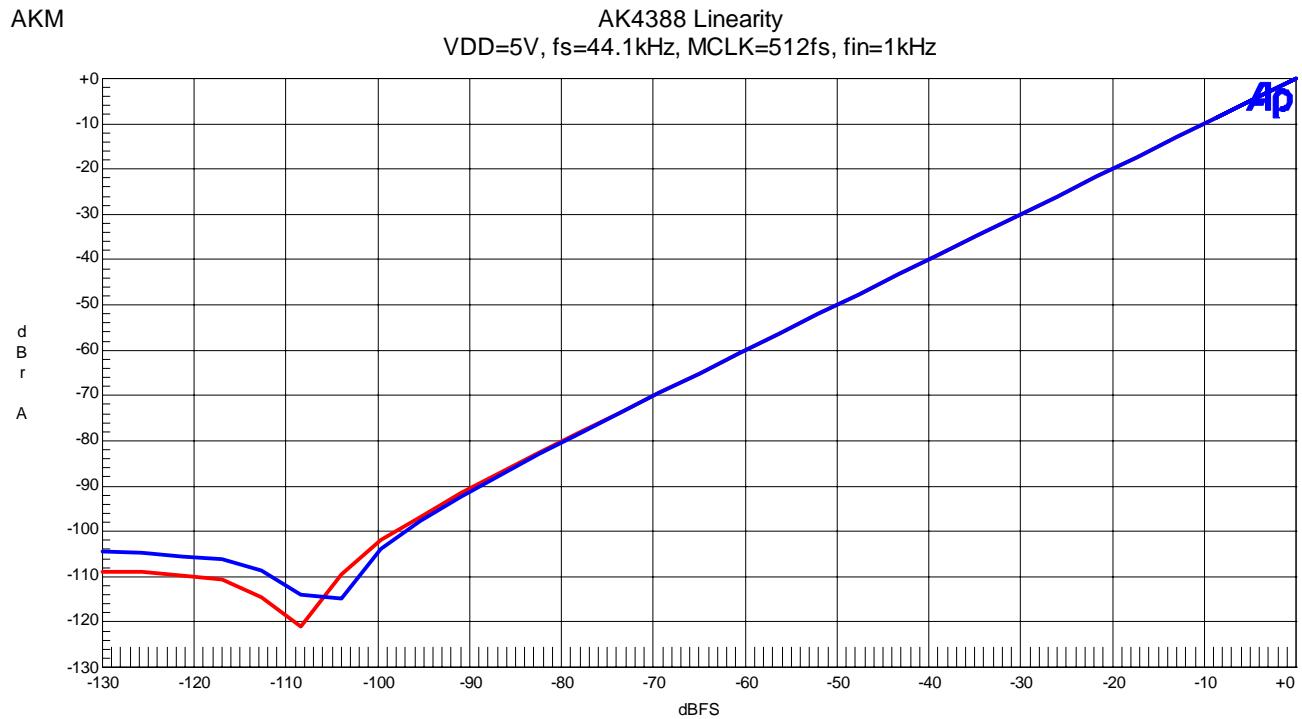


Figure 11. Linearity (fin=1kHz)

AKM AK4388 Frequency Response
VDD=5V, fs=44.1kHz, MCLK=512fs, 0dBFS input

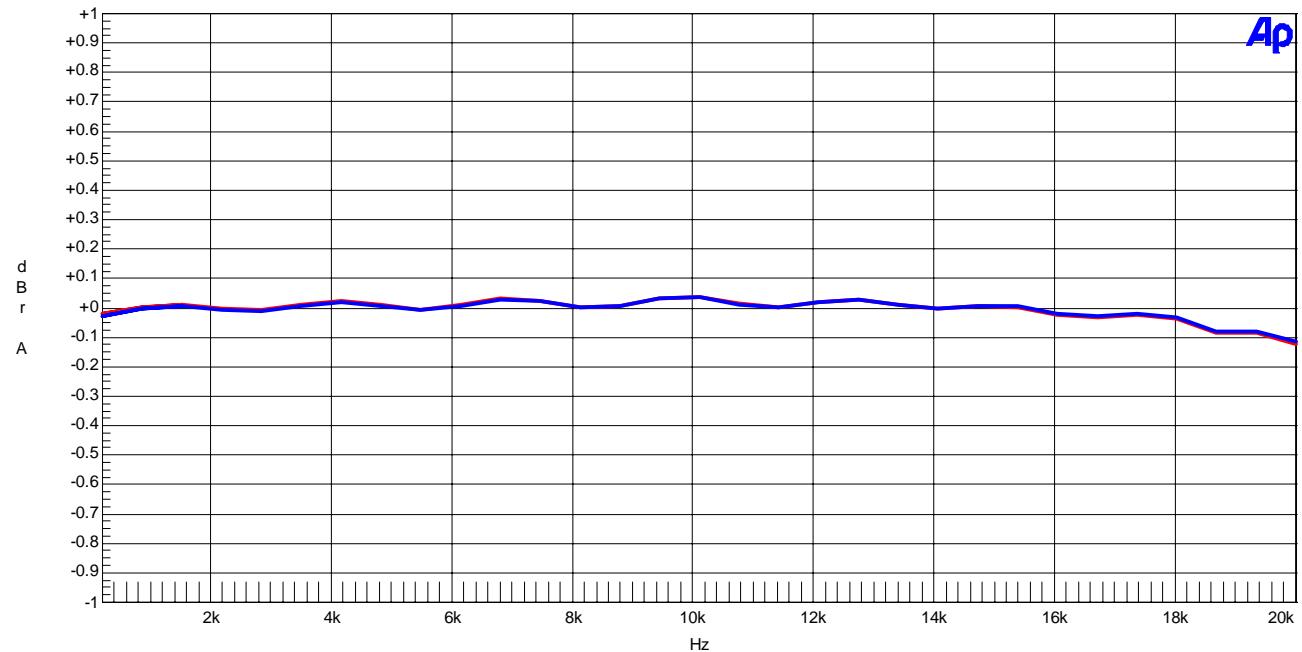


Figure 12. Frequency Response (0dBFS input)

(fs=44.1kHz)

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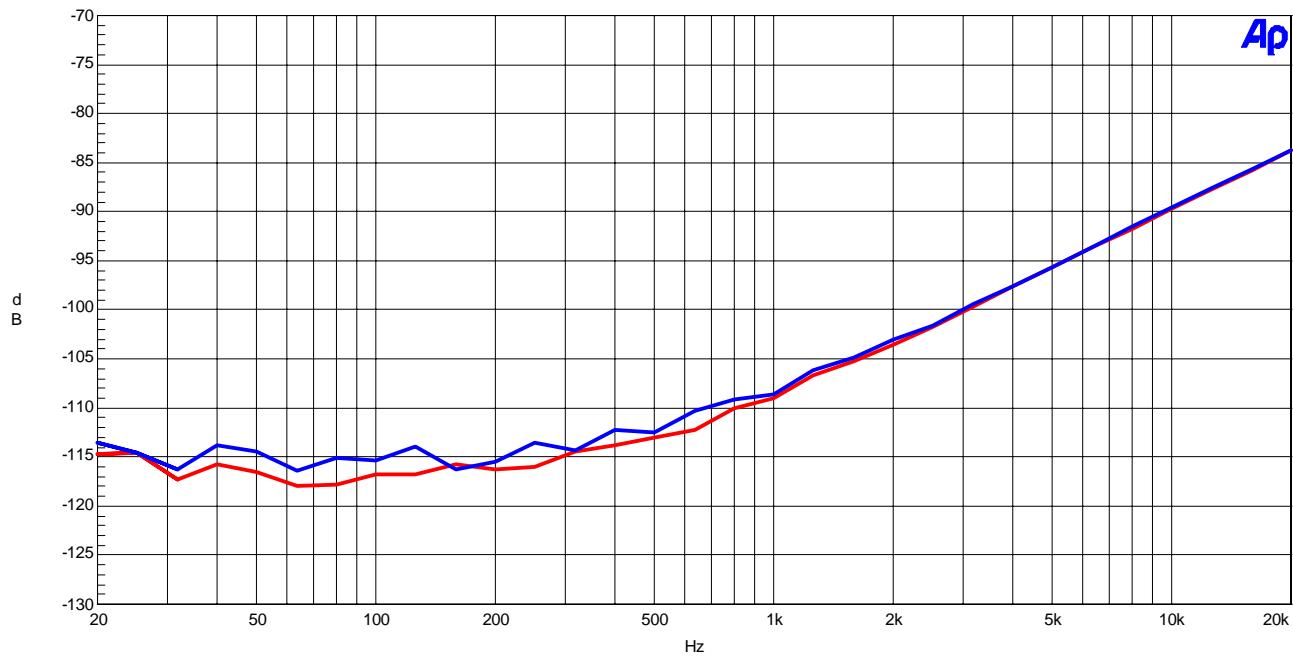
AK4388 Crosstalk (Red=Lch, Blue=Rch)
VDD=5V, fs=44.1kHz, MCLK=512fs, 0dBFS input

Figure 13. Crosstalk (0dBFS input)

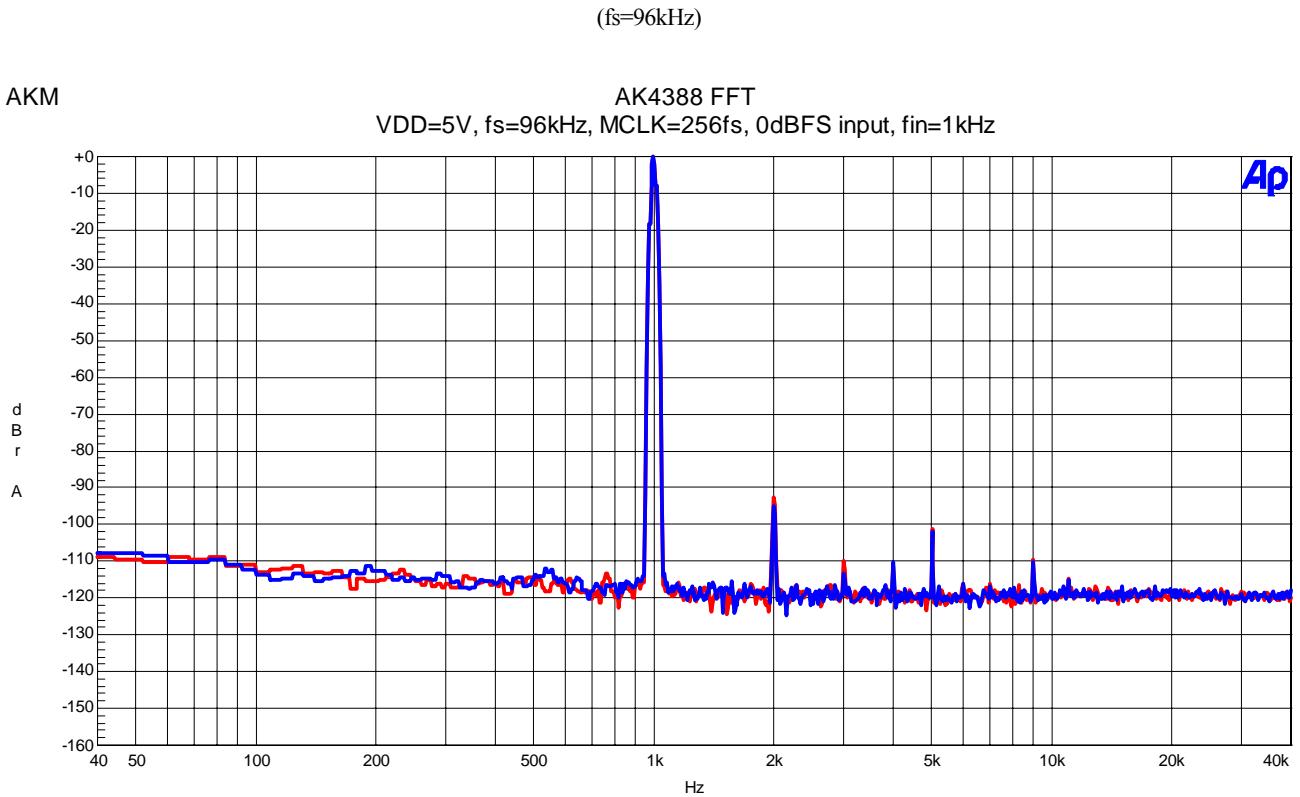


Figure 14. FFT (fin=1kHz, 0dBFS input)

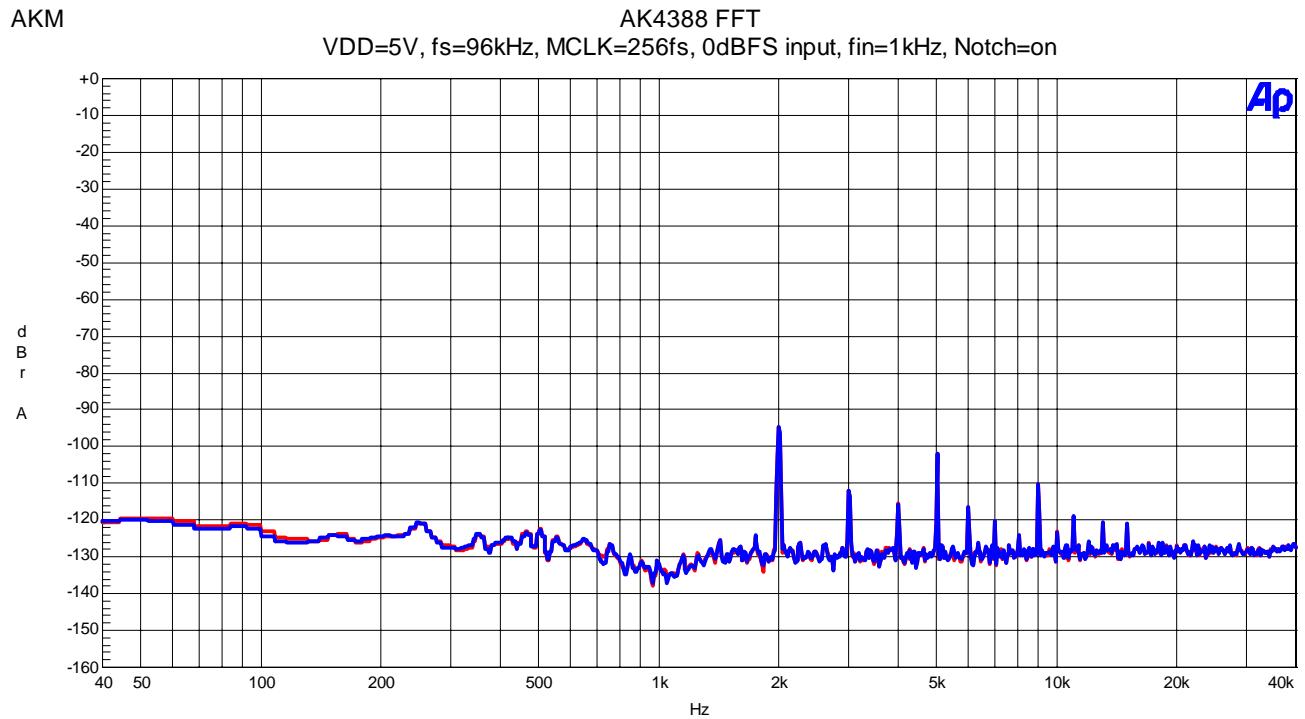


Figure 15. FFT(fin=1kHz, 0dBFS input, Notch)

(fs=96kHz)

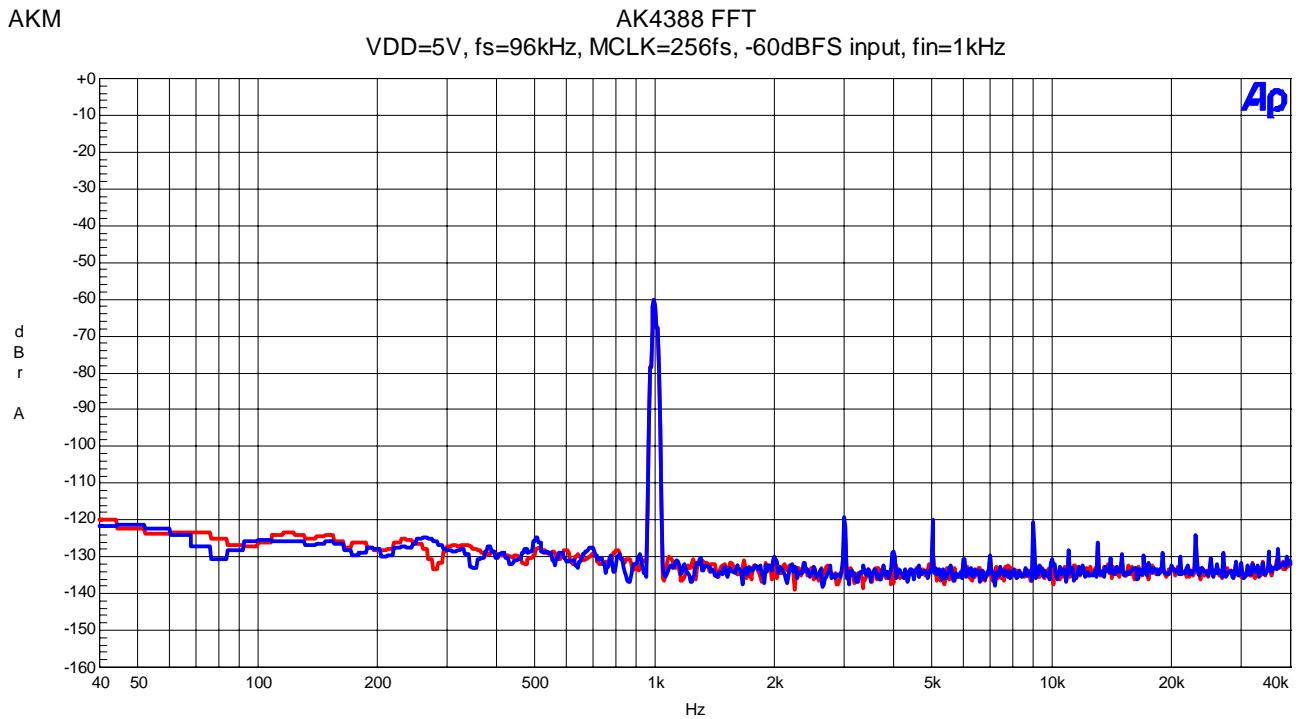


Figure 16. FFT (fin=1kHz, -60dBFS input)

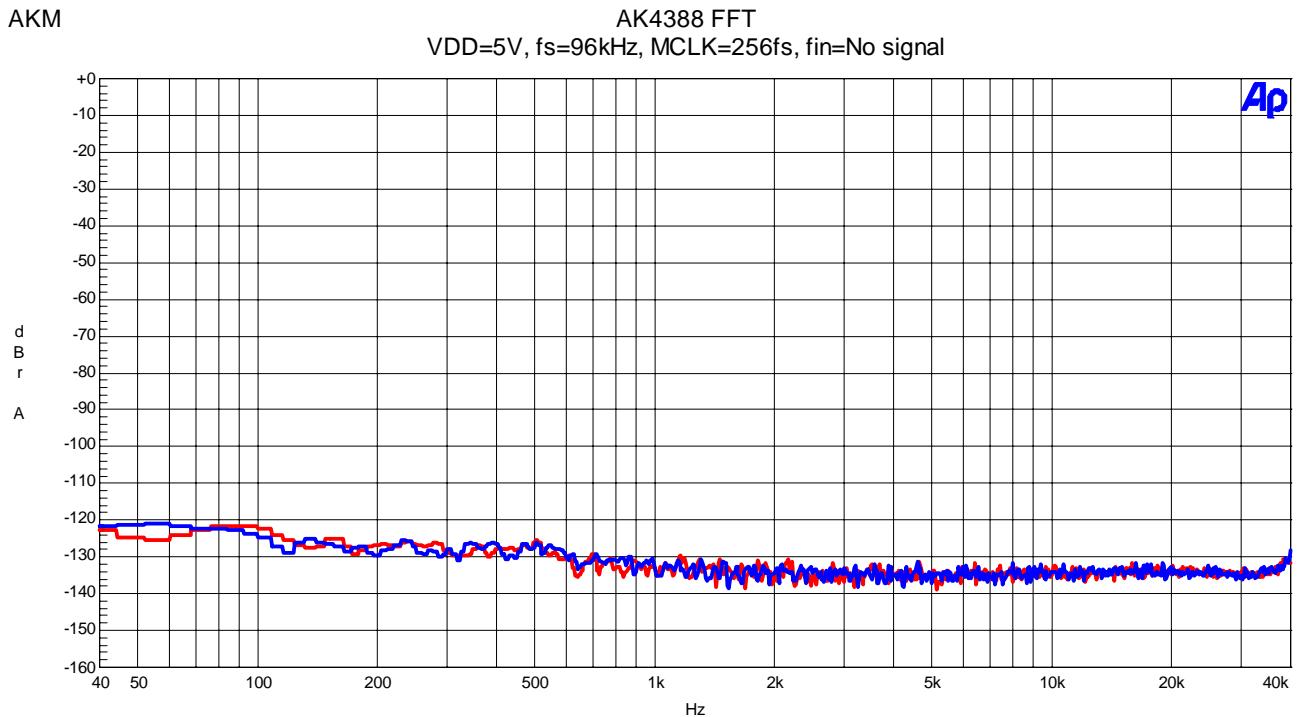


Figure 17. FFT (Noise Floor)

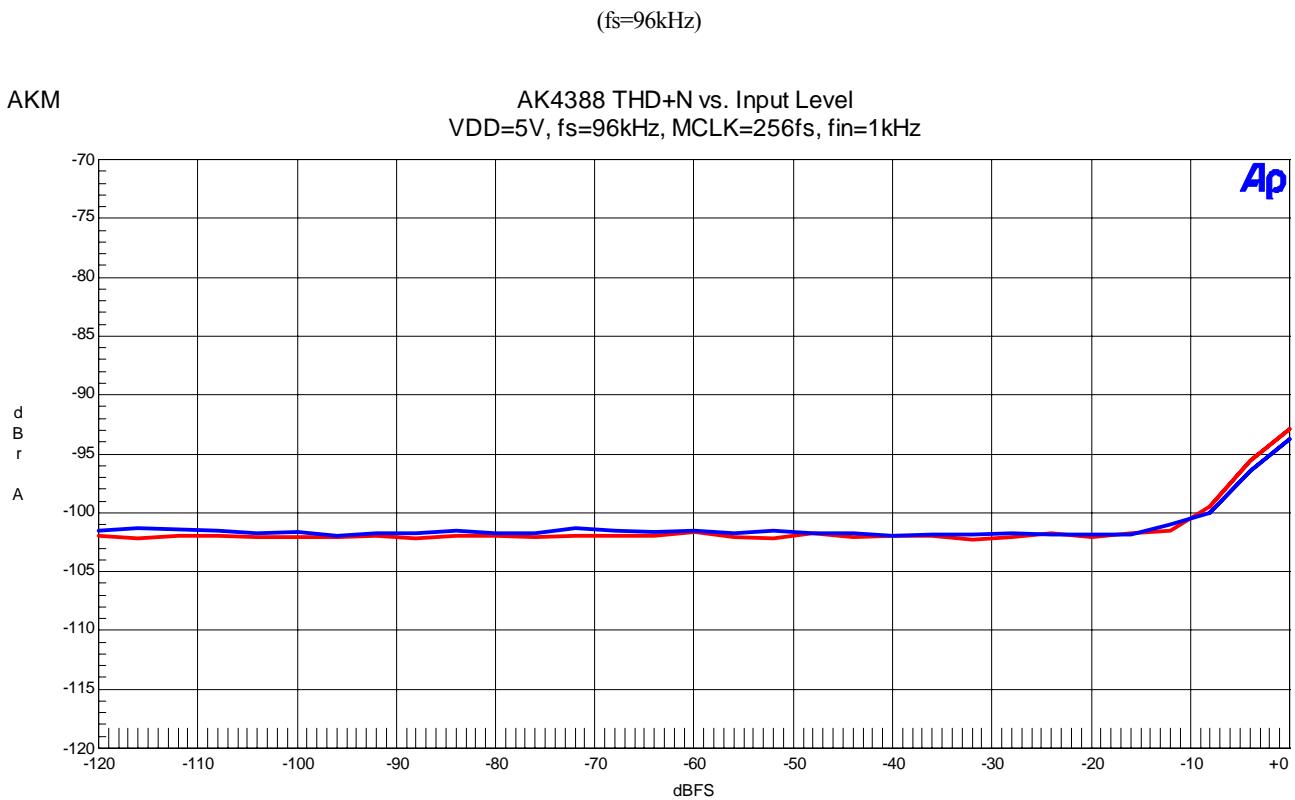


Figure 18. THD+N vs. Input level (fin=1kHz)

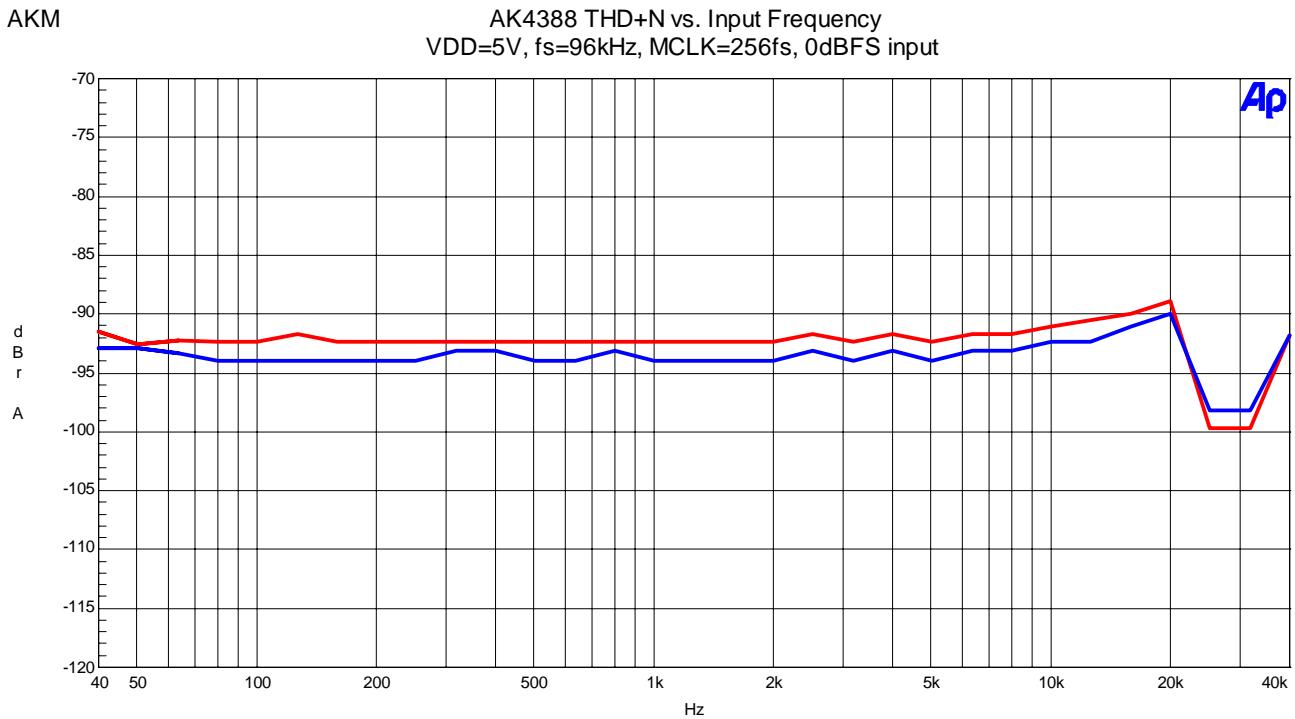


Figure 19. THD+N vs. Input Frequency (0dBFS input)

(fs=96kHz)

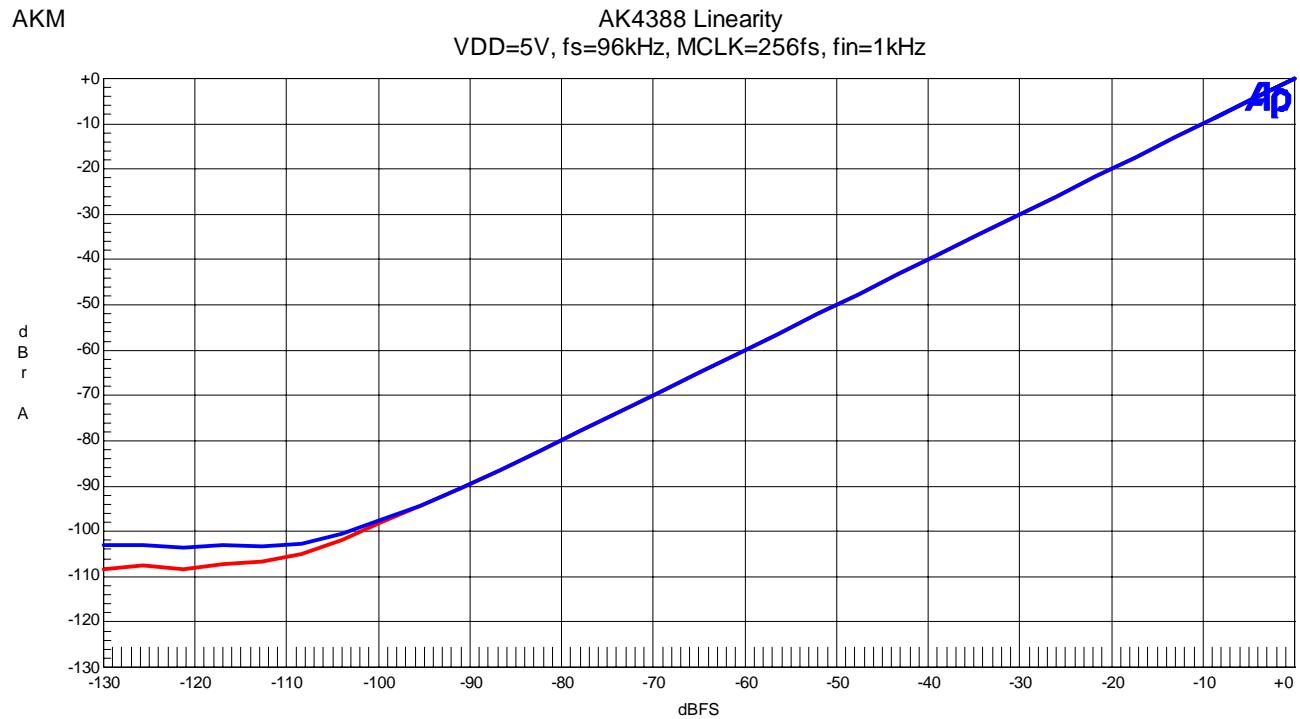


Figure 20. Linearity (fin=1kHz)

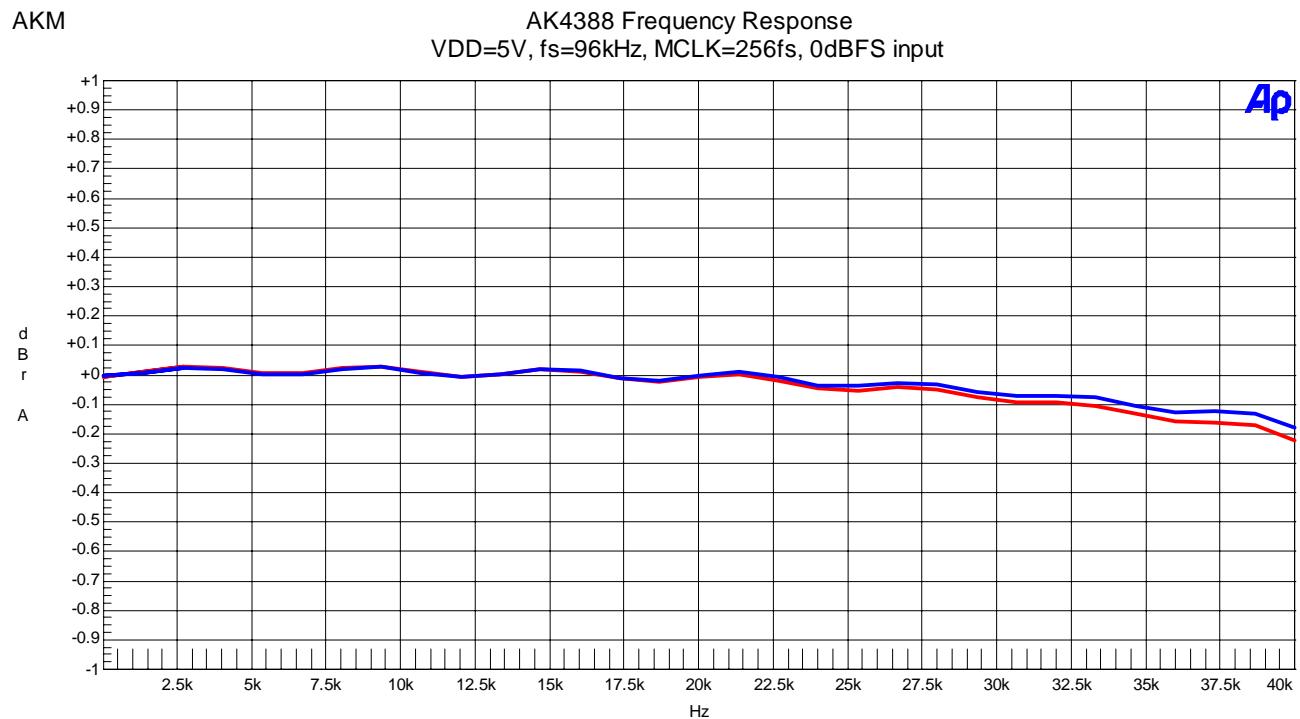


Figure 21. Frequency Response (0dBFS input)

(fs=96kHz)

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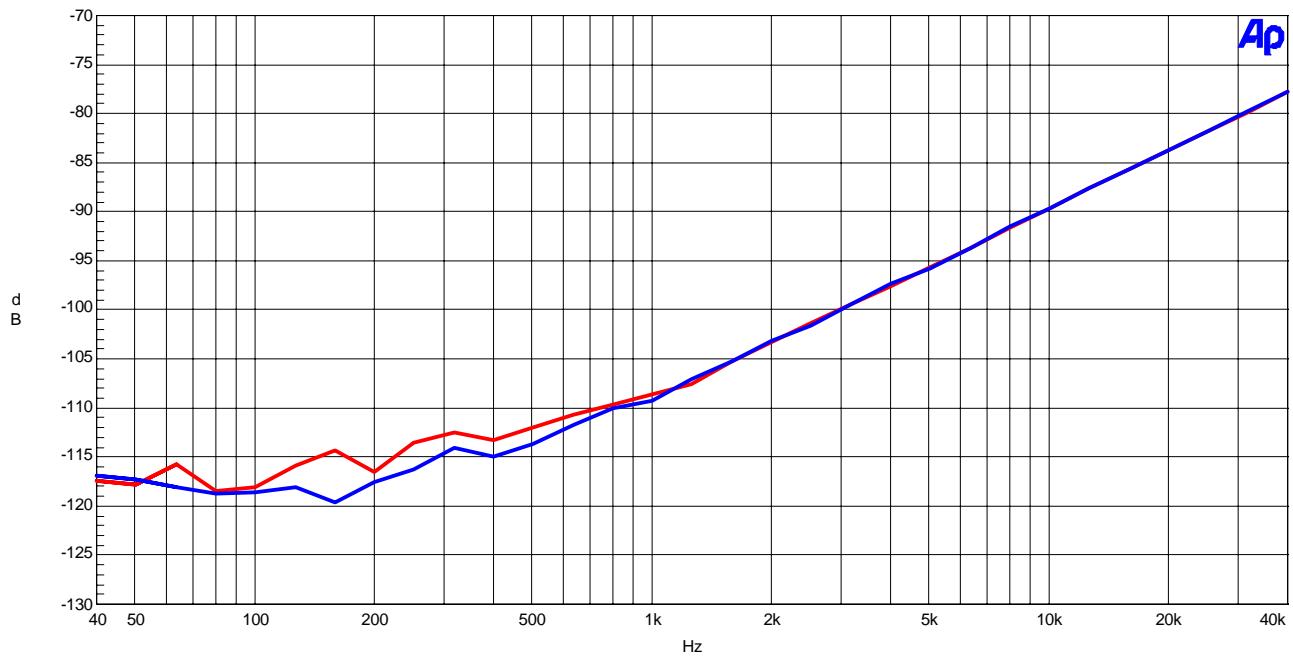
AK4388 Crosstalk (Red=Lch, Blue=Rch)
VDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input

Figure 22. Crosstalk (0dBFS input)

(fs=192kHz)

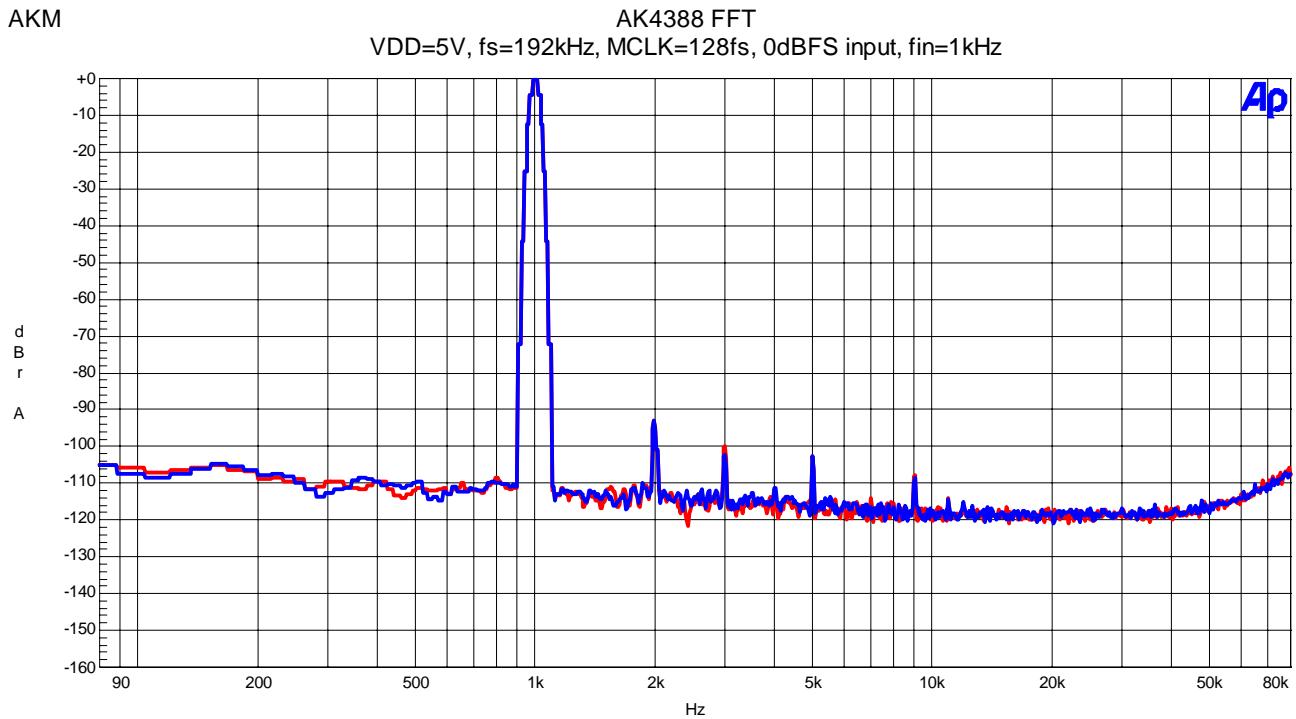


Figure 23. FFT (fin=1kHz, 0dBFS input)

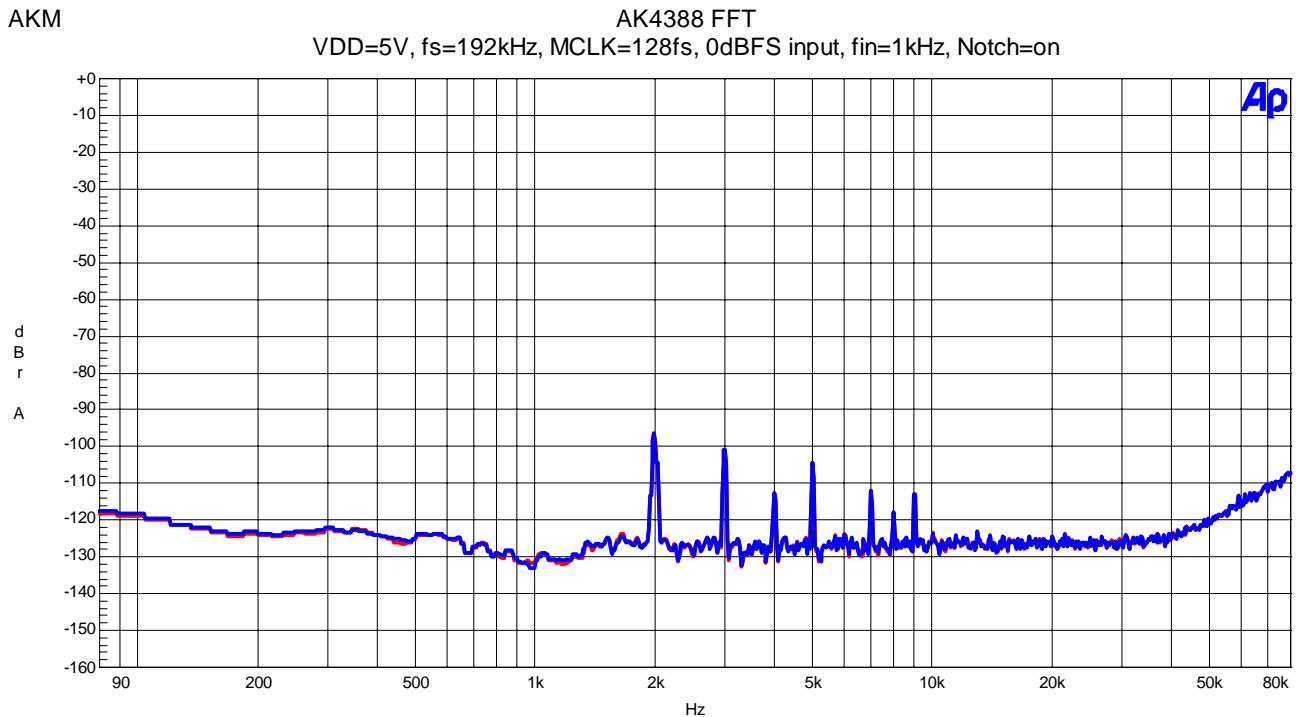


Figure 24. FFT(fin=1kHz, 0dBFS input, Notch)

(fs=192kHz)

AKM AK4388 FFT
VDD=5V, fs=192kHz, MCLK=128fs, -60dBFS input, fin=1kHz

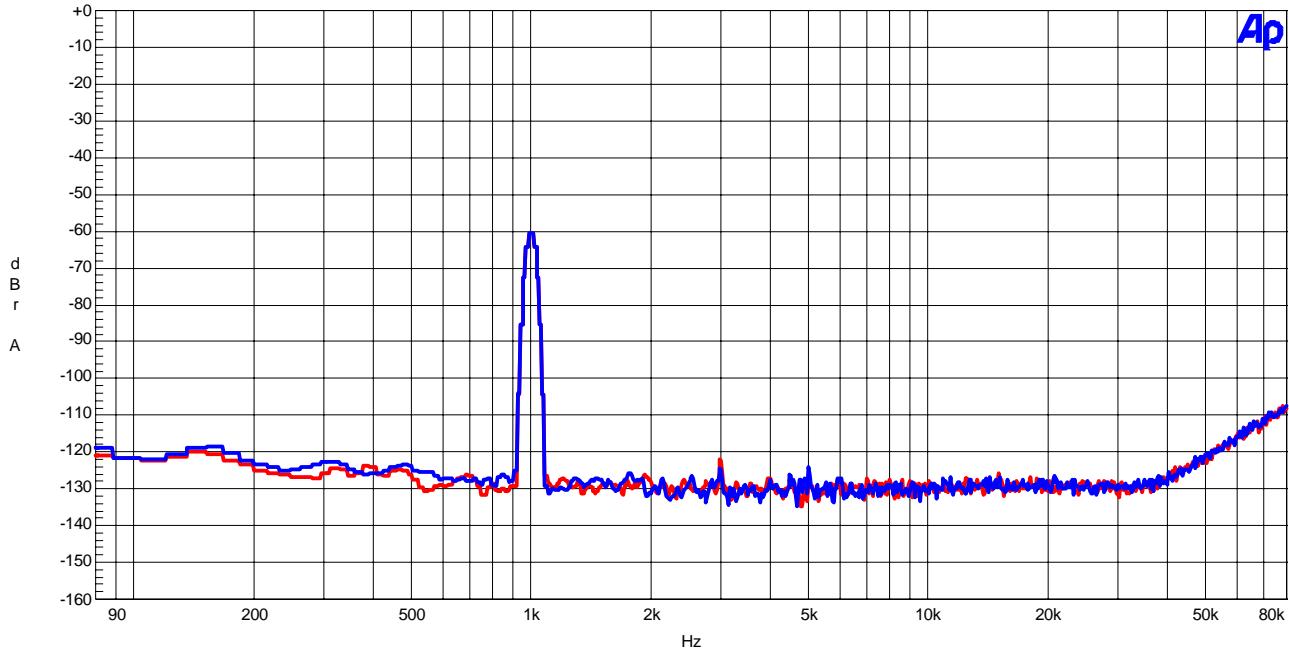


Figure 25. FFT (fin=1kHz, -60dBFS input)

AKM AK4388 FFT
VDD=5V, fs=192kHz, MCLK=128fs, fin=No signal

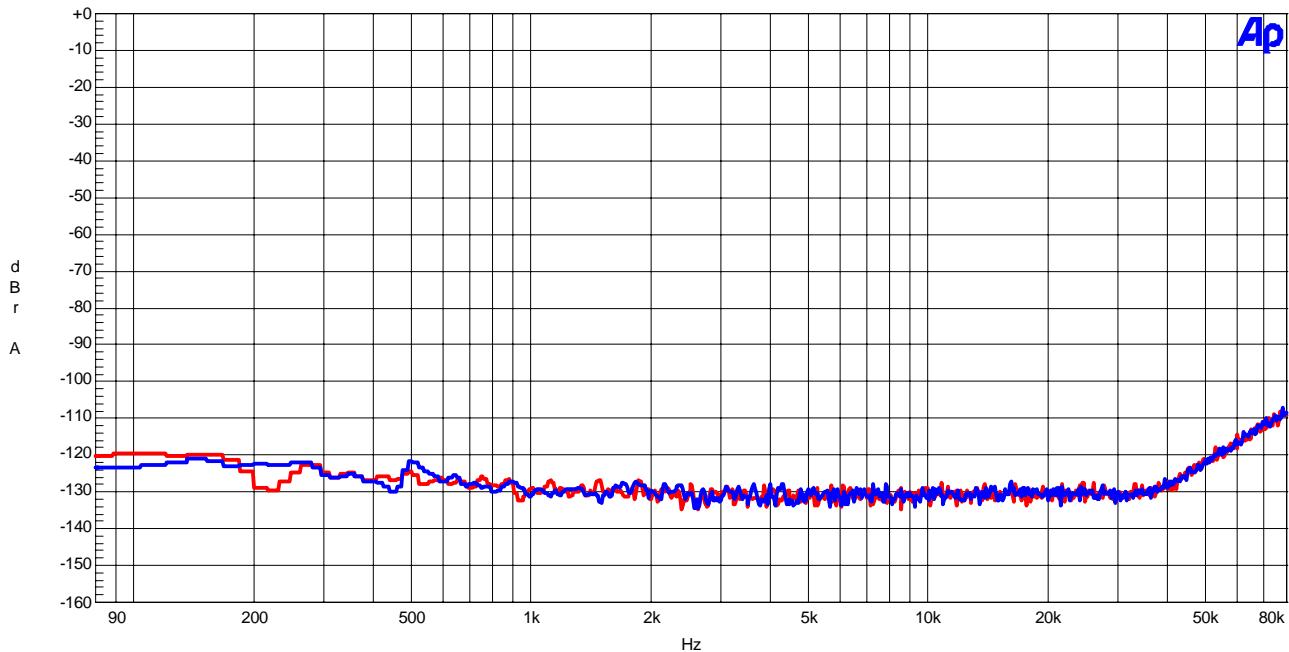


Figure 26. FFT (Noise Floor)

(fs=192kHz)

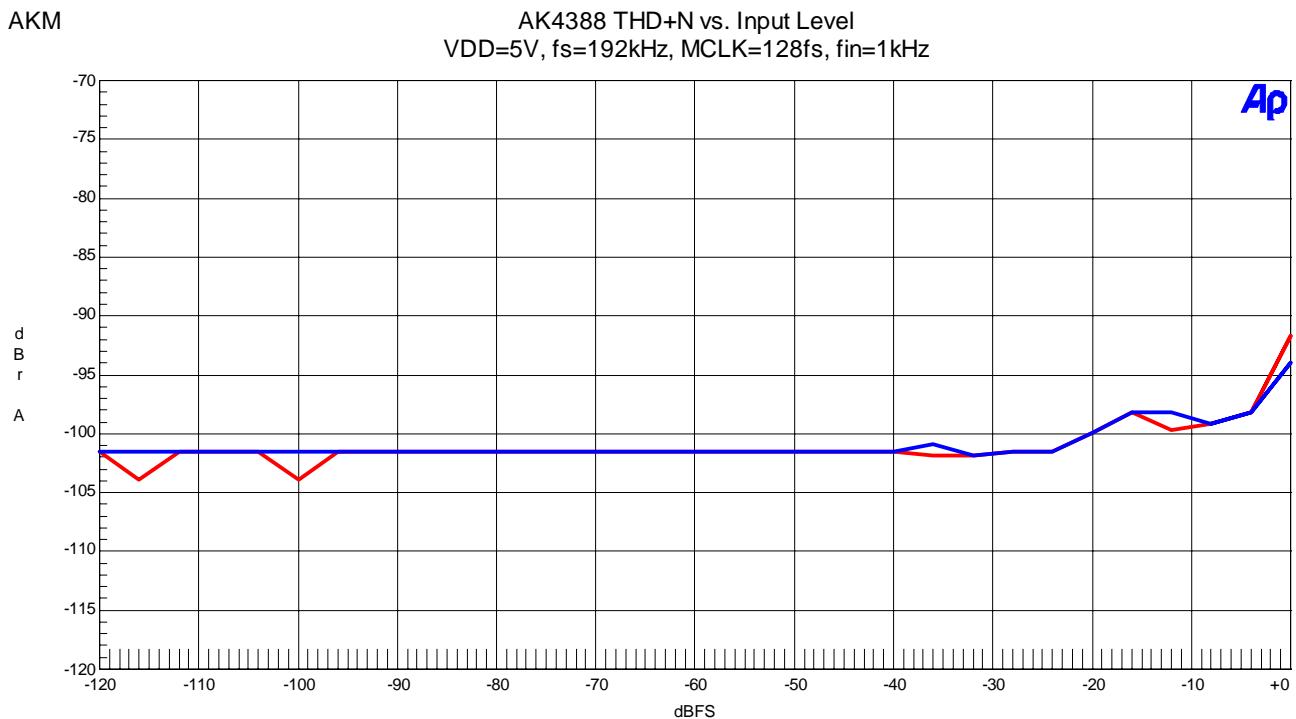


Figure 27. THD+N vs. Input level (fin=1kHz)

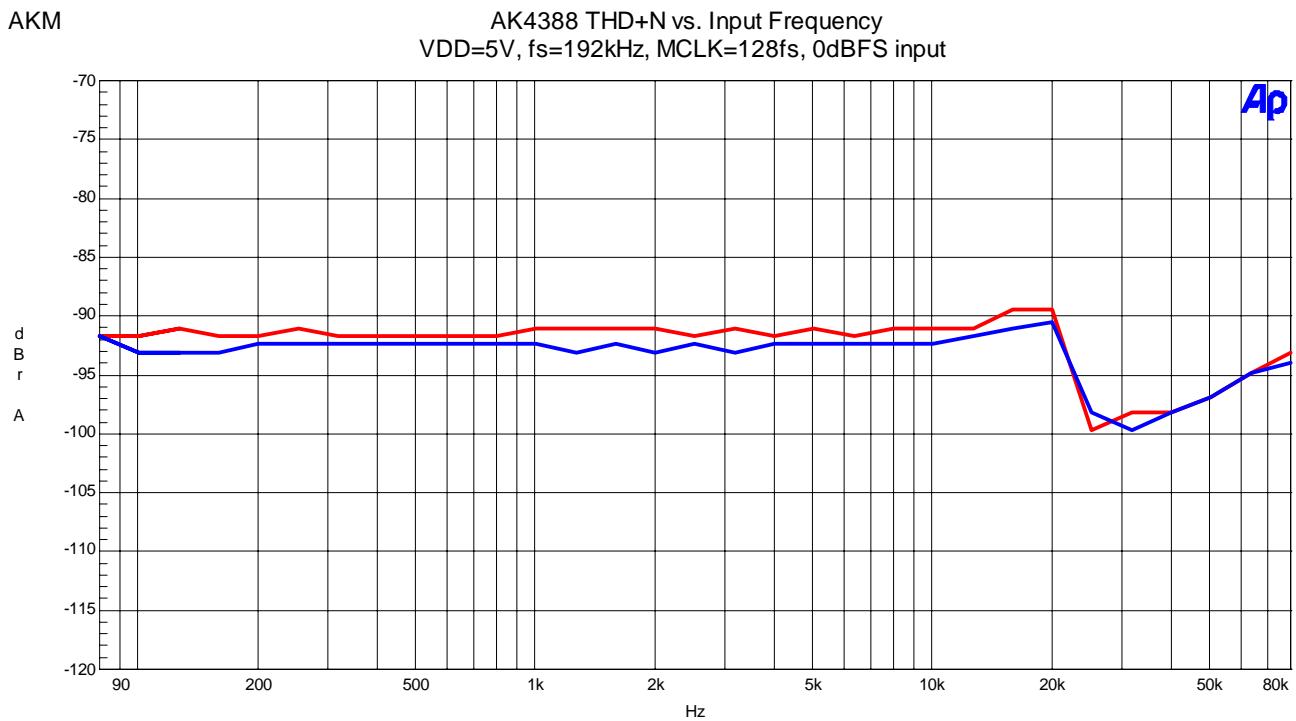


Figure 28. THD+N vs. Input Frequency (0dBFS input)

(fs=192kHz)

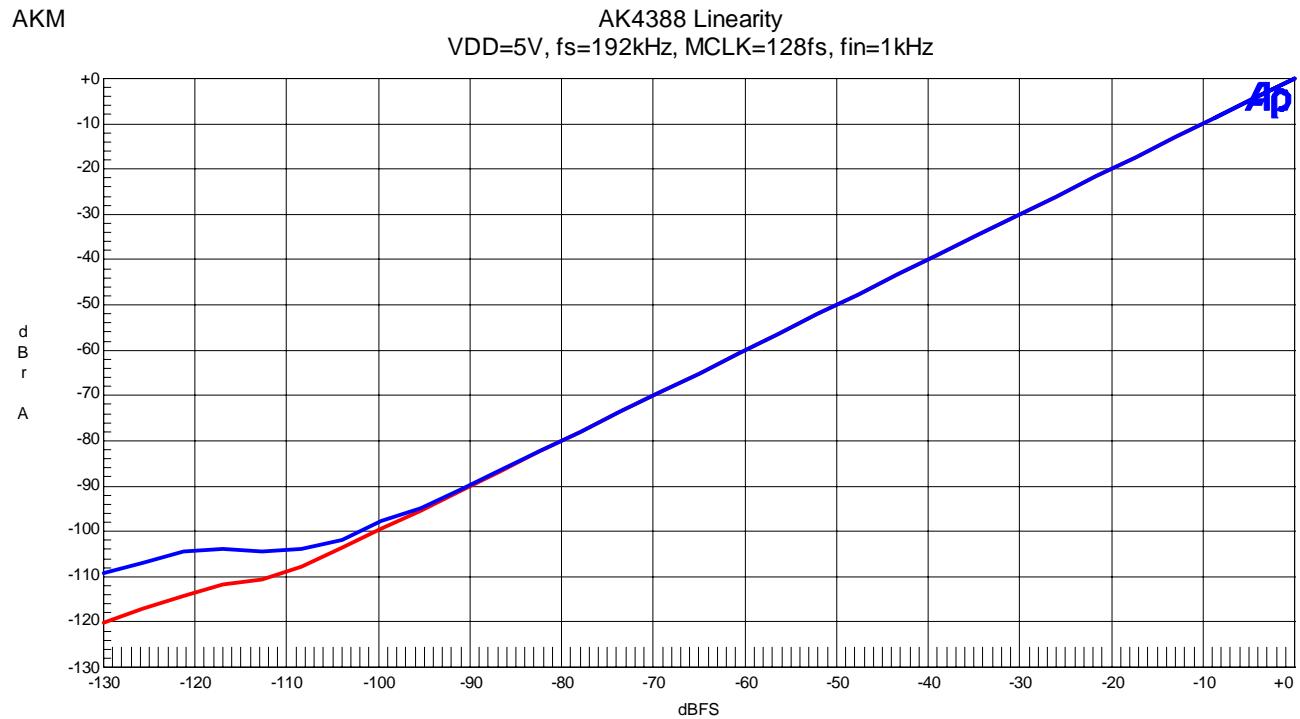


Figure 29. Linearity (fin=1kHz)

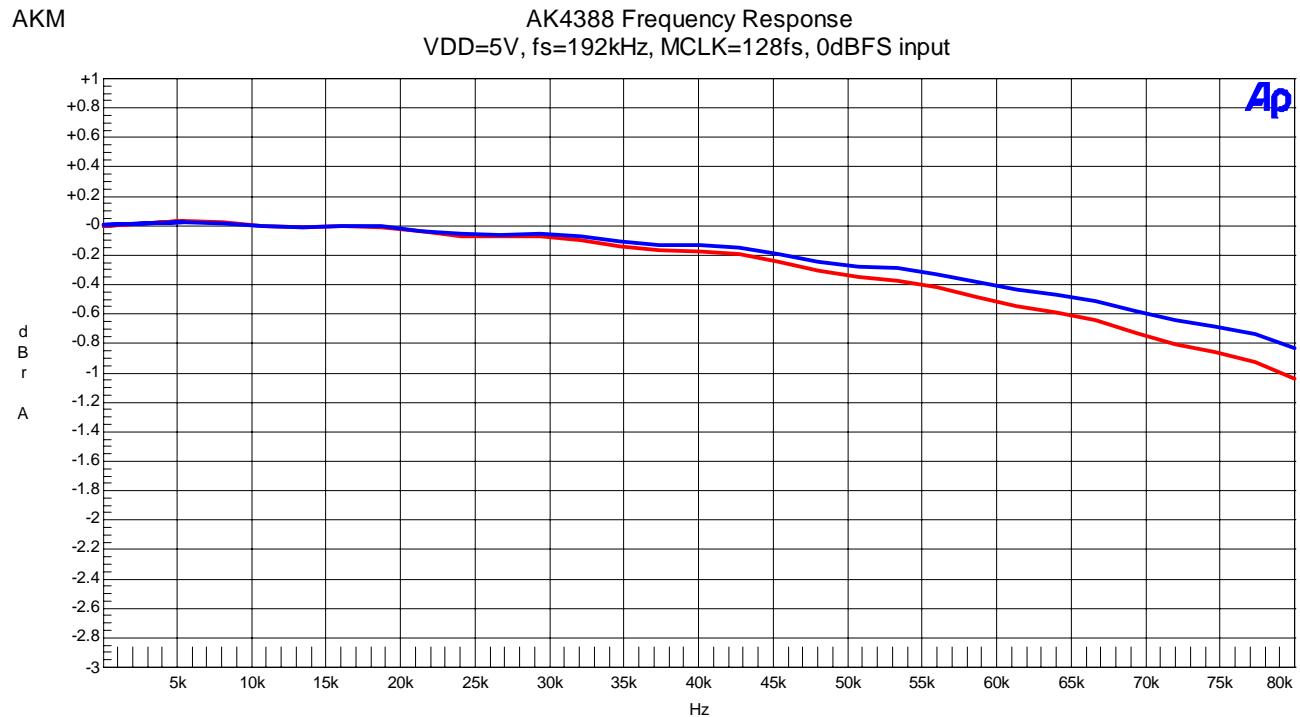


Figure 30. Frequency Response (0dBFS input)

(fs=192kHz)

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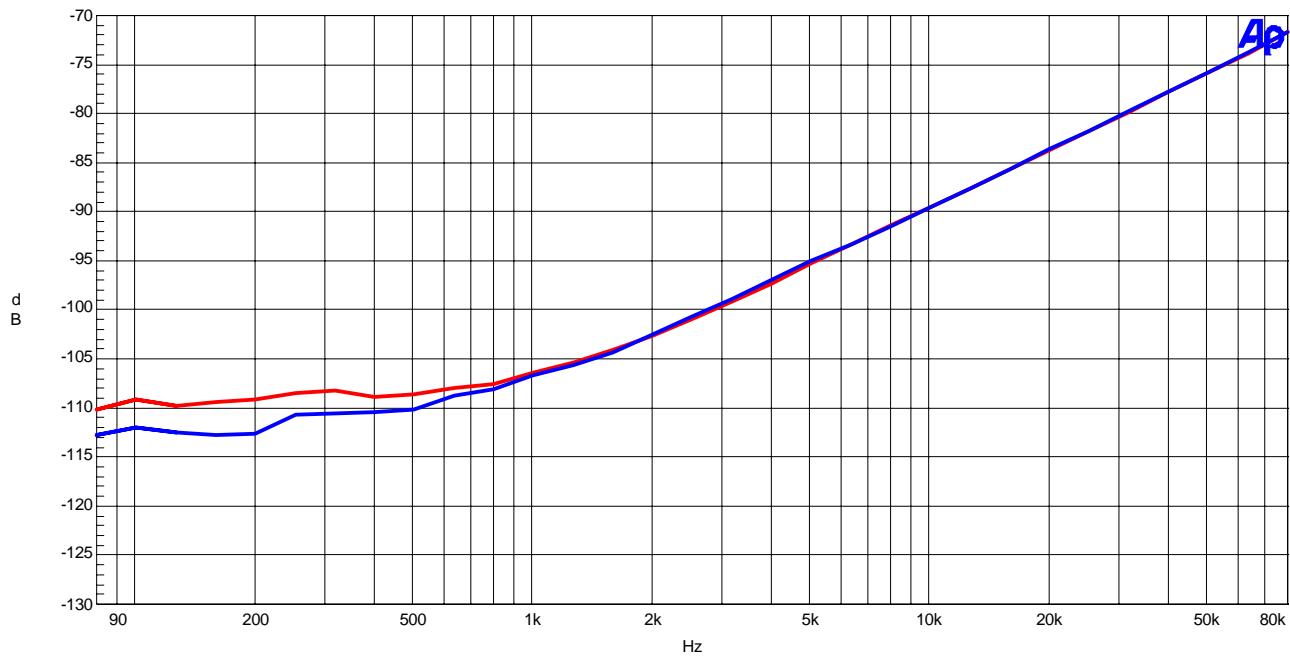
AK4388 Crosstalk (Red=Lch, Blue=Rch)
VDD=5V, fs=192kHz, MCLK=128fs, 0dBFS input

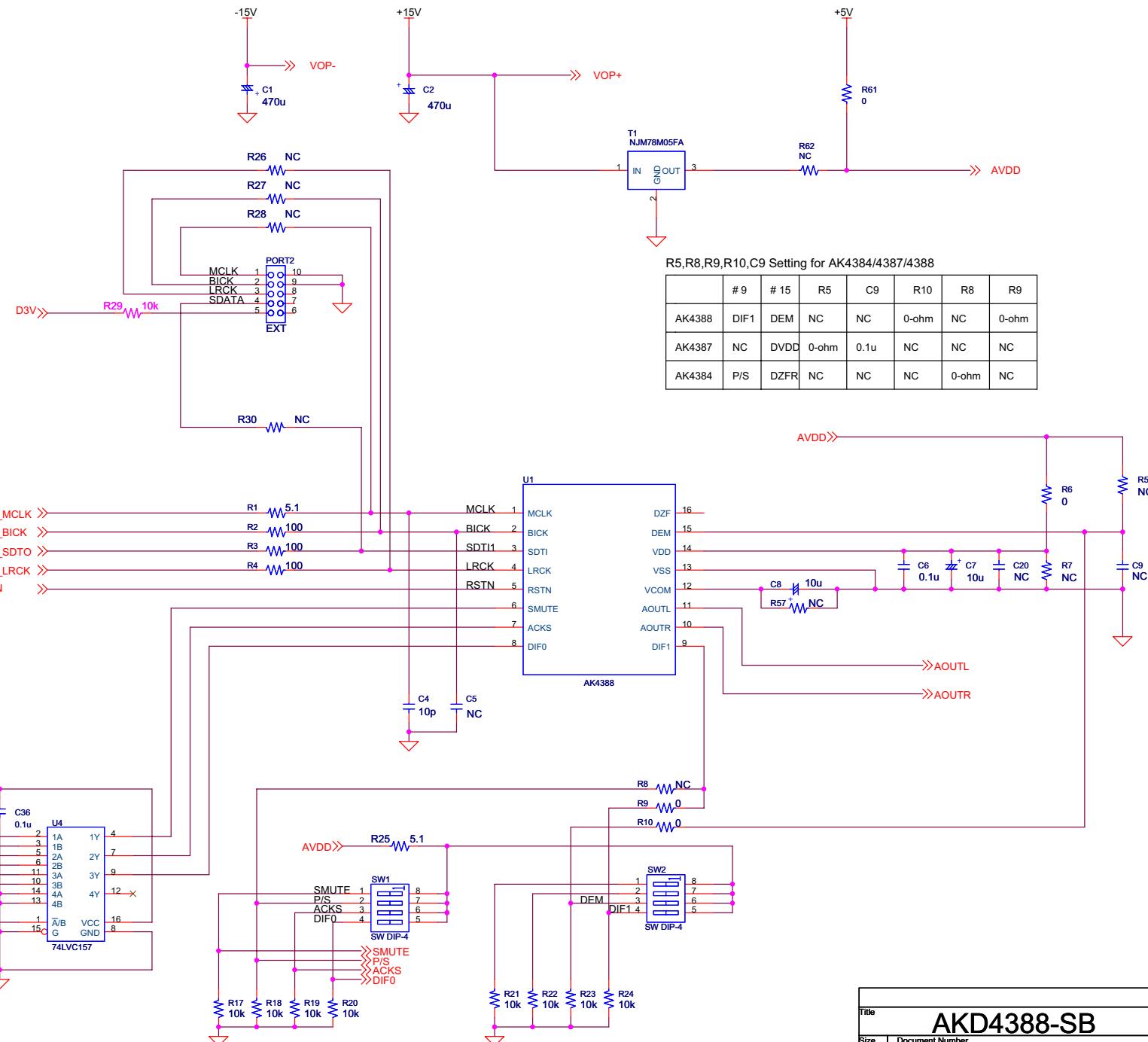
Figure 31. Crosstalk (0dBFS input)

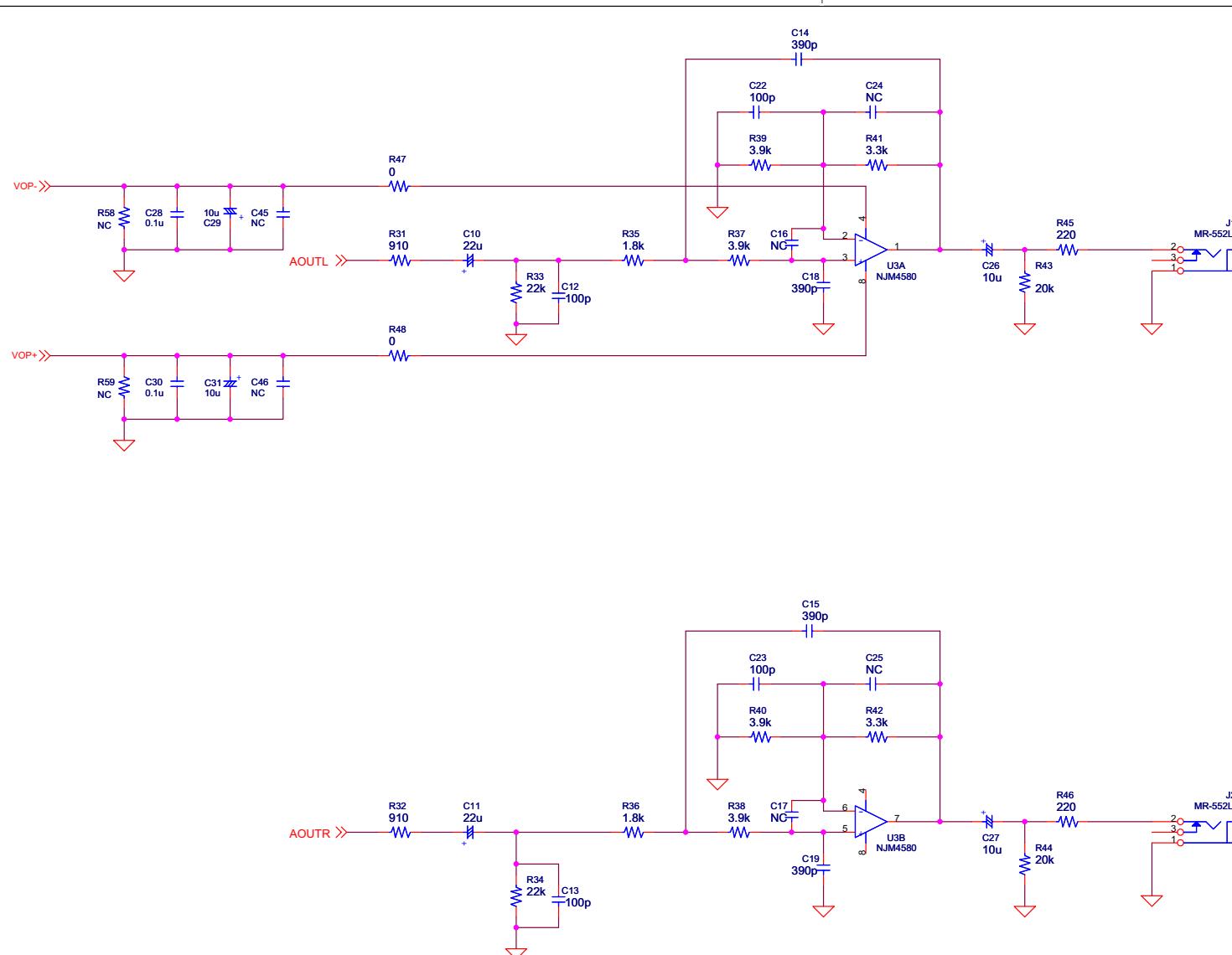
Revision History				
Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
06/05/16	KM083500	0	First edition	
06/06/06	KM083501	1	Change	GND pattern change.
06/09/28	KM083502	1	Error Correction	Error Correction P.4 : Table4 --> Table5

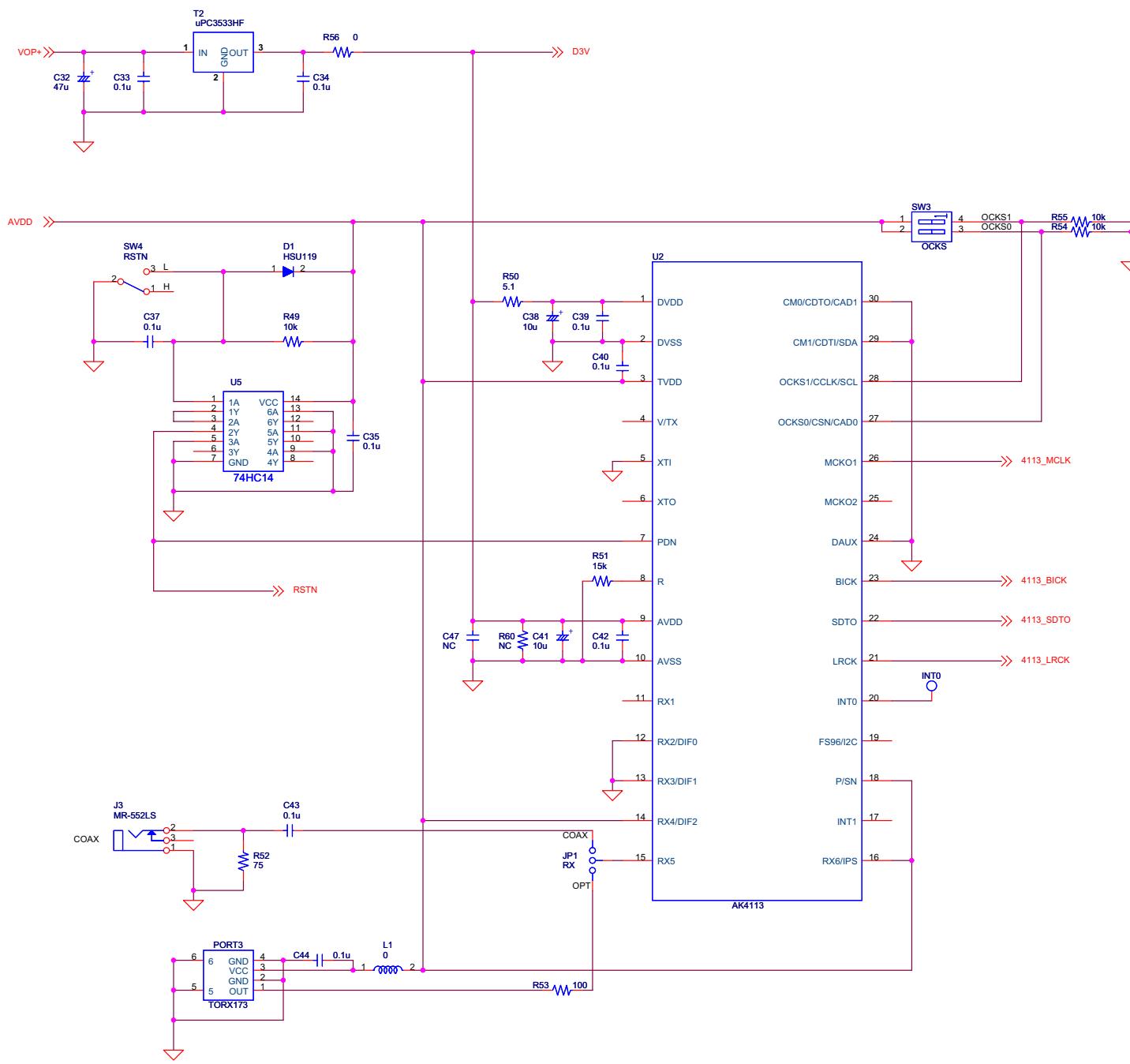
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Title		AKD4388-SB		
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Date: Tuesday, May 16, 2006				



S3

OCKS1	OCKS0	Master Clock
H	L	512fs@fs=32k/44.1k/48kHz
L	L	256fs@fs=88.2k/96kHz
H	H	128fs@fs=176.4k/192kHz