3 V/5 V, 12/14-Bit *nano*DAC™ D/A with 10 ppm/°C Max On-Chip Reference in SOT-23

Preliminary Technical Data

AD5620/AD5640

FEATURES

AD5620: low power single 12-bit *nano*DAC
AD5640: low power single 16-bit *nano*DAC
12-bit accuracy guaranteed
On-chip 1.25 V/2.5 V, 10 ppm/°C reference
Tiny 8-lead SOT-23/MSOP package
Power-down to 200 nA @ 5 V, 50 nA @ 3 V
3 V/5 V single power supply
Guaranteed 16-bit monotonic by design
Power-on reset to zero/midscale
3 power-down functions
Serial interface with Schmitt-triggered inputs
Rail-to-rail operation
SYNC interrupt facility

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

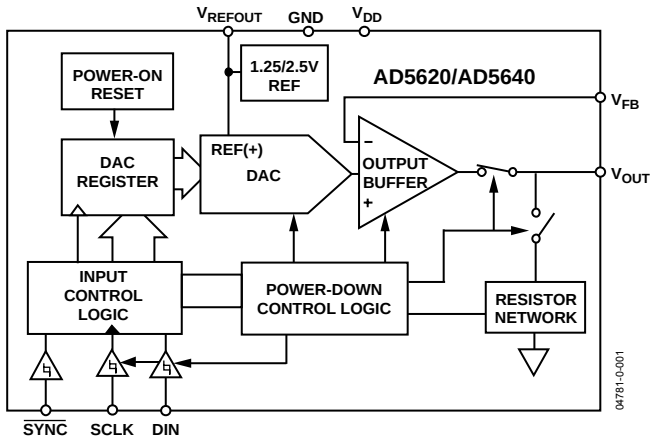

Figure 1.

GENERAL DESCRIPTION

The AD5620/40 parts are a member of the *nano*DAC family of devices. They are low power, single, 12-/14-bit buffered voltage-out DACs, guaranteed monotonic by design. The AD5620/40x-1 operate from a 3 V single supply featuring an internal reference of 1.25 V and an internal gain of 2. The AD5620/40x-2/3 operate from a 5 V single supply featuring an internal reference of 2.5 V and an internal gain of 2. Each reference has a 10 ppm/°C max temperature coefficient. The reference associated with each part is available at the REFOUT pin.

The part incorporates a power-on reset circuit, which ensures that the DAC output powers up to 0 V (AD5620/40x-1/2) or to midscale (AD5620/40x-3) and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 200 nA at 5 V and provides software selectable output loads while in power-down mode.

The AD5620/40 uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI™, QSPI™, MICROWIRE™, and DSP interface standards. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved.

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 0.7 mW at 5 V, reducing to 1 µW in power-down mode.

The AD5620/40 is designed with new technology and is the next generation to the AD53xx family.

RELATED DEVICES

Part No.	Description
AD5660	3 V/5 V 16-bit DAC in SOT-23, internal reference
AD5662	2.7 V to 5.5 V 16-bit DAC in SOT-23, external reference

PRODUCT HIGHLIGHTS

1. 16-bit DAC; 12-bit accuracy guaranteed.
2. On-chip 1.25 V/2.5 V, 10 ppm/°C max reference.
3. Available in 8-lead SOT-23 and 8-lead MSOP packages.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 50 nA at 3 V and 200 nA at 5 V.
6. 10 µS settling time.

Rev. PrA

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REVISION HISTORY

10/04—Revision 0: PrA

AD5620/40X-2/3–SPECIFICATIONS

V_{DD} = +4.5 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Grade	B Grade	C Grade	Unit	B Version [1] Conditions/Comments
STATIC PERFORMANCE[2]					
AD5620					
Resolution	12	12	12	Bits min	
Relative Accuracy	±6	±1	±1	LSB max	See Figure 4.
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design. See Figure 5.
AD5640					
Resolution	14	14	14	Bits min	
Relative Accuracy	±8	±4	±4	LSB max	See Figure 4.
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design. See Figure 5.
Zero Code Error	+5	+5	+5	mV typ	All 0s loaded to DAC register.
	+20	+20	+20	mV max	
Offset Error	±10	±10	±10	mV typ	
Full-Scale Error	−0.15	−0.15	−0.15	% of FSR typ	All 1s loaded to DAC register.
	−1.25	−1.25	−1.25	% of FSR max	
Gain Error	±1.25	±1.25	±1.25	% of FSR max	
Zero Code Error Drift[3]	±2	±2	±2	µV/°C typ	
Gain Temperature Coefficient	±2.5	±2.5	±2.5	ppm typ	Of FSR/°C
DC Power Supply Rejection Ratio	−100	−100	−100	dB typ	DAC code = midscale; V_{DD} = 5 V ±10%
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0	0		V min	
	V_{DD}	V_{DD}	V_{DD}	V max	
Output Voltage Settling Time	8	8	8	µs typ	To ±0.003% FSR 0x0200 to 0xFD00
	10	10	10	µs max	R_L = 2 kΩ; 0 pF < C_L < 200 pF
	12	12	12	µs typ	R_L = 2 kΩ; C_L = 500 pF
Slew Rate	1	1	1	V/µs typ	
Capacitive Load Stability	2	2	2	nF typ	R_L = ∞
	10	10	10	nF typ	R_L = 2 kΩ
Output Noise Spectral Density	80	80	80	nV/√Hz typ	DAC code = midscale, 10kHz
Output Noise (0.1 Hz to 10 Hz)	10	10	10	µVp-p typ	DAC code = midscale
THD, Total Harmonic Distortion	−80	−80	−80	dB typ	V_{REF} = 2 V ± 300 mV p-p, f = 5 kHz
Output Drift				ppm/°C typ	
Digital-to-Analog Glitch Impulse	5	5	5	nV-s typ	1 LSB change around major carry.
Digital Feedthrough	0.1	0.1	0.1	nV-s typ	
DC Output Impedance	0.5	0.5	0.5	Ω typ	
Short Circuit Current	30	30	30	mA typ	V_{DD} = 5 V
Power-Up Time	4	4	4	µs typ	Coming out of power-down mode. V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage					
AD5620/40x-2/3	2.495	2.495	2.495	V min	
	2.505	2.505	2.505	V max	
Reference TC	±25	±25	±10	ppm/°C max	
LOGIC INPUTS[3]					
Input Current	±1	±1	±1	µA max	

[1] Temperature ranges are as follows: B Version: -40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of 512 to 65024. Output unloaded.
[3] Guaranteed by design and characterization, not production tested.

Parameter	A Grade	B Grade	C Grade	Unit	B Version [1] Conditions/Comments
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	V_{DD} = 5 V
V_{INH}, Input High Voltage	2	2	2	V min	V_{DD} = 5 V
Pin Capacitance	3	3	3	pF max	
POWER REQUIREMENTS					
V_{DD}	4.5	4.5	4.5	V min	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)	5.5	5.5	5.5	V max	DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V	0.5	0.5	0.5	mA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V	1	1	1	mA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 4.5 V to 5.5 V	0.2	0.2	0.2	µA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V	1	1	1	µA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}	89	89	89	%	I_{LOAD} = 2 mA, V_{DD} = 5 V

AD5620/40X-1–SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade	B Grade	C Grade	Unit	B Version [4] Conditions/Comments
STATIC PERFORMANCE[5]					
AD5620					
Resolution	12	12	12	Bits min	
Relative Accuracy	±6	±1	±1	LSB max	See Figure 4.
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design. See Figure 5.
AD5640					
Resolution	14	14	14	Bits min	
Relative Accuracy	±8	±4	±4	LSB max	See Figure 4.
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed monotonic by design. See Figure 5.
Zero Code Error	+5	+5	+5	mV typ	All 0s loaded to DAC register
	+20	+20	+20	mV max	
Offset Error	±10	±10	±10	mV typ	
Full-Scale Error	−0.15	−0.15	−0.15	% of FSR typ	All 1s loaded to DAC register.
	−1.25	−1.25	−1.25	% of FSR max	
Gain Error	±1.25	±1.25	±1.25	% of FSR max	
Zero Code Error Drift[6]	±20	±20	±20	µV/°C typ	
Gain Temperature Coefficient	±5	±5	±5	ppm typ	Of FSR/°C
DC Power Supply Rejection Ratio	−100	−100	−100	dB typ	DAC code = midscale; V_{DD} = 3 V ±10%
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0	0		V min	
	V_{DD}	V_{DD}	V_{DD}	V max	
Output Voltage Settling Time	8	8	8	µs typ	To ±0.003% FSR 0200_H to $FD00_H$
	10	10	10	µs max	R_L = 2 kΩ; 0 pF < C_L < 200 pF.
	12	12	12	µs typ	R_L = 2 kΩ; C_L = 500 pF
Slew Rate	1	1	1	V/µs typ	
Capacitive Load Stability	2	2	2	nF typ	R_L = ∞
	10	10	10	nF typ	R_L = 2 kΩ
Output Noise Spectral Density	80	80	80	nV/√Hz typ	DAC code = midscale, 10 kHz
Output Noise (0.1 Hz to 10 Hz)	10	10	10	µVp-p typ	DAC code = midscale
THD, Total Harmonic Distortion	−80	−80	−80	dB typ	V_{REF} = 2 V ± 300 mV p-p, f = 5 kHz
Output Drift		tbd		ppm/°C typ	
Digital-to-Analog Glitch Impulse	5	5	5	nV-s typ	1 LSB change around major carry.
Digital Feedthrough	0.1	0.1	0.1	nV-s typ	
DC Output Impedance	0.5	0.5	0.5	Ω typ	
Short Circuit Current	30	30	30	mA typ	V_{DD} = 3 V
Power-Up Time	10	10	10	µs typ	Coming out of power-down mode. V_{DD} = 3 V
REFERENCE OUTPUT					
Output Voltage					
AD5620/40x-1	1.248	1.248	1.248	V min	
	1.252	1.252	1.252	V max	
Reference TC	±25	±25	±10	ppm/°C max	

[4] Temperature ranges are as follows: B Version: -40°C to +105°C, typical at 25°C.
[5] Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.
[6] Guaranteed by design and characterization, not production tested.

Parameter	A Grade	B Grade	C Grade	Unit	B Version [4] Conditions/Comments
LOGIC INPUTS[3]					
Input Current	±1	±1	±1	μA max	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2	2	2	V min	V_{DD} = 3 V
Pin Capacitance	3	3	3	pF max	
POWER REQUIREMENTS					
V_{DD}	2.7	2.7	2.7	V min	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)	3.6	3.6	3.6	V max	DAC active and excluding load current
V_{DD} = 2.7 V to 3.6 V	0.5	0.5	0.5	mA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V	1	1	1	mA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = 2.7 V to 3.6 V	0.2	0.2	0.2	μA typ	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V	1	1	1	μA max	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}					I_{LOAD} = 2 mA, V_{DD} = 3 V

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
See Figure 2.
V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

	Limit at T_{MIN}, T_{MAX}			
Parameter	**V_{DD} = 2.7 V to 3.6 V**	**V_{DD} = 3.6 V to 5.5 V**	**Unit**	**Conditions/Comments**
t_1 [7]	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	13	13	ns min	SCLK low time
t_4	0	0	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	50	33	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	13	ns min	$\overline{SYNC}$ rising edge to SCLK fall ignore
t_{10}	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore

[7] Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

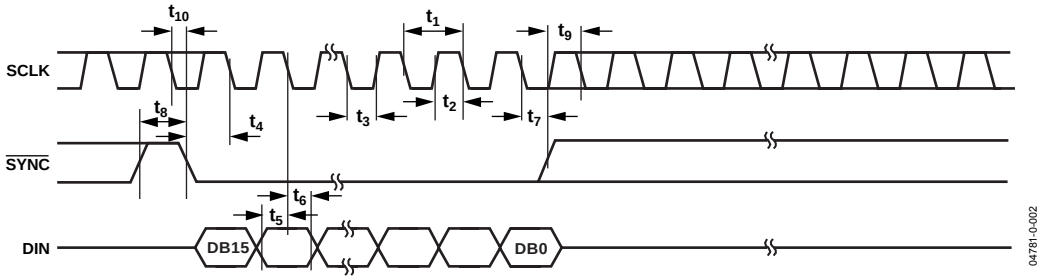

Figure 2. Serial Write Operation

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

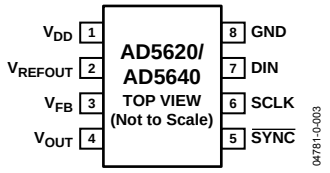

Figure 3. 8-Lead S0T-23/MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V, and V_{DD} should be de-coupled to GND.
2	V_{REFOUT}	Reference Voltage Output.
3	V_{FB}	Feedback Connection for the Output Amplifier.
4	V_{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle, unless $\overline{SYNC}$ is taken high before this edge; in which case, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC.
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
7	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	GND	Ground Reference Point for All Circuitry on the Part.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
SOT-23 Package	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 4.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 5.

Zero-Code Error
It is a measure of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5620/AD5640 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of the zero-code error vs. temperature can be seen in Figure 8.

Full-Scale Error
It is a measure of the output error when full-scale code (0xFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of the full-scale error vs. temperature can be seen in Figure 8.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error (TUE)
TUE is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 6.

Zero-Code Error Drift
This is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
It is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FF to 0x800). See Figure 21.

Digital Feedthrough
It is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

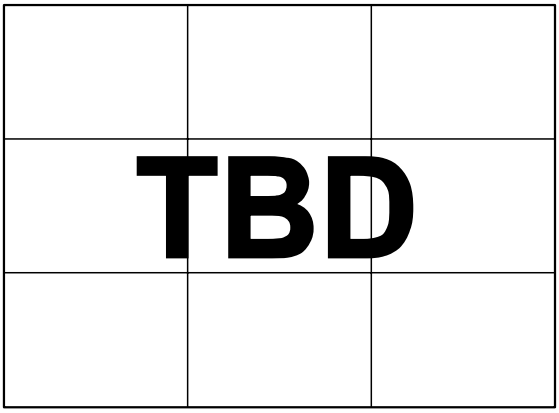

Figure 4. AD5620 Typical INL Plot

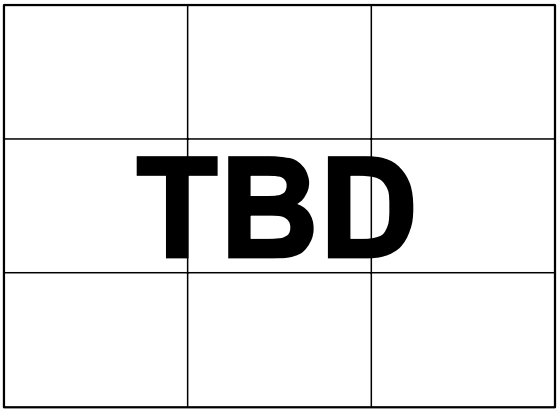

Figure 7. INL Error and DNL Error vs. Temperature

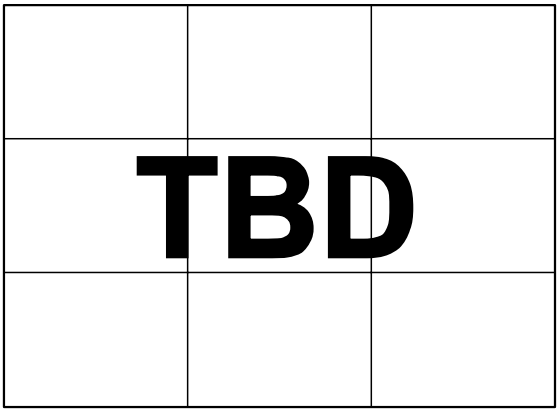

Figure 5. AD5620 Typical DNL Plot

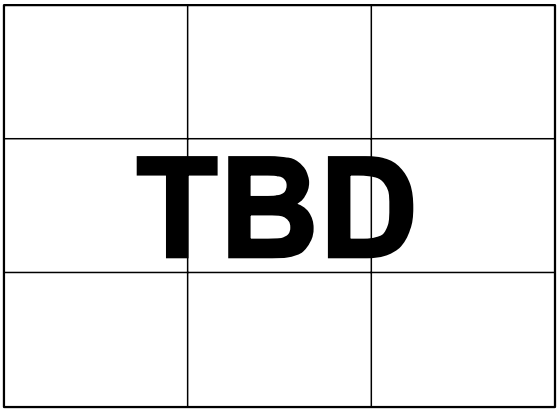

Figure 8. Zero-Scale Error and Full-Scale Error vs. Temperature

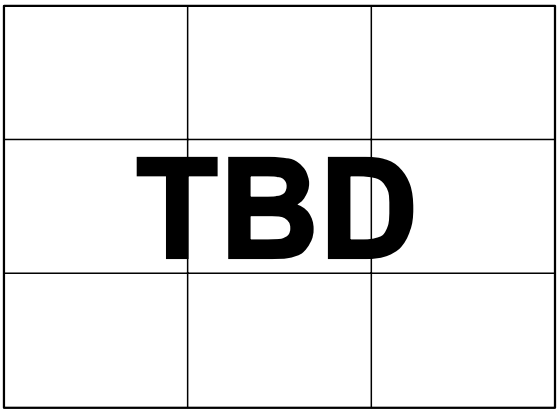

Figure 6. AD5620 Typical Total Unadjusted Error (TUE) Plot

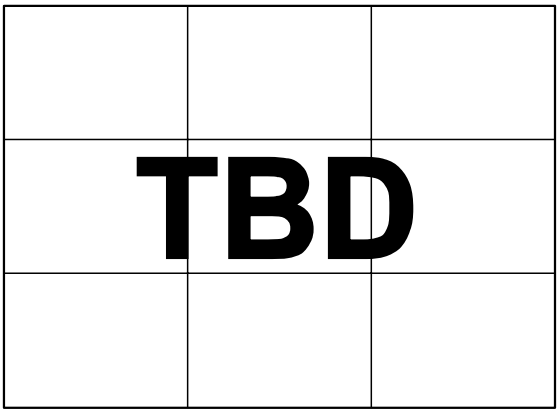

Figure 9. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

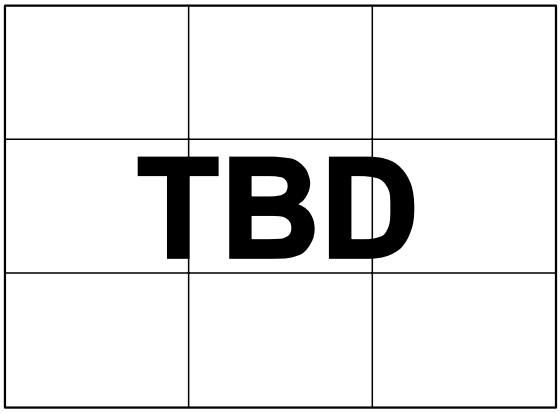

Figure 10. Source and Sink Current Capability with V_{DD} = 3 V

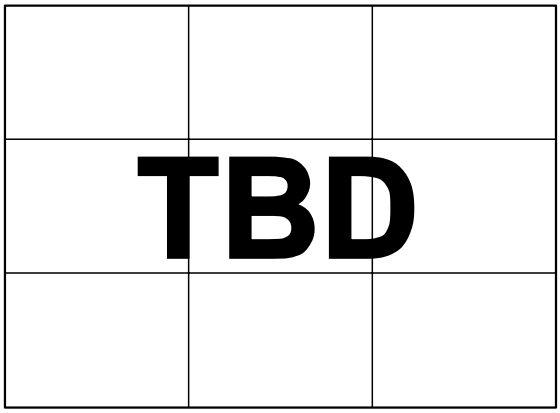

Figure 13. Supply Current vs. Temperature

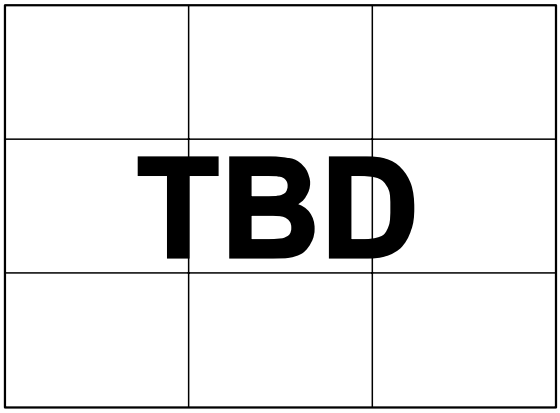

Figure 11. Source and Sink Current Capability with V_{DD} = 5 V

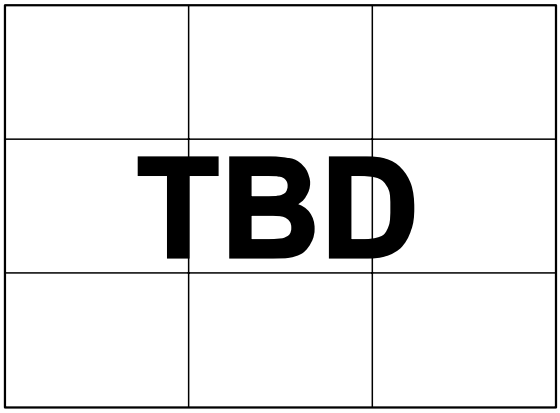

Figure 14. Supply Current vs. Supply Voltage

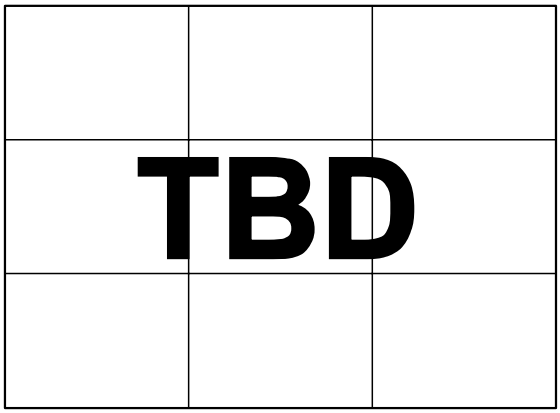

Figure 12. Supply Current vs. Code

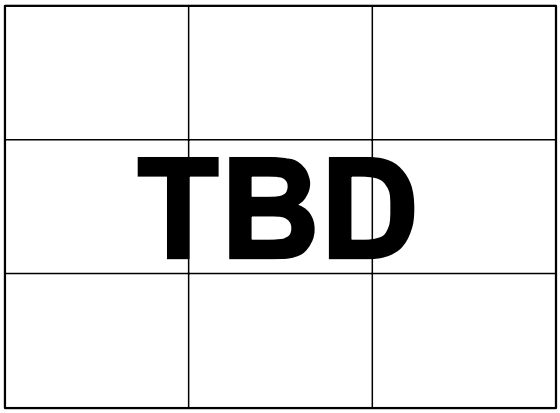

Figure 15. Power-Down Current vs. Supply Voltage

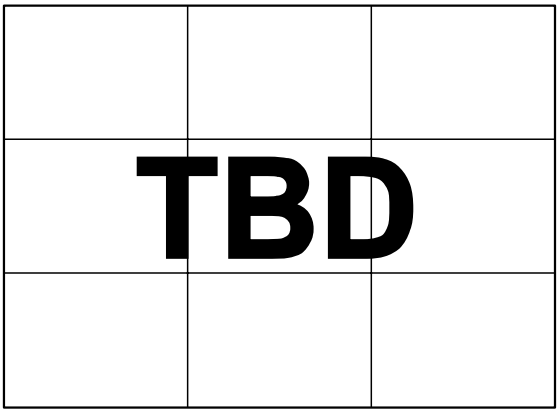

Figure 16. Supply Current vs. Logic Input Voltage

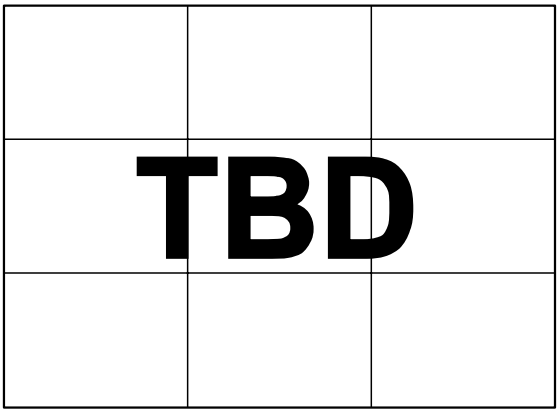

Figure 19. Power-On Reset to 0 V

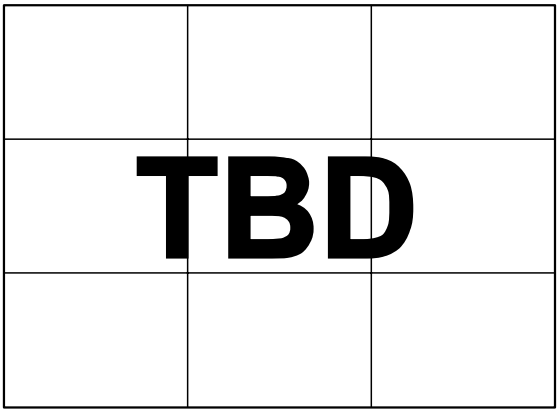

Figure 17. Full-Scale Settling Time

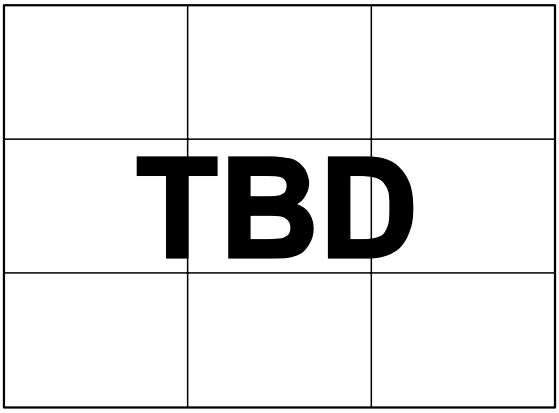

Figure 20. Exiting Power-Down (0x800 Loaded)

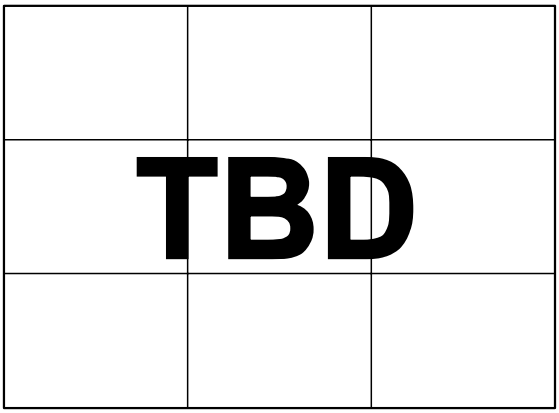

Figure 18. Half-Scale Settling Time

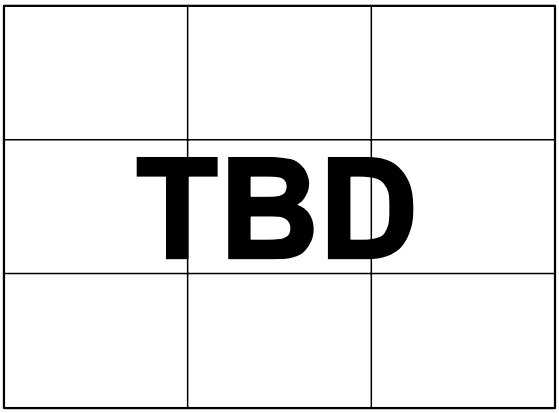

Figure 21. Digital-to-Analog Glitch Impulse

THEORY OF OPERATION

D/A Section

The AD5620/AD5640 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. The parts include an internal 1.25 V/2.5 V, 10 ppm/°C reference with an internal gain of 2. Figure 22 shows a block diagram of the DAC architecture.

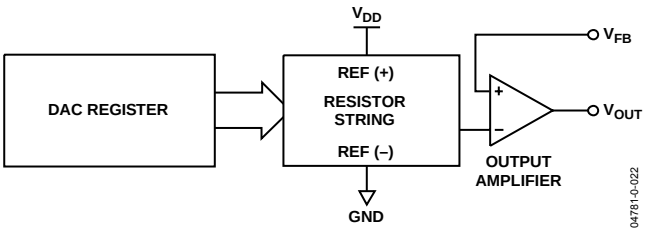

Figure 22. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = 2 \times VREF \times \left(\frac{D}{65536} \right)$$

where:
D equals the decimal equivalent of the binary code that is loaded to the DAC register; 0 – 4095 for AD5620 (12 bit) and 0 – 16383 for AD5640 (14 bit).
N equals the DAC resolution.

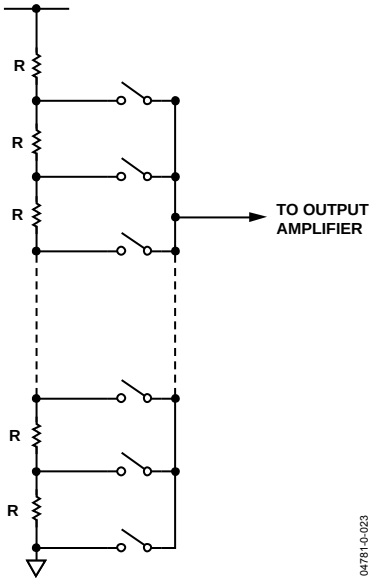

Figure 23. Resistor String

Resistor String

The resistor string section is shown in Figure 23. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 10 and Figure 11. The slew rate is 1 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5620/AD5640 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN), which is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5620/AD5640 compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, i.e., a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{\text{SYNC}}$ line can be kept low or can be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Since the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 2.4 V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned previously, however, it must be brought high again just before the next write sequence.

Input Shift Register

The input shift register is 16 bits wide (see Figure 24 and Figure 25). The first two bits are control bits, which control the mode of operation that the part is in (normal mode or any one of the three power-down modes). For a more complete description of the various modes, see the Power-Down Modes section. The next 14/12 bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

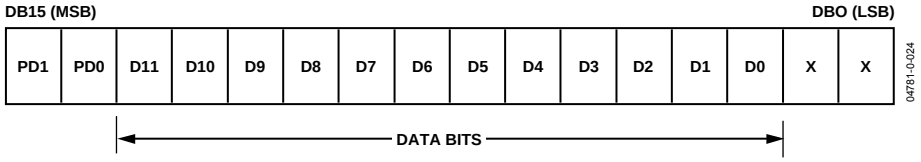

Figure 24. AD5620 Input Register Contents

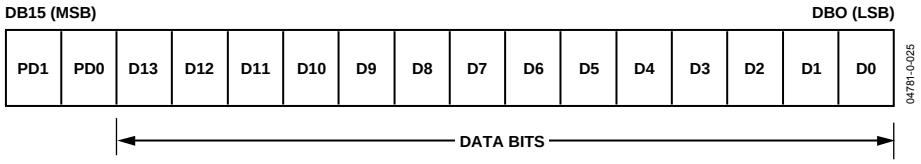

Figure 25. AD5640 Input Register Contents

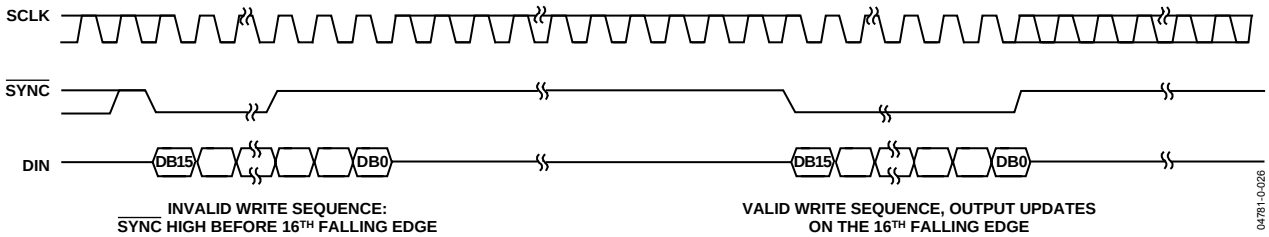

Figure 26. $\overline{SYNC}$ Interrupt Facility

$\overline{SYNC}$ Interrupt

In a normal write sequence, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK, and the DAC is updated on the 16th falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs (see Figure 26).

Power-On Reset

The AD5620/AD5640 family contains a power-on-reset circuit, which controls the output voltage during power-up. The AD5620/AD5640x-1/AD5620/AD5640x-2 DAC output powers up to 0 V, and the AD5620/AD5640x-3 DAC output powers up to midscale. The output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Power-Down Modes

The AD5620/AD5640 family contains four separate modes of operation. These modes are software-programmable by setting two bits, DB15 and DB14, in the control register. Table 6 shows how the state of the bits corresponds to the mode of operation of the device.

Table 6. Modes of Operation for the AD5620/AD5640

Operating Mode	DB15	DB14
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
100 kΩ to GND	1	0
Three-State	1	1

When both bits are set to 0, the part works normally with its normal power consumption of 250 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V and to 0 nA at 3 V. Not only does the supply current fall, but the output stage is internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or left open-circuited (three-state). The output stage is illustrated in Figure 27.

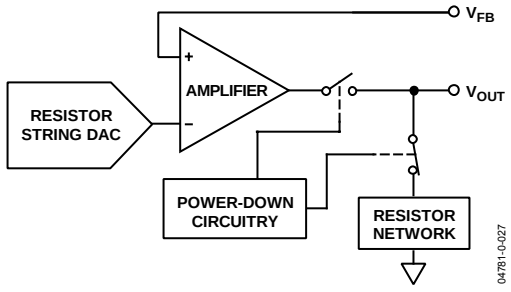

Figure 27. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and the other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and 5 µs for V_{DD} = 3 V. See Figure 20.

MICROPROCESSOR INTERFACING

AD5620/AD5640 to ADSP-2101/ADSP-2103 Interface

Figure 28 shows a serial interface between the AD5620/AD5640 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after SPORT is enabled.

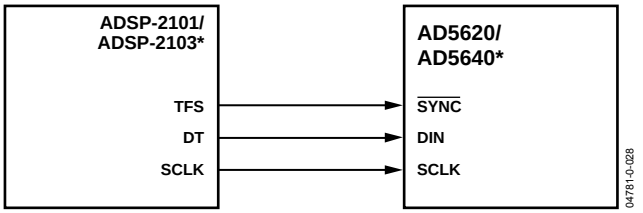

Figure 28. AD5620/AD5640 to ADSP-2101/ADSP-2103 Interface

AD5620/AD5640 to 68HC11/68L11 Interface

Figure 29 shows a serial interface between the AD5620/AD5640 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5620/AD5640, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The set-up conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. When data transmits to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 transmits in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data transmits MSB first. In order to load data to the AD5620/AD5640, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

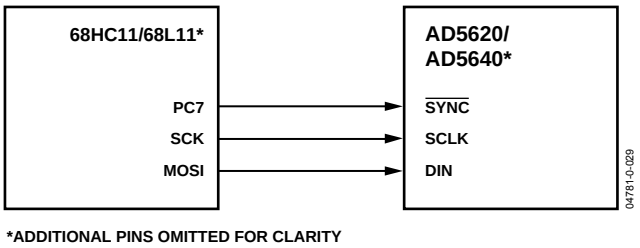

Figure 29. AD5620/AD5640 to 68HC11/68L11 Interface

AD5620/AD5640 to 80C51/80L51 Interface

Figure 30 shows a serial interface between the AD5620/AD5640 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5620/AD5640, while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data transmits to the AD5620/AD5640, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5620/AD5640 requires its data with MSBfirst. The 80C51/80L51 transmit routine should take this into account.

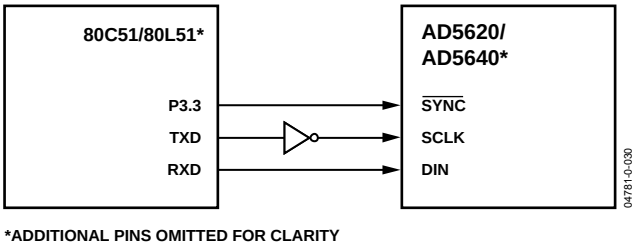

Figure 30. AD5620/AD5640 to 80C51/80L51 Interface

AD5620/AD5640 to MICROWIRE Interface

Figure 31 shows an interface between the AD5320 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5320 on the rising edge of the SK.

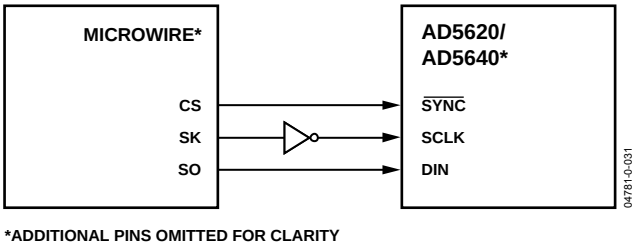

Figure 31. AD5620/AD5640 to MICROWIRE Interface

OUTLINE DIMENSIONS

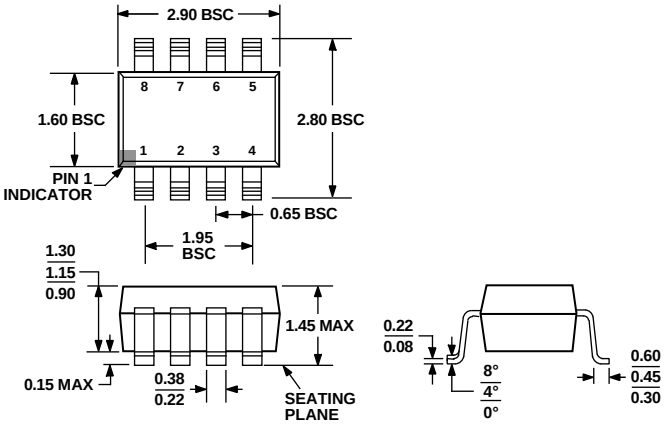

Figure 32. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimension shown in millimeters

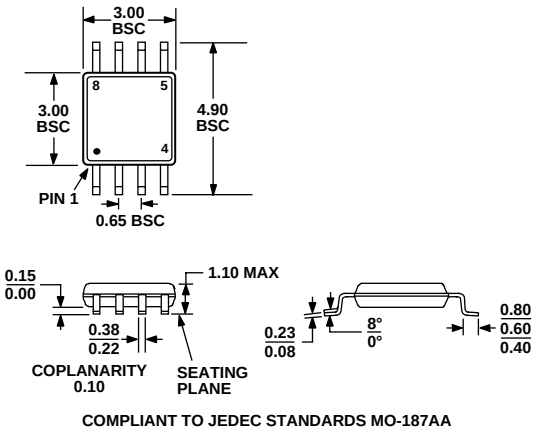

Figure 33. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Grade	Power-On Reset to	Internal Reference	Package Description	Package Options	Branding	Description
AD5620ARJ-1	A	Zero	1.25 V	SOT-23	RJ-8	D2K	±2 LSB INL, 25 ppm/°C Ref
AD5620ARJ-2	A	Zero	2.5 V	SOT-23	RJ-8	D2L	±2 LSB INL, 25 ppm/°C Ref
AD5620BRJ-1	B	Zero	1.25 V	SOT-23	RJ-8	D2H	±1 LSB INL, 25 ppm/°C Ref
AD5620BRJ-2	B	Zero	2.5 V	SOT-23	RJ-8	D2J	±1 LSB INL, 25 ppm/°C Ref
AD5620CRJ-1	C	Zero	1.25 V	SOT-23	RJ-8	D2M	±1 LSB INL, 25 ppm/°C Ref
AD5620CRJ-2	C	Zero	2.5 V	SOT-23	RJ-8	D2N	±1 LSB INL, 10 ppm/°C Ref
AD5620CRJ-3	C	Midscale	2.5 V	SOT-23	RJ-8	D2P	±1 LSB INL, 10 ppm/°C Ref
AD5620CRM-1	C	Zero	1.25 V	MSOP	RM-8	D2M	±1 LSB INL, 10 ppm/°C Ref
AD5620CRM-2	C	Zero	2.5 V	MSOP	RM-8	D2N	±1 LSB INL, 10 ppm/°C Ref
AD5620CRM-3	C	Midscale	2.5 V	MSOP	RM-8	D2P	±1 LSB INL, 10 ppm/°C Ref
AD5640ARJ-1	A	Zero	1.25 V	SOT-23	RJ-8	D2S	±8 LSB INL, 25 ppm/°C Ref
AD5640ARJ-2	A	Zero	2.5 V	SOT-23	RJ-8	D2T	±8 LSB INL, 25 ppm/°C Ref
AD5640BRJ-1	B	Zero	1.25 V	SOT-23	RJ-8	D2Q	±4 LSB INL, 25 ppm/°C Ref
AD5640BRJ-2	B	Zero	2.5 V	SOT-23	RJ-8	D2R	±4 LSB INL, 25 ppm/°C Ref
AD5640CRJ-1	C	Zero	1.25 V	SOT-23	RJ-8	D2U	±4 LSB INL, 25 ppm/°C Ref
AD5640CRJ-2	C	Zero	2.5 V	SOT-23	RJ-8	D2V	±4 LSB INL, 10 ppm/°C Ref
AD5640CRJ-3	C	Midscale	2.5 V	SOT-23	RJ-8	D2W	±4 LSB INL, 10 ppm/°C Ref
AD5640CRM-1	C	Zero	1.25 V	MSOP	RM-8	D2U	±4 LSB INL, 10 ppm/°C Ref
AD5640CRM-2	C	Zero	2.5 V	MSOP	RM-8	D2V	±4 LSB INL, 10 ppm/°C Ref
AD5640CRM-3	C	Midscale	2.5 V	MSOP	RM-8	D2W	±4 LSB INL, 10 ppm/°C Ref

NOTES

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PR04781–0–10/04(PrA)