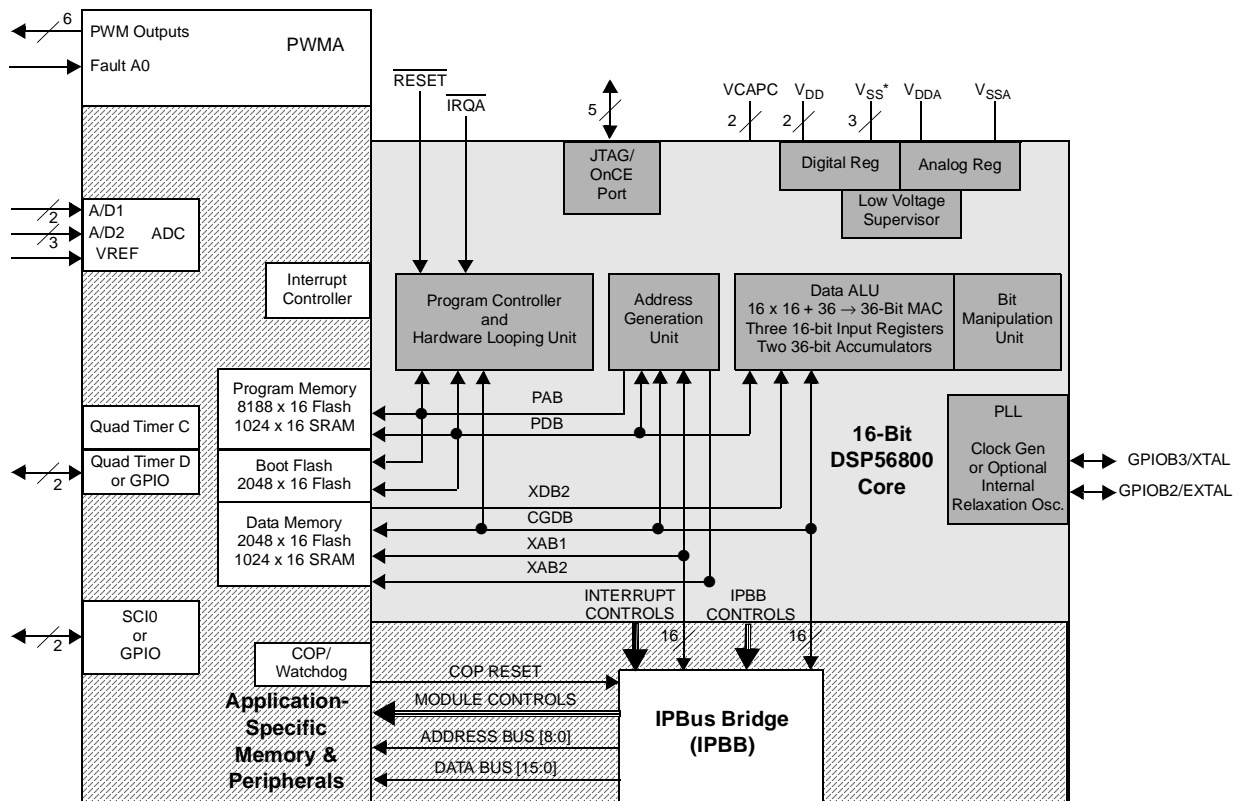# DSP56F802

*Product Brief*
# DSP56F802 16-bit Digital Signal Processor

- Up to 40 MIPS operation at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 8K × 16-bit words Program Flash
- 1K × 16-bit words Program RAM
- 2K × 16-bit words Data Flash
- 1K × 16-bit words Data RAM
- 2K × 16-bit words Boot Flash

- Hardware DO and REP loops
- 6-channel PWM Module
- Two 12-bit ADCs (1 x 2 channel, 1 x 3 channel)
- Serial Communications Interface (SCI)
- Two General Purpose Quad Timers with 2 external pins
- JTAG/OnCE™ port for debugging
- On-chip relaxation oscillator
- 32-pin LQFP Package
- 4 shared GPIO



*includes TCS pin which is reserved for factory use and is tied to VSS

**Figure 1. DSP56F802 Block Diagram**

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# DSP56800 Digital Signal Processing Core Features

- Efficient 16-bit DSP56800 family DSP engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80 MHz core frequency
- Single-cycle $16 \times 16$-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

# DSP56F802 Memory Features

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low cost, high volume flash solution
    - $8K \times 16$ bit words of Program Flash
    - $1K \times 16$-bit words of Program RAM
    - $2K \times 16$-bit words of Data Flash
    - $1K \times 16$-bit words of Data RAM
    - $2K \times 16$-bit words of BootFLASH
- Programmable BootFLASH supports customized boot code and field upgrades of stored code through JTAG interface

# DSP56F802 Peripheral Circuit Features

- Pulse Width Modulator (PWM) with six PWM outputs with deadtime insertion; supports both center- and edge-aligned modes
- Two 12-bit, Analog-to-Digital Converters (ADCs), 1 x 2 channel and 1 x 3 channel, which support two simultaneous conversions with a total of five inputs; ADC and PWM modules can be synchronized
- General Purpose Quad Timers with two extra pins (or two addidtional GPIO lines)
- Serial Communication Interface (SCI) with two pins (or two GPIO)
- Four multiplexed General Purpose I/O (GPIO) pins
- Computer-Operating Properly (COP) watchdog timer
- External reset pin for hardware reset
- Trimmable on-chip relaxation oscillator

- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the DSP core clock

# Energy Information

- Fabricated in high-density CMOS with 5V tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Integrated power supervisor
- Wait and Stop modes available

# DSP56F802 Description

The DSP56F802 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the DSP56F802 is well-suited for many applications. The DSP56F802 includes many peripherals that are especially useful for applications such as: motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, and industrial control for power, lighting, automation.

The DSP56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers to enable rapid development of optimized control applications.

# "Best in Class" Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow programmers to create their unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

# Product Documentation

The four documents listed in Table 1 are required for a complete description and proper design with the DSP56F802. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/dsp.

### Table 1. DSP56F802 Chip Documentation

| Topic | Description | Order Number |
|---|---|---|
| DSP56800 Family Manual | Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set | DSP56800FM/D |
| DSP56F80x User's Manual | Detailed description of memory, peripherals, and interfaces of the DSP56F801, DSP56F802, DSP56F803, DSP56F805, and DSP56F807 | DSP56F801-7UM/D |
| DSP56F802 Technical Data Sheet | Electrical and timing specifications, pin descriptions, and package descriptions | DSP56F802/D |
| DSP56F802 Product Brief | Summary description and block diagram of the DSP56F802 core, memory, peripherals and interfaces (this document) | DSP56F802PB/D |

# Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to order parts.

### Table 2. DSP56F802 Ordering Information

| Part | Supply Voltage | Package Type | Pin Count | Frequency (MHz) | Order Number |
|---|---|---|---|---|---|
| DSP56F802 | 3.0–3.6 V | Plastic Quad Flat Pack (LQFP) | 48 | 80 | DSP56F802FA80 |

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