



16-BIT PIN PROGRAMMABLE D/S OR D/R CONVERTER

DESCRIPTION

The DSC-11520 is a versatile multiplying digital-to-analog converter. The digital input represents an angle and the output is pin programmable for either resolver type sin/cos or for three-line synchro output. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is DC-coupled to the output, the DSC-11520 can be used in many configurations:

With a synchro or resolver reference input, the DSC-11520 is a digital-to-synchro or digital-to-resolver converter.

With a DC reference input, the unit can be used as a hybrid digital-to-sin/cos DC converter.

With the reference input proportional to the radius vector, the DSC-11520 converts polar to rectangular coordinates.

With a sawtooth reference input and a rotating digital input, the module can generate a cartwheel rotating sweep for PPI displays.

Packaged in a 36 pin double DIP, the DSC-11520 is a complete D/S and D/R converter in one hybrid module.

The DSC-11520 features low weight, low power consumption, very high reliability, and a wide operating temperature range. The circuit design results in high accuracy and reduces the output scale factor so that the output can drive displays directly. The output line-to-line voltage can be scaled by external resistors. The reference input provides high AC and DC common mode rejection.

APPLICATIONS

Because of its high reliability, small size and low power consumption, the hybrid DSC-11520 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-PRF-38534 processing as a standard option.

Among the many possible applications are computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems, and PPI displays including moving target indicators.

FEATURES

- Complete D/S or D/R Converter
- Accuracy: to ±1 Minute
- 0.05% Scale Factor Variation With Angle
- DC-Coupled Reference Accepts Any Waveform
- Generates SIN/COS DC or Rotating PPI Sweep
- High-Rel CMOS D/R Chip
- 8-Bit/2-Byte Double Buffered Transparent Latches

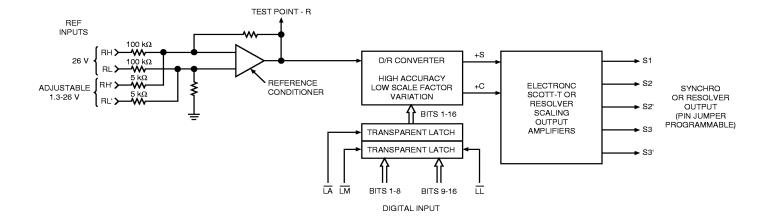
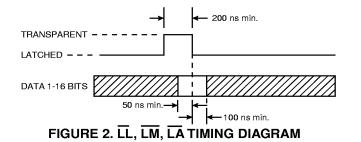


FIGURE 1. DSC-11520 BLOCK DIAGRAM

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TABLE 1. DSC-11520 SPECIFICATIONS Apply over temperature range, power supply ranges, reference voltage							
and frequency range and 10% harmonic distortion in the reference.							
PARAMETER	VALUE						
RESOLUTION	16 bits						
ACCURACY AND							
DYNAMICS Output Accuracy	+9 minutes to +1 min (See Ordering Info)						
Differential Linearity	±8 minutes to ±1 min. (See Ordering Info.) ±1 LSB max						
Output Settling Time	Less than 20 µsec for any digital step change.						
DIGITAL INPUT							
Logic Typ e	Natural binary angle parallel positive logic CMOS and						
	TTL compatible.						
	Inputs are CMOS transient protected. Each input has a 20 µA max pull down to GND.						
Logic Voltage Level V _L	V = +4.5 V to +15 V supply						
	Logic $0 = 0$ to $+0.25 \text{ V}_1$						
Load Current	Logic 1 = 0.4 V_{L} to V_{L}						
Load Cullent	20 μ A max to GND (bit 1-16) 20 μ A to V _L (\overline{LL} , \overline{LM} , \overline{LA}) See Timing Diagram						
	(FIGURE 2)						
REFERENCE INPUT							
Туре	Two differential solid-state inputs, one for standard 26						
Frequency Range	V input and one programmable. DC to 1000 Hz						
l requeries riange	Standard Input Programmable input						
Voltage	26 V ±10% 1.3 V min for full output;						
			tages are scaled by series resistors				
Input Impedance		adding (W	2 361163 16313(013				
Single Ended	100 kΩ \pm 0.5%	5 kΩ ± 0.5%					
Differential	$200 \text{ k}\Omega \pm 0.5\%$	$10 \text{ k}\Omega \pm 0$.5%				
ANALOG OUTPUT	Pin programmable for synchro or resolver mode.						
Type Output current	2 mA rms max.						
Max Output Voltage (Tracks	11.8 V rms L-L ±0.25%nominal in synchro mode						
Reference Input Voltage)	6.81 V rms L-L ±0.25%nominal resolver mode						
	±0.2% max						
Transformation Ratio Tol. Scale Factor Variation	±0.05% max						
DC Offset Each Line to	±15 mV standard, varies with input angle						
GND	±5 mV available- Consult Factory						
POWER SUPPLIES	1						
Voltage		-15 V	Logic Voltage V _L				
Voltage Limits		±5% -18 V	+4.5 V TO +15 V +18 V				
Max Voltage Without Damage	+18 V	-18 V	+18 V				
Current or impedance	20 mA max	20 mAmax	±100 μA				
· ·		connected wher	e +5 V logic levels				
	are used.						
TEMPERATURE RANGES							
(CASE)							
Operating -1 Option	-55°C to +125°C						
-3 Option	0°C to +70°C						



-55°C to 135°C

36 pin double DIP

0.85 oz (24g)

0.78 X 1.9 X 0.21inch (2.0 X 4.8 X 0.53 cm)

Storage

PHYSICAL

CHARACTERISTICS

Туре

Size

Weight

INTRODUCTION

As shown in the block diagram, the signal conversion in the DSC-11520 is performed by a high accuracy digital-to-resolver converter whose sin and cos outputs have a low scale factor variation as a function of the digital input angle. This resolver output is either amplified by scaling amplifiers for resolver output, or is both amplified and converted to a synchro output by an electronic Scott-T. In both cases, the output line currents are limited to 2 mA rms max, which is sufficient for driving S/D converters, solid-state control transformers, and displays. Output power amplifiers will be required, however, for driving electro-mechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high AC and DC common mode rejection, so that a reference isolation transformer will seldom be required. There are two sets of reference inputs. The RH, RL input provides the maximum synchro or resolver output voltage for a standard 26 V rms reference input. The RH', RL' input is used to scale the output for other reference voltage levels. Series resistors can be added to the reference input as described below either to accommodate lower reference levels for full output, or to reduce the output level.

The reference conditioner output -R is intended for test purposes. A signal between 6 V and 7.5 V at -R indicates that a reference input signal is present.

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The DSC-11520 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage.

The maximum line-to line levels are determined by the output amplifiers and are nominally 11.8 V for synchro output and 6.81 V for resolver output. The RH, RL reference input is designed to provide this nominal output for the standard 26 V reference level. The scaling adjustment is made by two internal 100 $k\Omega$ resistors in series with the reference conditioner input (see DSC-11520 Block Diagram). The maximum output levels without distortion are 10% greater than the nominal 11.8 V and 6.81 V levels.

The RH', RL' reference input has only 5 k Ω internal resistors in series with the reference conditioner input, so that nominal line-to-line output is obtained for a reference input of 1.3 V. For higher reference voltages, two resistors R' must be inserted in series with the inputs as shown in FIGURE 3. These resistors scale the

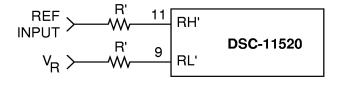


FIGURE 3. REFERENCE LEVEL ADJUSTMENT

DSC-11520 outputs down to the nominal 11.8 V and 6.81 V levels stated above, or to lower voltages if desired. The magnitude of the resistors R' in ohms is calculated as follows:

$$R' = \frac{5000}{1.3} (V_R - 1.3) \left(\frac{NOMINAL L-L VOLTAGE LEVEL}{DESIRED L-L VOLTAGE LEVEL} \right)$$

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing: Synchro output

S1 — S3 = (RH-RL)
$$A_0$$
 (1 + A(θ)) sin θ
S3 — S2 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 120°)
S2 — S1 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 240°)
Resolver output

S1 — S3 = (RH-RL)
$$A_0$$
 (1 + $A(\theta)$) $\sin \theta$
S2 — S4 = (RH-RL) A_0 (1 + $A(\theta)$) $\cos \theta$

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The transformation ratio A_O is 11.8/26 for 11.8 V rms L-L output. The maximum variation in A_O from all causes is ±0.2%. The term A (θ) represents the variation of the amplitude with the digital input angle. A (θ) , which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.05% for all values of θ . The total maximum variation in A_O (1 + A(θ)) is therefore ±0.25%.

Because the amplitude factor (RH-RL) A_0 (1 + $A(\theta)$) varies simultaneously on all output lines, it will not be a source of error when the DSC-11520 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in X-Y plotters, the amplitude variations must be taken into account.

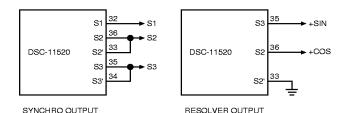
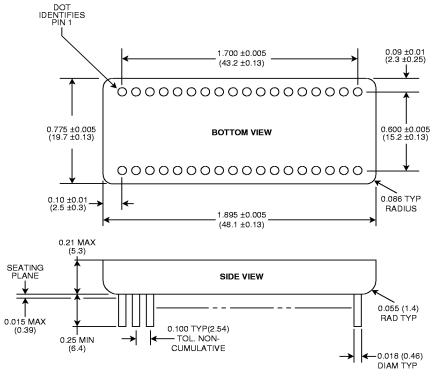


FIGURE 4. OUTPUT PIN PROGRAMMING

TABLE 2. PIN CONNECTIONS							
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION		
1 2 3 4 5 6 7 8 9 10 11 12	NC +15 V GND -15 V NC VL -R RL RL' RH RH' BIT 14	13 14 15 16 17 18 19 20 21 22 23 24	BIT 13 BIT 12 BIT 11 BIT 10 BIT 9 BIT 8 BIT 7 BIT 6 BIT 5 BIT 5 BIT 4 BIT 3	25 26 27 28 29 30 31 32 33 34 35 36	BIT 1 (MSB) BIT 15 BIT 16 (LSB) LM LL LA NC S1 S2' S3' S3 (+SIN) S2 (+COS)		

Notes:

- 1.-R (PIN 7) can be used for test purposes to detect whether a reference signal is present. See block diagram.
- 2. Functions LL, LA and LM may be left unconnected when not used.
- 3. V_L (PIN 6) may be left unconnected where 5 V logic levels are used.

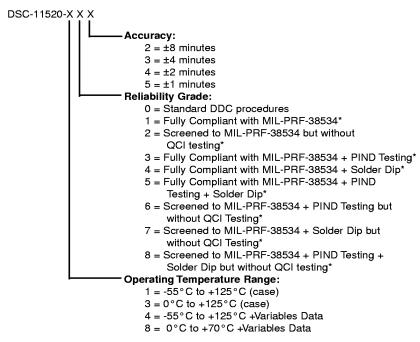


NOTES

- 1. Dimensions shown are in inches (millimeters)
- 2. Lead identification numbers are for reference only. 3. Lead cluster shall be Centered within ± 0.10 of out-
- line dimensions. Lead spacing dimensions apply only at seating plane.
- Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
- 5. Package is Kovar with electroless nickel plating.
- 6. Case is electrically floating.

FIGURE 5. MECHANICAL OUTLINE 36 PIN DOUBLE DIP

ORDERING INFORMATION



*Available in -55°C to +125°C tempeature range only.

The information in this data sheet is believed to be accurate; however, no responsibility is assumed by ILC Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith.

Specifications are subject to change without notice.



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F-10/96-500 PRINTED IN THE U.S.A.