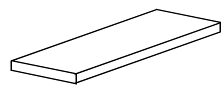
PRELIMINARY

128-common x 132-segment BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6679** is a 128-common x 132-segment bit map LCD driver to display graphics or characters.
It contains 25,344 bits display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.
An image data from CPU through the serial or 8-bit parallel interface are stored into the 25,344 bits internal display data RAM and are displayed on the LCD panel through the commons and segments drivers.
The **NJU6679** displays 128 x 132 dots graphics or 8-character 8-line by 16 x 16 dots character.
The **NJU6679** contains a built-in OSC circuit for reducing external components. And it features Partial Display Function containing selectable active display block(s) (two blocks max.) and optimizing the duty cycle ratio. This function dramatically reduces the operating current, setting the optimum boosted voltage combined with a programmable voltage booster circuit and an electrical variable resister. As result, it reduces the operating current.
The operating voltage from 2.4V to 3.6V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE



NJU6679CJ

■ FEATURES

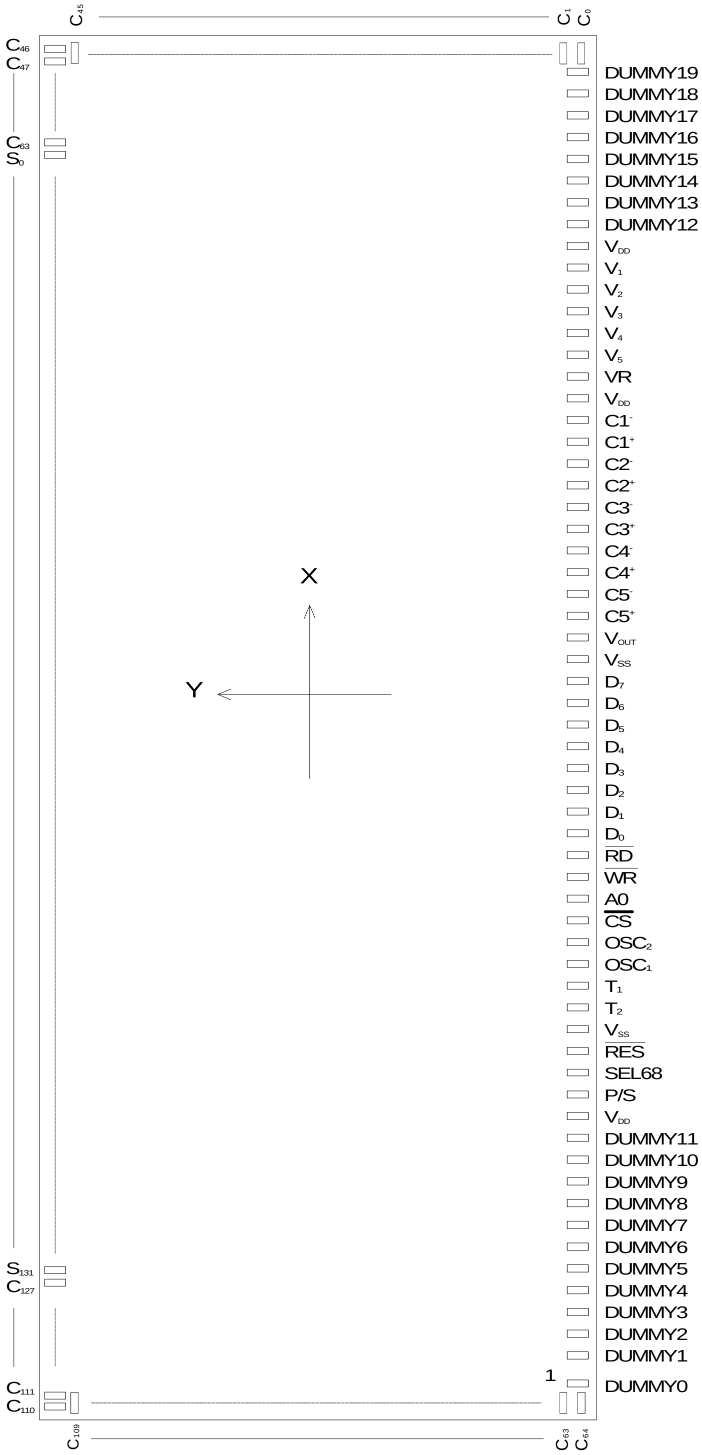
- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Data RAM - 25,344 bits ;(1.5 times over than display size)
- LCD drivers - 128-common and 132-segment
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface
- Partial Display Function Two limited active display blocks setting. Duty ratio set automatically.
- Easy Vertical Scroll by setting the start line address of over size display data RAM
- Programmable Bias selection ; 1/4,1/5,1/6,1/7,1/8,1/9,1/10,1/11,1/12 bias
- Common Driver Order Assignment by mask option

Version	C_0 to C_{127}(Pin name)
NJU6679A	Com_0 to Com_{127}
NJU6679B	Com_{127} to Com_0

- Useful Instruction Sets
  Display ON/OFF Cont, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Display Data Read/Write, Inverse Display, All On/Off, Partial Display, Bias Select, n-Line Inverse, Voltage Booster Circuits Multiple Select(Maximum 6-time), Read Modify Write, Power Saving, ADC Select, etc.
- Power Supply Circuits for LCD; Programmable Voltage Booster Circuits(6-time Maximum, Voltage boosting polarity:Negative voltage(V_{DD} Common)),Regulator, Voltage Follower (x 4)
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 3.6V
- LCD Driving Voltage --- 6.0V to 18V
- Package Outline --- COF / TCP / Bumped Chip
- C-MOS Technology (Substrate:N)

2001
Ver.4.8

■ PAD LOCATION



Chip Center	: X=0um,Y=0um
Chip Size	: X=10.31mm,Y=3.13mm
Chip Thickness	: 675um ± 30um
Bump Size	: 45um x 83um
Pad pitch	: 60um(Min)
Bump Height	: 15um TYP.
Bump Material	: Au
Voltage boosting polarity	:Negative voltage (VDD Common)
Substrate	:N

■TERMINAL DESCRIPTION

Chip Size 10.31 x 3.13mm (Chip Center X=0um,Y=0um)

PAD No.	Terminal	X= um	Y= um
1	DUMMY0	-4884	-1405
2	DUMMY1	-4132	-1405
3	DUMMY2	-4062	-1405
4	DUMMY3	-3992	-1405
5	DUMMY4	-3922	-1405
6	DUMMY5	-3852	-1405
7	DUMMY6	-3782	-1405
8	DUMMY7	-3712	-1405
9	DUMMY8	-3642	-1405
10	DUMMY9	-3572	-1405
11	DUMMY10	-3502	-1405
12	DUMMY11	-3432	-1405
13	V_{DD}	-3270	-1405
14	P/S	-3104	-1405
15	SEL68	-2884	-1405
16	$\overline{RES}$	-2648	-1405
17	V_{SS}	-2490	-1405
18	T_2	-2333	-1405
19	T_1	-2098	-1405
20	OSC_1	-1877	-1405
21	OSC_2	-1641	-1405
22	$\overline{CS}$	-1420	-1405
23	A0	-1184	-1405
24	$\overline{WR}$	-954	-1405
25	$\overline{RD}$	-717	-1405
26	D_0	-481	-1405
27	D_1	-260	-1405
28	D_2	-40	-1405
29	D_3	180	-1405
30	D_4	400	-1405
31	D_5	621	-1405
32	$D_{6(SCL)}$	841	-1405
33	$D_{7(SI)}$	1061	-1405
34	V_{SS}	1222	-1405
35	V_{OUT}	1398	-1405
36	$C5^+$	1468	-1405
37	$C5^-$	1538	-1405
38	$C4^+$	1608	-1405
39	$C4^-$	1678	-1405
40	$C3^+$	1748	-1405
41	$C3^-$	1818	-1405
42	$C2^+$	1888	-1405
43	$C2^-$	1958	-1405
44	$C1^+$	2028	-1405
45	$C1^-$	2098	-1405
46	V_{DD}	2168	-1405
47	VR	2327	-1405
48	V_5	2582	-1405
49	V_4	2652	-1405
50	V_3	2722	-1405

PAD No.	Terminal	X= um	Y= um
51	V_2	2792	-1405
52	V_1	2862	-1405
53	V_{DD}	2932	-1405
54	DUMMY12	3315	-1405
55	DUMMY13	3385	-1405
56	DUMMY14	3455	-1405
57	DUMMY15	3525	-1405
58	DUMMY16	3595	-1405
59	DUMMY17	3665	-1405
60	DUMMY18	3735	-1405
61	DUMMY19	4884	-1405
62	C_0	4995	-1416
63	C_1	4995	-1356
64	C_2	4995	-1296
65	C_3	4995	-1236
66	C_4	4995	-1176
67	C_5	4995	-1116
68	C_6	4995	-1056
69	C_7	4995	-996
70	C_8	4995	-936
71	C_9	4995	-876
72	C_{10}	4995	-816
73	C_{11}	4995	-756
74	C_{12}	4995	-696
75	C_{13}	4995	-636
76	C_{14}	4995	-576
77	C_{15}	4995	-516
78	C_{16}	4995	-456
79	C_{17}	4995	-396
80	C_{18}	4995	-336
81	C_{19}	4995	-276
82	C_{20}	4995	-216
83	C_{21}	4995	-156
84	C_{22}	4995	-96
85	C_{23}	4995	-36
86	C_{24}	4995	24
87	C_{25}	4995	84
88	C_{26}	4995	144
89	C_{27}	4995	204
90	C_{28}	4995	264
91	C_{29}	4995	324
92	C_{30}	4995	384
93	C_{31}	4995	444
94	C_{32}	4995	504
95	C_{33}	4995	564
96	C_{34}	4995	624
97	C_{35}	4995	684
98	C_{36}	4995	744
99	C_{37}	4995	804
100	C_{38}	4995	864

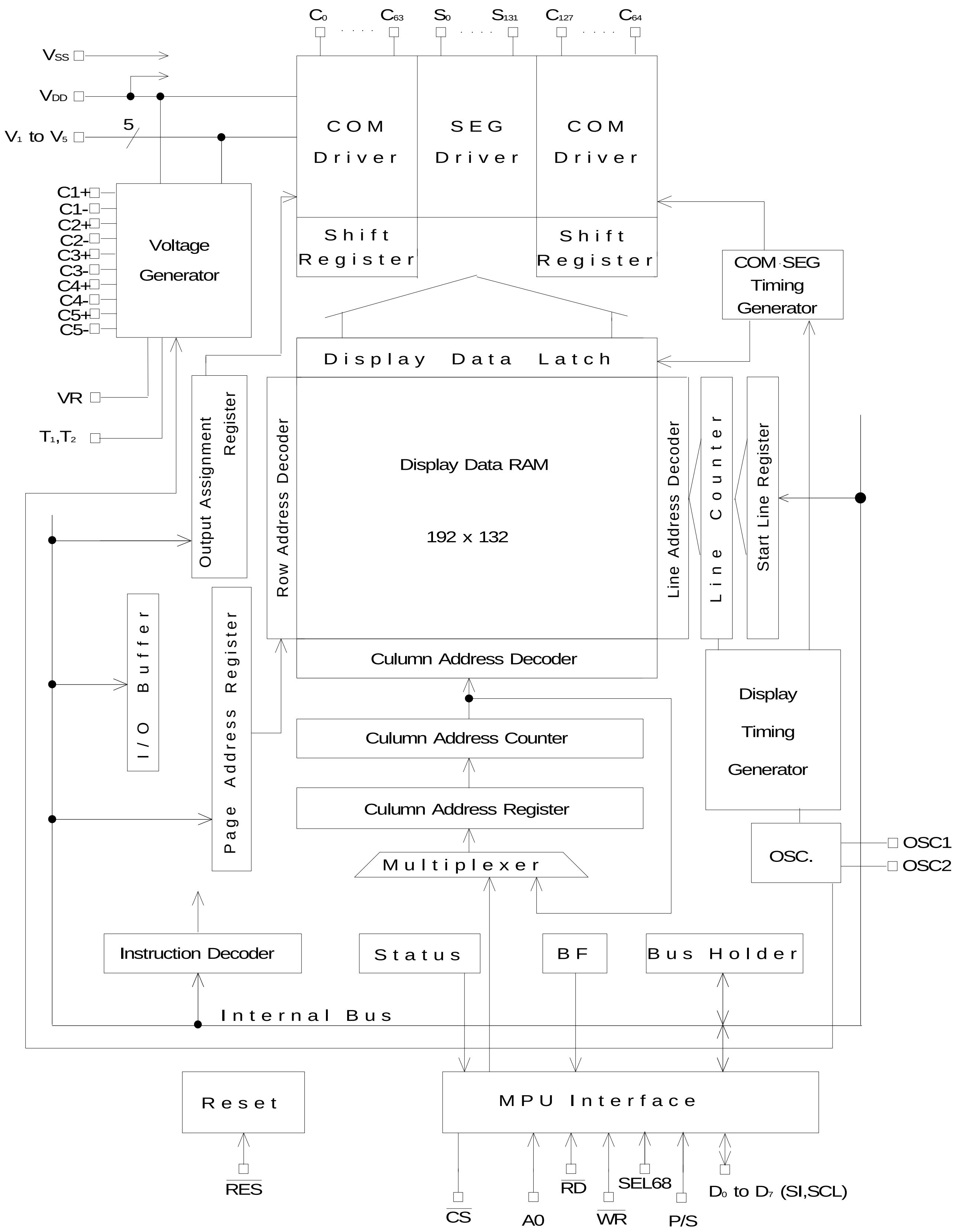
PAD No.	Terminal	X= um	Y= um
101	C_{39}	4995	924
102	C_{40}	4995	984
103	C_{41}	4995	1044
104	C_{42}	4995	1104
105	C_{43}	4995	1164
106	C_{44}	4995	1224
107	C_{45}	4995	1284
108	C_{46}	5010	1405
109	C_{47}	4950	1405
110	C_{48}	4890	1405
111	C_{49}	4830	1405
112	C_{50}	4770	1405
113	C_{51}	4710	1405
114	C_{52}	4650	1405
115	C_{53}	4590	1405
116	C_{54}	4530	1405
117	C_{55}	4470	1405
118	C_{56}	4410	1405
119	C_{57}	4350	1405
120	C_{58}	4290	1405
121	C_{59}	4230	1405
122	C_{60}	4170	1405
123	C_{61}	4110	1405
124	C_{62}	4050	1405
125	C_{63}	3990	1405
126	S_{0}	3930	1405
127	S_{1}	3870	1405
128	S_{2}	3810	1405
129	S_{3}	3750	1405
130	S_{4}	3690	1405
131	S_{5}	3630	1405
132	S_{6}	3570	1405
133	S_{7}	3510	1405
134	S_{8}	3450	1405
135	S_{9}	3390	1405
136	S_{10}	3330	1405
137	S_{11}	3270	1405
138	S_{12}	3210	1405
139	S_{13}	3150	1405
140	S_{14}	3090	1405
141	S_{15}	3030	1405
142	S_{16}	2970	1405
143	S_{17}	2910	1405
144	S_{18}	2850	1405
145	S_{19}	2790	1405
146	S_{20}	2730	1405
147	S_{21}	2670	1405
148	S_{22}	2610	1405
149	S_{23}	2550	1405
150	S_{24}	2490	1405

PAD No.	Terminal	X= um	Y= um
151	S_{25}	2430	1405
152	S_{26}	2370	1405
153	S_{27}	2310	1405
154	S_{28}	2250	1405
155	S_{29}	2190	1405
156	S_{30}	2130	1405
157	S_{31}	2070	1405
158	S_{32}	2010	1405
159	S_{33}	1950	1405
160	S_{34}	1890	1405
161	S_{35}	1830	1405
162	S_{36}	1770	1405
163	S_{37}	1710	1405
164	S_{38}	1650	1405
165	S_{39}	1590	1405
166	S_{40}	1530	1405
167	S_{41}	1470	1405
168	S_{42}	1410	1405
169	S_{43}	1350	1405
170	S_{44}	1290	1405
171	S_{45}	1230	1405
172	S_{46}	1170	1405
173	S_{47}	1110	1405
174	S_{48}	1050	1405
175	S_{49}	990	1405
176	S_{50}	930	1405
177	S_{51}	870	1405
178	S_{52}	810	1405
179	S_{53}	750	1405
180	S_{54}	690	1405
181	S_{55}	630	1405
182	S_{56}	570	1405
183	S_{57}	510	1405
184	S_{58}	450	1405
185	S_{59}	390	1405
186	S_{60}	330	1405
187	S_{61}	270	1405
188	S_{62}	210	1405
189	S_{63}	150	1405
190	S_{64}	90	1405
191	S_{65}	30	1405
192	S_{66}	-30	1405
193	S_{67}	-90	1405
194	S_{68}	-150	1405
195	S_{69}	-210	1405
196	S_{70}	-270	1405
197	S_{71}	-330	1405
198	S_{72}	-390	1405
199	S_{73}	-450	1405
200	S_{74}	-510	1405

PAD No.	Terminal	X= um	Y= um
201	S_{75}	-570	1405
202	S_{76}	-630	1405
203	S_{77}	-690	1405
204	S_{78}	-750	1405
205	S_{79}	-810	1405
206	S_{80}	-870	1405
207	S_{81}	-930	1405
208	S_{82}	-990	1405
209	S_{83}	-1050	1405
210	S_{84}	-1110	1405
211	S_{85}	-1170	1405
212	S_{86}	-1230	1405
213	S_{87}	-1290	1405
214	S_{88}	-1350	1405
215	S_{89}	-1410	1405
216	S_{90}	-1470	1405
217	S_{91}	-1530	1405
218	S_{92}	-1590	1405
219	S_{93}	-1650	1405
220	S_{94}	-1710	1405
221	S_{95}	-1770	1405
222	S_{96}	-1830	1405
223	S_{97}	-1890	1405
224	S_{98}	-1950	1405
225	S_{99}	-2010	1405
226	S_{100}	-2070	1405
227	S_{101}	-2130	1405
228	S_{102}	-2190	1405
229	S_{103}	-2250	1405
230	S_{104}	-2310	1405
231	S_{105}	-2370	1405
232	S_{106}	-2430	1405
233	S_{107}	-2490	1405
234	S_{108}	-2550	1405
235	S_{109}	-2610	1405
236	S_{110}	-2670	1405
237	S_{111}	-2730	1405
238	S_{112}	-2790	1405
239	S_{113}	-2850	1405
240	S_{114}	-2910	1405
241	S_{115}	-2970	1405
242	S_{116}	-3030	1405
243	S_{117}	-3090	1405
244	S_{118}	-3150	1405
245	S_{119}	-3210	1405
246	S_{120}	-3270	1405
247	S_{121}	-3330	1405
248	S_{122}	-3390	1405
249	S_{123}	-3450	1405
250	S_{124}	-3510	1405
251	S_{125}	-3570	1405
252	S_{126}	-3630	1405
253	S_{127}	-3690	1405
254	S_{128}	-3750	1405
255	S_{129}	-3810	1405
256	S_{130}	-3870	1405
257	S_{131}	-3930	1405
258	C_{127}	-3990	1405
259	C_{126}	-4050	1405
260	C_{125}	-4110	1405
261	C_{124}	-4170	1405
262	C_{123}	-4230	1405
263	C_{122}	-4290	1405
264	C_{121}	-4350	1405
265	C_{120}	-4410	1405
266	C_{119}	-4470	1405
267	C_{118}	-4530	1405
268	C_{117}	-4590	1405
269	C_{116}	-4650	1405
270	C_{115}	-4710	1405
271	C_{114}	-4770	1405
272	C_{113}	-4830	1405
273	C_{112}	-4890	1405
274	C_{111}	-4950	1405
275	C_{110}	-5010	1405
276	C_{109}	-4995	1284
277	C_{108}	-4995	1224
278	C_{107}	-4995	1164
279	C_{106}	-4995	1104
280	C_{105}	-4995	1044
281	C_{104}	-4995	984
282	C_{103}	-4995	924
283	C_{102}	-4995	864
284	C_{101}	-4995	804
285	C_{100}	-4995	744
286	C_{99}	-4995	684
287	C_{98}	-4995	624
288	C_{97}	-4995	564
289	C_{96}	-4995	504
290	C_{95}	-4995	444
291	C_{94}	-4995	384
292	C_{93}	-4995	324
293	C_{92}	-4995	264
294	C_{91}	-4995	204
295	C_{90}	-4995	144
296	C_{89}	-4995	84
297	C_{88}	-4995	24
298	C_{87}	-4995	-36
299	C_{86}	-4995	-96
300	C_{85}	-4995	-156

PAD No.	Terminal	X= um	Y= um
301	C_{84}	-4995	-216
302	C_{83}	-4995	-276
303	C_{82}	-4995	-336
304	C_{81}	-4995	-396
305	C_{80}	-4995	-456
306	C_{79}	-4995	-516
307	C_{78}	-4995	-576
308	C_{77}	-4995	-636
309	C_{76}	-4995	-696
310	C_{75}	-4995	-756
311	C_{74}	-4995	-816
312	C_{73}	-4995	-876
313	C_{72}	-4995	-936
314	C_{71}	-4995	-996
315	C_{70}	-4995	-1056
316	C_{69}	-4995	-1116
317	C_{68}	-4995	-1176
318	C_{67}	-4995	-1236
319	C_{66}	-4995	-1296
320	C_{65}	-4995	-1356
321	C_{64}	-4995	-1416

■ BLOCK DIAGRAM



■TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1 to 12,
54 to 61</td><td>DUMMY0
to
DUMMY19</td><td></td><td>Dummy Terminals.
These are open terminals electrically.</td></tr>
<tr><td>13,46,53</td><td>V_{DD}</td><td>Power</td><td>Power Supply Terminal (+2.4V - +3.6V)</td></tr>
<tr><td>17,34</td><td>V_{SS}</td><td>GND</td><td>Ground Terminal (0V)</td></tr>
<tr><td>52
51
50
49
48</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminals. In case of the external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation.
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$
In case of the internal power supply, LCD driving voltages V1-V4 depending on the Bias selection are supplied as shown in follows;
<table>
<tr><th>Bias</th><th>V_1</th><th>V_2</th><th>V_3</th><th>V_4</th></tr>
<tr><td>1/4Bias</td><td>V_5+3/4V_{LCD}</td><td>V_5+2/4V_{LCD}</td><td>V_5+2/4V_{LCD}</td><td>V_5+1/4V_{LCD}</td></tr>
<tr><td>1/5Bias</td><td>V_5+4/5V_{LCD}</td><td>V_5+3/5V_{LCD}</td><td>V_5+2/5V_{LCD}</td><td>V_5+1/5V_{LCD}</td></tr>
<tr><td>1/6Bias</td><td>V_5+5/6V_{LCD}</td><td>V_5+4/6V_{LCD}</td><td>V_5+2/6V_{LCD}</td><td>V_5+1/6V_{LCD}</td></tr>
<tr><td>1/7Bias</td><td>V_5+6/7V_{LCD}</td><td>V_5+5/7V_{LCD}</td><td>V_5+2/7V_{LCD}</td><td>V_5+1/7V_{LCD}</td></tr>
<tr><td>1/8Bias</td><td>V_5+7/8V_{LCD}</td><td>V_5+6/8V_{LCD}</td><td>V_5+2/8V_{LCD}</td><td>V_5+1/8V_{LCD}</td></tr>
<tr><td>1/9Bias</td><td>V_5+8/9V_{LCD}</td><td>V_5+7/9V_{LCD}</td><td>V_5+2/9V_{LCD}</td><td>V_5+1/9V_{LCD}</td></tr>
<tr><td>1/10Bias</td><td>V_5+9/10V_{LCD}</td><td>V_5+8/10V_{LCD}</td><td>V_5+2/10V_{LCD}</td><td>V_5+1/10V_{LCD}</td></tr>
<tr><td>1/11Bias</td><td>V_5+10/11V_{LCD}</td><td>V_5+9/11V_{LCD}</td><td>V_5+2/11V_{LCD}</td><td>V_5+1/11V_{LCD}</td></tr>
<tr><td>1/12Bias</td><td>V_5+11/12V_{LCD}</td><td>V_5+10/12V_{LCD}</td><td>V_5+2/12V_{LCD}</td><td>V_5+1/12V_{LCD}</td></tr>
</table>
(V_{LCD}=V_{DD}-V_5)</td></tr>
<tr><td>44,45
42,43
40,41
38,39
36,37</td><td>$C1^+$,$C1^-$
$C2^+$,$C2^-$
$C3^+$,$C3^-$
$C4^+$,$C4^-$
$C5^+$,$C5^-$</td><td>O</td><td>Capacitor connecting terminals for Internal Voltage Booster.Boosting time is programmed by instruction (2 to 6 times)</td></tr>
<tr><td>35</td><td>V_{OUT}</td><td>O</td><td>Boosted voltage output terminal. Connects the capacitor between V_{OUT} terminal and V_{SS}.</td></tr>
<tr><td>47</td><td>VR</td><td>I</td><td>V_{LCD} voltage adjustment terminal. The gain of V_{LCD} setup circuit for V5 level is adjusted by external resistors.</td></tr>
<tr><td>19
18</td><td>T_1
T_2</td><td>I</td><td>LCD bias voltage control terminals.
<table>
<tr><th>T_1</th><th>T_2</th><th>Voltage booster Cir.</th><th>Voltage Adj.</th><th>V/F Cir.</th></tr>
<tr><td>L</td><td>L/H</td><td>Available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr>
</table></td></tr>
<tr><td>26 to 33</td><td>D_0 to
D_7
(SI)
(SCL)</td><td>I/O</td><td>Data Input/Output terminals.
In Pararel Interface Mode (P/S="H")
I/O terminals of 8-bit bus.
In Serial Interface Mode (P/S="L")
D_7: Input terminal of serial data (SI).
D_6: Input terminal of serial data clock (SCL).
D_0 to D_5 terminals are Hi-impedance.
When $\overline{CS}$="H", D_0 to D_7 terminals are Hi-impedance.</td></tr>
<tr><td>23</td><td>A0</td><td>I</td><td>Data discrimination signal input terminal. The signal from MPU discreminates transmoitted data between Display data and Instruction.
<table>
<tr><th>A0</th><th>H</th><th>L</th></tr>
<tr><td>Distin.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>16</td><td>$\overline{RES}$</td><td>I</td><td>Reset terminal.
Reset operation is executing during "L" state of $\overline{RES}$.</td></tr>
<tr><td>22</td><td>$\overline{CS}$</td><td>I</td><td>Chip select signal input terminal.
Data Input/Output are available during $\overline{CS}$ ="L".</td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>25</td><td>$\overline{RD}$(E)</td><td>I</td><td>RD(80 type) or E(68 type) signal input terminal.
<In 80 type MPU mode >(SEL68="L")
$\overline{RD}$ signal from 80 type MPU input terminal. Active "L".
D_0 to D_7 terminals are output during "L" level.
<In 68 type MPU mode >(SEL68="H")
Enable signal from 68 type MPU input terminal. Active "H".</td></tr>
<tr><td>24</td><td>$\overline{WR}$(RW)</td><td>I</td><td>WR(80 type) or R/W(68 type) signal input terminal
<In 80 type MPU mode >(SEL68="L")
$\overline{WR}$ signal from 80 type MPU input terminal. Active "L".
The data transmitted during WR="L" are fetched at the rising edge of $\overline{WR}$.
<In 68 type MPU mode > (SEL68="H")
R/W signal from 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>15</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal. This terminal must connect to V_{DD} or V_{SS}.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>14</td><td>P/S</td><td>I</td><td>Parallel or Serial interface selection signal input terminal.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>serial Clock</td></tr>
<tr><td>"H"</td><td>$\overline{CS}$</td><td>A</td><td>D_0 to D_7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr>
</table>
In case of serial interface(P/S="L")
RAM data and status read operation do not work in mode of the serial interface. $\overline{RD}$ and $\overline{WR}$ terminals must fix to "H" or "L". D_0 to D_5 terminals are Hi-impedance.</td></tr>
<tr><td>20
21</td><td>OSC_1
OSC_2</td><td>I</td><td>External clock input terminal. In Internal oscillation operation, OSC1 and OSC2 terminals should be Open.In External clock operation, the external clock input to OSC1 terminal.</td></tr>
<tr><td>62 to 125</td><td>C_0 to C_{63}</td><td>O</td><td rowspan="3">LCD driving signal output terminals.
Common output terminals:C_0 to C_{127}
Segment output terminals:S_0 to S_{131}

Common output terminal
Following output voltage is selected by the combination of alternating (FR) signal and Common scanning data.
<table>
<tr><td>Scan data</td><td>FR</td><td>Output Voltage</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table>
Segment output terminal
Following output voltage is selected by the combination of alternating (FR) signal and display data in the DD RAM.
<table>
<tr><td rowspan="2">RAM Data</td><td rowspan="2">FR</td><td colspan="2">Output Voltage</td></tr>
<tr><td>Normal</td><td>Reverse</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>126 to 257</td><td>S_0 to S_{131}</td><td>O</td></tr>
<tr><td>321 to 258</td><td>C_{64} to C_{127}</td><td>O</td></tr>
</table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)
The Busy Flag (BF) is set to logical ”1” in busy of internal execution by an instruction, and any instruction excepting for the “Status Read” is disable at this time. Busy Flag is outputted through D_7 terminal by “Status Read” instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in ■AC Characteristics is secured completely.

(1-2)Display Start Line Register
The Display Start Line Register is a register to set a display data RAM address corresponding to the COM_0 display line (the top line normally) for the vertical scroll on the LCD, Page address change and so forth. The Display Start Line Address set instruction sets the 8-bit display start address into this register.

(1-3) Line Counter
Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6679**.

(1-4) Column Address Counter
Column Address Counter is the 8-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Figure 1. The counter is incremented automatically after the display data read/write instructions execution. When the Column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Page Address Register.
By the address inverse instruction (ADC select) as shown in Figure 1, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Page address Register
Page Address Register assigns the page address of the display data RAM as shown in Figure 1. In case of accessing from the MPU with changing the page address, Page Address Set instruction is required.

(1-6) Display Data RAM
The Display data RAM (DD RAM) is the bit map RAM consisting of 25,344 bits to store the display data corresponding to the LCD pixel on LCD panel.

The DD RAM data and the state of the LCD:
In Normal Display : “1”=Turn-On Display, “0” =Turn-Off Display
In Reveres Display : “1”=Turn-Off Display, “0” =Turn-On Display

DD RAM output 132 bits parallel data addressed by line address counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the CPU and latch to the display data latch operation are done independently.

(1-7) Common Driver Assignment
This circuit determines the scanning direction of the common output.

Table 1

	COM Outputs Terminals				
PAD No.	62	125		258	321
Pin name	C_0	C_{63}		C_{127}	C_{64}
Ver.A	COM_0 →	COM_{63}		COM_{127} ←	COM_{64}
Ver.B	COM_{127} ←	COM_{64}		COM_0 →	COM_{63}

The Mask fixes the common scanning direction between version A and B that can not be changed by the instruction.

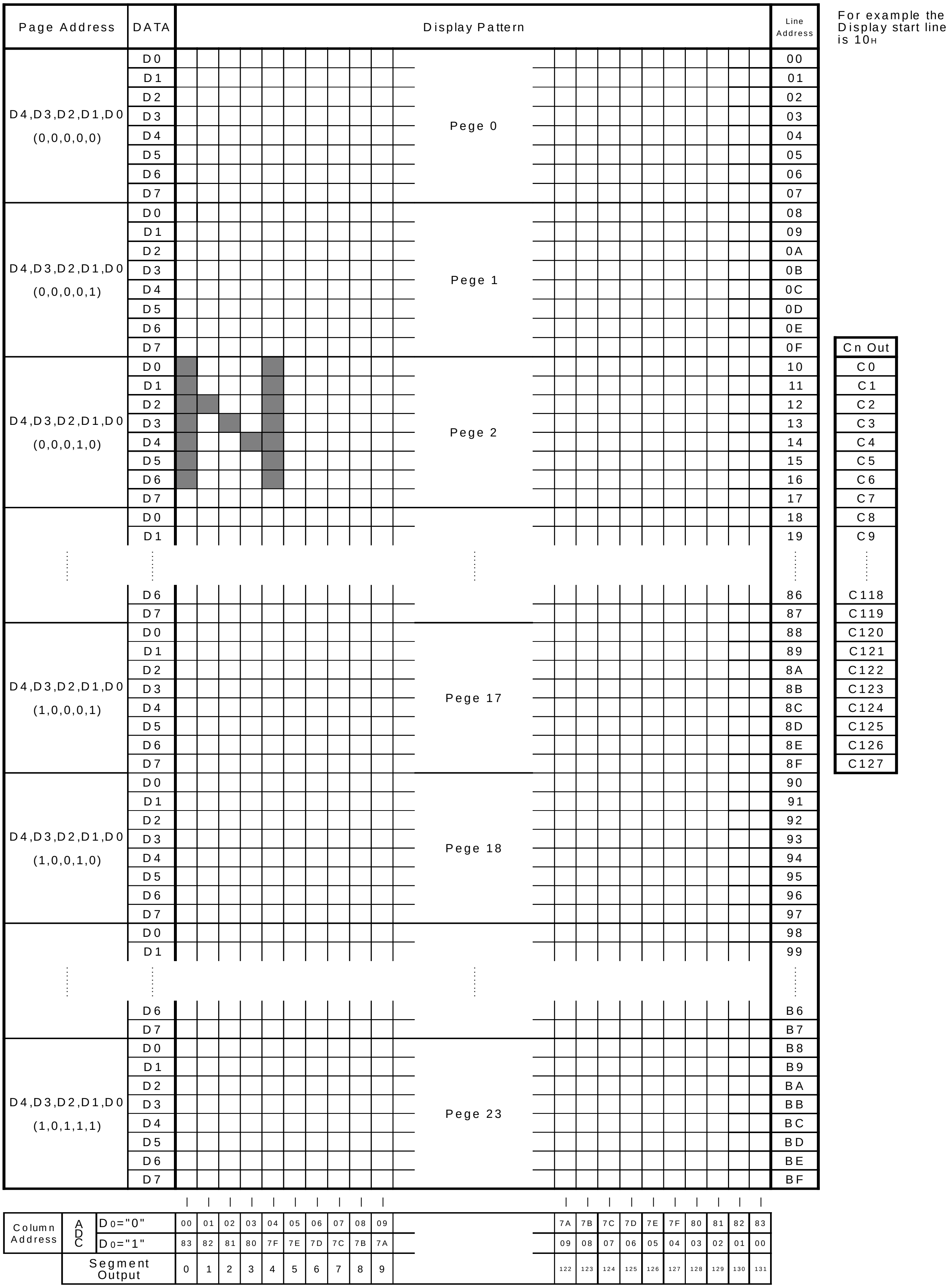


Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit
When the input signal to $\overline{RES}$ terminal goes to “L”, the reset circuit executes initialization as below;

The Initialization state (default)

1 Display Off
2 Normal Display (not inverse)
3 ADC Select : Normal (ADC Instruction D_0 =”0”)
4 Read Modify Write Mode Off
5 Voltage Booster off, Voltage Regulator off, Voltage follower off
6 Static Drive Off
7 Driver Output Off
8 Clear the data of serial interface register
9 Set the Column Address Counter to 00_H
10 Set the Display Start Line Register to 00_H
11 Set the Page Address Register to page “0”
12 Set the EVR register to FF_H
13 Set the Partial Display(1/128 duty)
14 Set the Bias select(1/12 Bias)
15 Set the Voltage Booster(6 times)
16 Set the n-line inverse register to 0_H

The $\overline{RES}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in “ the MPU interface “ in the Application Circuit section. The “L” level input signal as reset signal must keep the period over than 10us as shown in DC Characteristics. The **NJU6679** takes 1us for the reset operation after the rising edge of the $\overline{RES}$ signal.
The reset operation by $\overline{RES}$ =”L” initializes each resister setting as above reset status, but the internal oscillation circuit and output terminals (D0 to D7) are not affected.
To avoid the lock-up, the reset operation by the $\overline{RES}$ terminal must be required every time when power terns on.
The reset operation by the reset instruction, function 9 to 16 operations mentioned above is performed.
The $\overline{RES}$ terminal must be keep “L” level when the power terns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving Circuit
(a) LCD Driving Circuits
LCD driver is 260 sets of multiplexer consisting of 132 segments and 128 commons drivers to output LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in ■LCD DRIVING WAVEFORM.

(b) Display Data Latch Circuits
Display Data Latch Circuit latches the 132-bit display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display, Display On/Off, Static drive On/Off instruction processes only stored data in this Display Data Latch Circuit.

(c) Signal forming to Line Counter and Display Data Latch Circuit
The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 132 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to LCD driving circuits.
The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(d) Display Timing Generation Circuit
The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

(e)Common Timing Generator

The Common Timing Generator generates the common timing signal from the display clock (CL).

-2-frame alternating drive mode

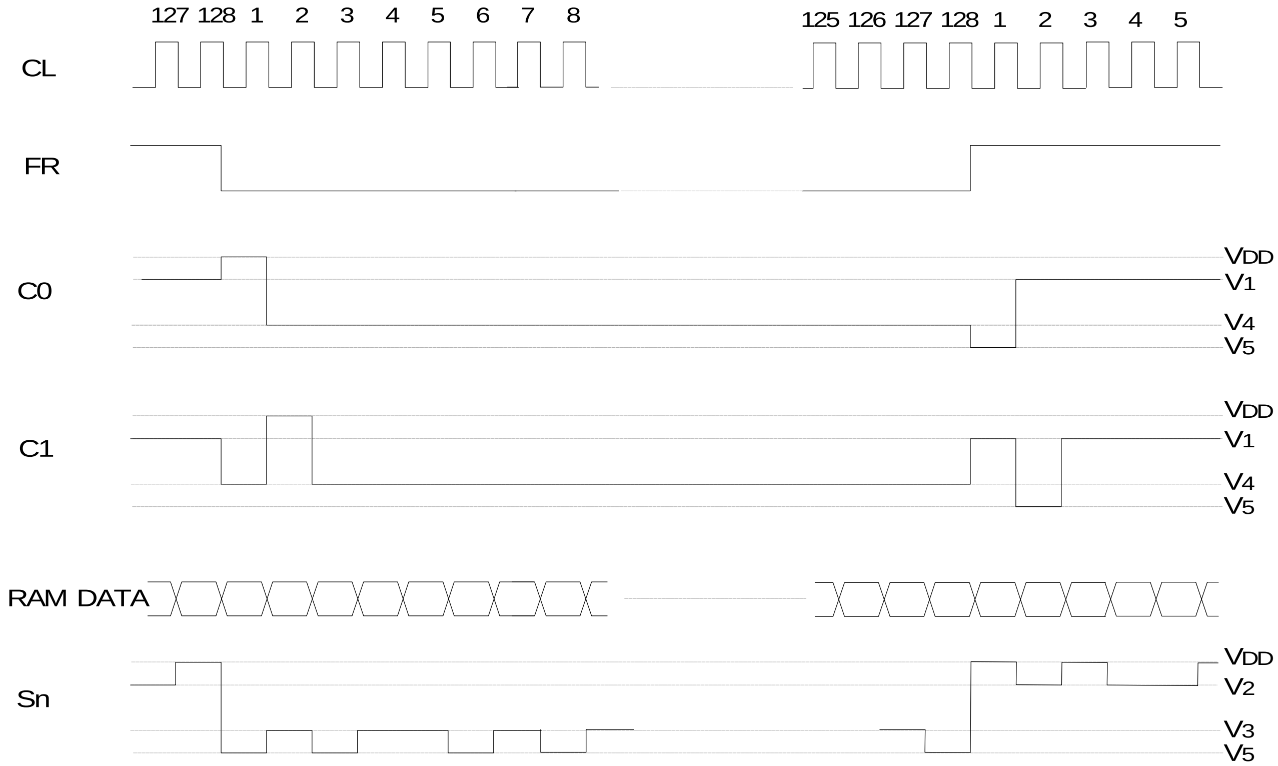


Fig.2

-n-line inverse drive mode (n=7, line inverting register sets to 6)

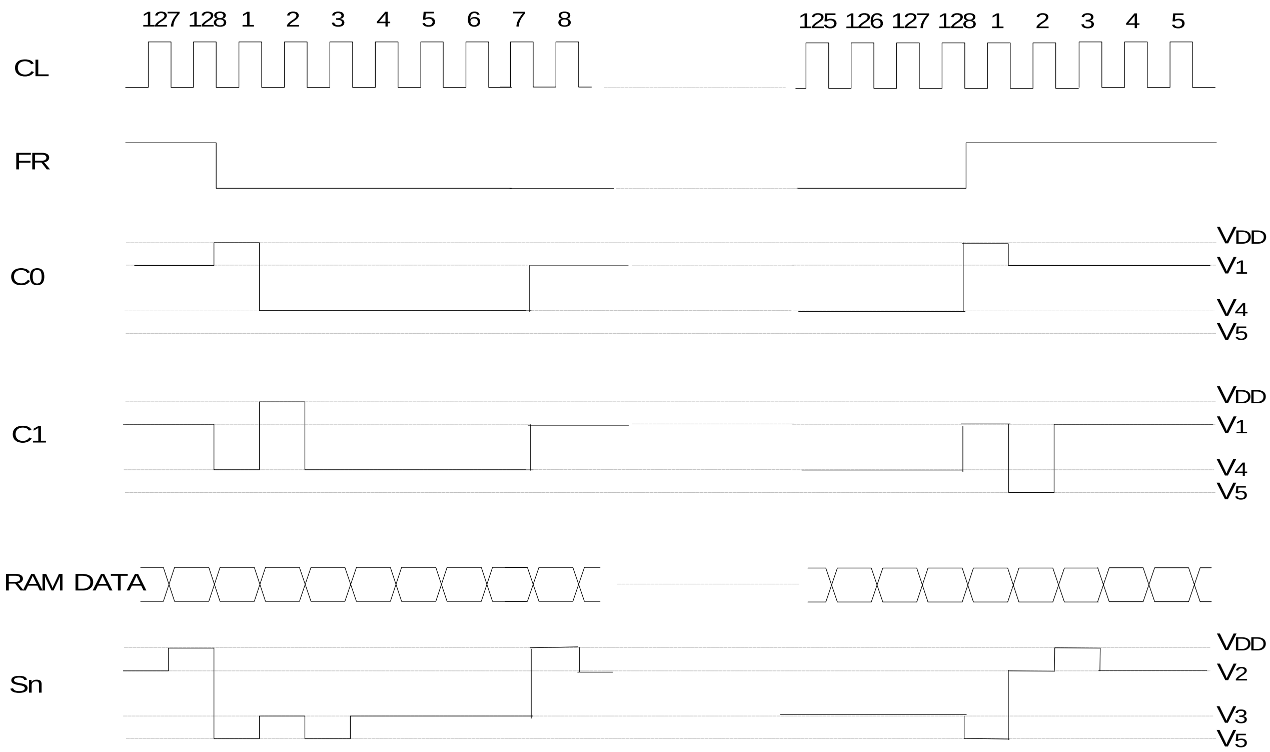


Fig.3

(f) Oscillation Circuit
The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

-The relation between duty and divide

Table 2

Duty	1/8	1/16	1/24	1/32	1/40	1/48	1/56	1/64	1/72	1/80,88	1/96,104	1/112,120,128
Divide	1/64	1/32	1/21	1/16	1/12	1/10	1/9	1/8	1/7	1/6	1/5	1/4

(g) Power Supply Circuit
The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (from 2 times to 6 times), voltage regulator circuits, and voltage followers.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4,V_5 and V_{OUT} for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, $C4^+$, $C4^-$, $C5^+$, $C5^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

Table 3

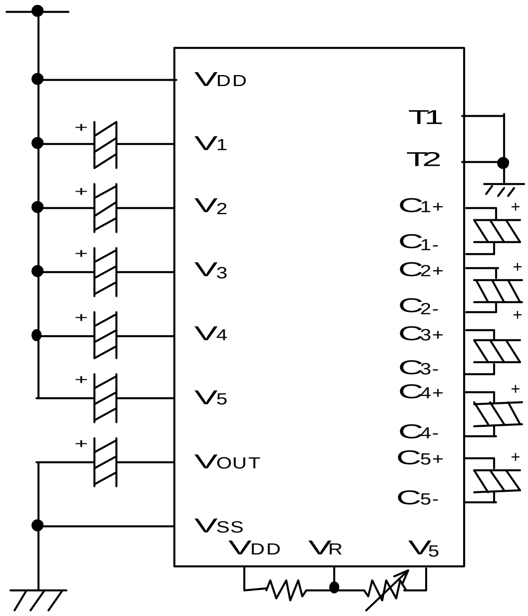
T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Pow Supply	C_{1+},C_{1-} to C_{5+},C_{5-}	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5,V_{OUT}	Open	Open

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$,$C3^+$, $C3^-$, $C4^+$, $C4^-$, $C5^+$, $C5^-$ terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.
When (T_1, T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

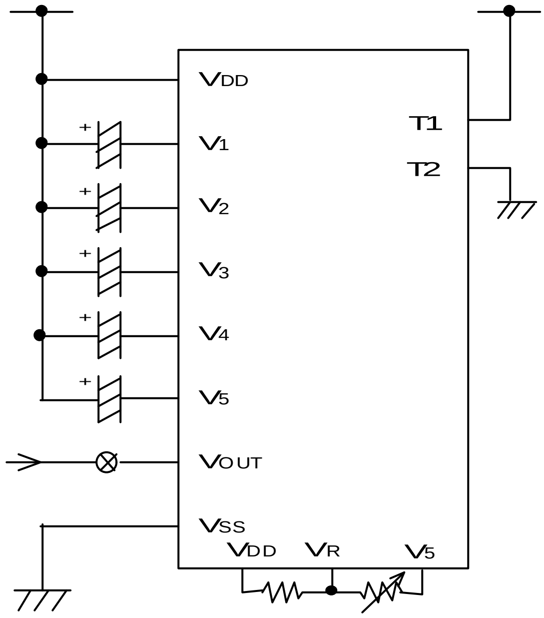
The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6679** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition..
To keep good display condition, external component of the capacitors connecting to the V1 to V5 terminals and voltage booster circuits and the feedback resistors for the V5 operational amplifier must fix each optimized constant after checking various display patterns on LCD panel actually in the application.

○Power Supply applications

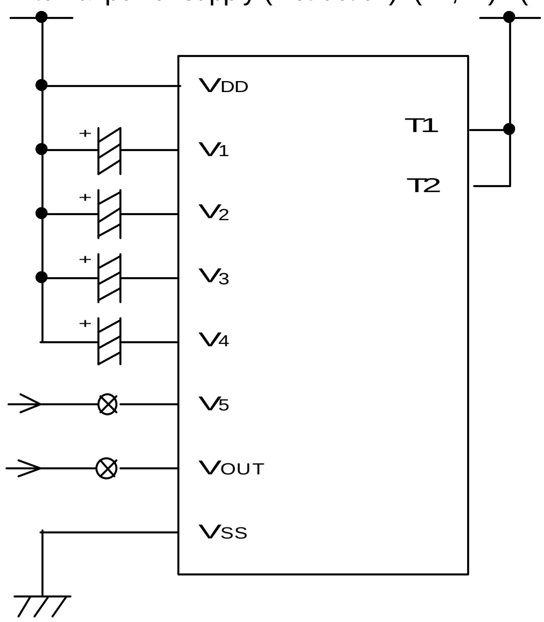
(1) Internal Power Supply Example.
All of the Internal Booster, Voltage Regulator, Voltage Follower using.
Internal power supply ON (instruction) (T1,T2)=(L,L)



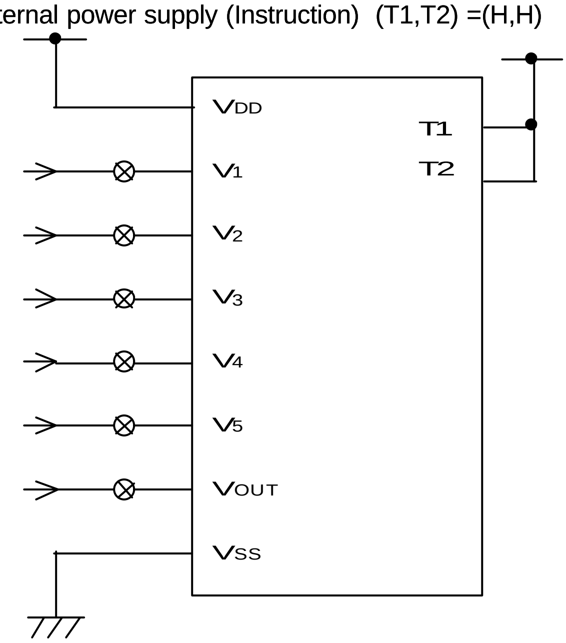
(2) Only V_{OUT} Supply from outside Example.
Internal Voltage Regulator, Voltage Follower using
Internal power supply ON (Instruction) (T1,T2) = (H,L)



(3) V_{OUT} and V5 supply from outside Example.
Internal Voltage Follower using.
Internal power supply (Instruction) (T1,T2) =(H,H)



(4) External Power Supply Example
All of V1 to V5 and V_{OUT} supply from outside
Internal power supply (Instruction) (T1,T2) =(H,H)



⊗ : These switches should be open during the power save mode.

(2) Instruction

The **NJU6679** distinguishes the data on the data bus D0 to D7 as an instruction by combination of A0, $\overline{RD}$, and $\overline{WR}$(R/W) signals. The decoding of the instruction and exection performes with only high speed internal timing without relation to the external clock. Therefore, no busy flag check required normally. In case of the serial interface, the data input as MSB(D7) first serially. Table.4 shows the instruction codes of the **NJU6679**.

Table 4. Instruction Code (*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(a)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display ON/OFF 0:OFF 1:ON
(b)	Display Start Line Set High Order 4bits	0	1	0	0	1	0	1	High Order Address				Determine the Display Line of RAM to the COM0. (Set the Higher order 4bits)
	Display Start Line Set Lower Order 4bits	0	1	0	0	1	1	0	Lower Order Address				Determine the Display Line of RAM to the COM0. (Set the Lower order 4bits)
(c)	Page Address Set High Order 1bits	0	1	0	0	1	0	0	*	*	*	Hi.	Set the Higher order 1bit page of DD RAM to the Page Address Register
	Page Address Set Lower Order 4bits	0	1	0	1	1	0	0	Lower Order Page Address				Set the Lower order 4 bit page of DD RAM to the Page Address Register
(d)	Column Address Set High Order 4bits	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(e)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(f)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(g)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(h)	Normal or Inverse ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the ON and OFF Display 0:Normal 1:Inverse
(i)	Static Drive ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(j)	Sub instruction table mode	0	1	0	0	1	1	1	0	0	0	0	Set the Sub instruction table.
Sub Inst.	(k)Partial Display												
	1st Block, Set Start display unit	0	1	0	0	0	0	0	Start display unit				Set the Start display unit of 1st Block.
	1st Block, Set The number of display units	0	1	0	0	0	1	number of display units					Set the number of display units of 1st Block.
	2nd Block, Set Start display unit	0	1	0	1	1	0	0	Start display unit				Set the Start display unit of 2nd Block.
	2nd Block, Set The number of display units	0	1	0	1	1	1	number of display units					Set the number of display units of 2nd Block.
	Partial display on	0	1	0	0	1	0	0	0	0	0	0	It comes off the mode to set and a display is executed.
	(l)n-line Inverse Drive Set												
	Register Set Higher order 2 bits	0	1	0	0	1	0	1	*	*	higher order		Set the number of inverse drive line.
	Register Set Lower order 4 bits	0	1	0	0	1	1	0	Lower order				Set the number of inverse drive line.
	n-line Inverse Drive Set is executed.	0	1	0	0	1	1	1	0	0	0	0	The execution of the line inverse drive.
	(m)EVR Register Set												
	EVR Register Set Higher order 4 bits	0	1	0	1	0	0	0	EVR Data Higher order				Set the V_5 output level to the EVR register. (Higher order 4 bits)
	EVR Register Set Lower order 4 bits	0	1	0	1	0	0	1	EVR Data Lower order				Set the V_5 output level to the EVR register. (Lower order 4 bits)
	EVR Register Set is executed.	0	1	0	1	0	1	0	0	0	0	0	The execution of the EVR.
(n)	End of sub instruction table mode	0	1	0	0	1	1	1	0	0	0	1	It ends the setting of sub instruction table.

(*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(o)	Bias Select	0	1	0	1	0	1	1	Bias				Select the bias (9 Patterns)
(p)	Boost Level Select	0	1	0	0	0	1	1	0	Boost Multiple			Set the Booster circuits
(q)	Read Modify Write /End	0	1	0	1	1	1	0	0	0	0*	0/1	Read Modify Write mode D0=0:On D0=1:End
(r)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(s)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	0	0	0/1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(t)	Driver Outputs ON/OFF	0	1	0	0	0	1	0	0	0	1	0/1	D0=0: LCD Driver Outouts OFF D0=1: LCD Driver Outputs ON
(u)	Power Save (Complex Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power Save Mode (LCD Display OFF +Static Drive ON)
(v)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment D0=0:Normal D0=1:Inverse

(2-1) Explanation of Instruction Code

(a) Display On/Off
It executes the ON/OFF control of the whole display without relation to the DD RAM or any internal conditions.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off
1:Display On

(b) Display Start Line
It sets the DD RAM line address corresponding to the COM0 terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	A_7	A_6	A_5	A_4
0	1	0	0	1	1	0	A_3	A_2	A_1	A_0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Line Address(HEX)
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
			:					:
			:					:
1	0	1	1	1	1	1	1	BF

(c) Page Address Set
When MPU access to the DD RAM, a page address is set by page Address Set instruction before writing the data. (Note: the change of page address is not affected to the display.)

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	*	*	*	A_4
0	1	0	1	1	0	0	A_3	A_2	A_1	A_0

(*:Don't Care)

A_4	A_3	A_2	A_1	A_0	Page
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	0	1	1	1	23

(d) Column Address

When MPU accesses to the DD RAM , the row address set by Page Address Set instruction is required with the column address before writing the data. The column address set requires twice address set which are higher order 4 bits address set and lower order 4 bits.
When the MPU access to the DD RAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Higher Order
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower Order

A7	A6	A5	A4	A3	A2	A1	A0	Column Address(HEX)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
				:				:
1	0	0	0	0	0	1	1	83

(e) Status Read

This instruction reads out the internal status of "BUSY", “ADC", "ON/OFF" and "RESET" described as follows.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
All instructions can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0 :Counterclockwise Output (Inverse)
1 :Clockwise Output (Normal)
(Note) The data "0=Inverse" and "1=Normal" of ADC status is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing by $\overline{RES}$ terminal signal or reset instruction.
0 : Not Reset status
1 : In the Reset status

(f) Write Display Data
It writes the data on the data bus into the DD RAM. column address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuously without the address setting at every writing time once the starting address is set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

(g) Read Display Data
This instruction reads out the 8-bit data from DD RAM addressed by the column and the page address. The column address automatically increments after the 8-bit data read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see “(4-4) Access to the DD RAM and the Internal Register”).
In the serial interface mode, the display data is unable to read out.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(h) Normal or Inverse On/Off Set
It changes the display condition of normal or reverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D 0 : Normal RAM data "1" correspond to "On"
1 : Inverse RAM data "0" correspond to "On"

(i) Static Drive
This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the "Normal or Inverse On/Off Set" Instruction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D 0 : Normal Display
1 : Whole Display turns On

When the “Static Drive ON” instruction is executed at Display OFF status, the **NJU6679** operates in Power Save Mode. (Refer “ Power Save Mode “)

(j) Sub Instruction table mode

This instruction switches the instruction table from the main to the sub. The sub instruction table contains instructions of partial display, n-line inverse drive set and EVR register set as mentioned in (k), (l) and (m).
The instruction of sub instruction table mode must be executed before above 3 sub instructions execution. The instruction of end of sub instruction table mode (n) switches the instruction table from the sub to the main. If any main instructions are written in the sub instruction mode, the **NJU6679** will malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

-Set sub Instruction table flow is shown below:

Sub Instruction table mode	Switches to Sub instruction table mode.
Set sub instructions.	
End of Sub Instruction table mode.	Switches to Main instruction mode.

(k) Partial Display

It selects two active display areas on the LCD Panel partially. The display area is divided to 16 units with four commons each and selected two display blocks by setting Unit number and number of Unit required (not overlap, not over than 16 units) to display on the LCD panel. These two display blocks are assigned optionally on the LCD panel. Duty selects an adapted ratio number corresponding to the total number of two display blocks automatically.
Partial Display function adjusts the LCD driving voltage, Voltage boosting times and E.V.R level by the instruction to generate the optimum LCD driving voltage for display quality. As result, the operating current is reduced.

· Display Unit Structure

UNIT	0	(8 commons)
UNIT	1	
UNIT	2	
UNIT	3	
UNIT	4	
UNIT	5	
UNIT	6	
UNIT	7	
UNIT	8	
UNIT	9	
UNIT	10	
UNIT	11	
UNIT	12	
UNIT	13	
UNIT	14	
UNIT	15	(8 commons)

128-common

132-segment

Partial display instruction

When Partial Display functions, both of Top Unit Number of display area (the Start Unit) and the number of the effective continuous unit (Display Unit) from the Start Unit for the first display block and the second. Attention that the first display block and the second definition must not be overlap of display area and not be over than 16 units in total.

In case of whole display (1/128 duty), the first display block defines Start Unit=0 (0,0,0,0) and Display Unit = 16 (1,0,0,0,0) for all of display area selection. In this time, the definition of the second display block is ignored.
In case of only the first block display, the second display block defines Start Unit=0 (0,0,0,0) and Display Unit = 0 (0,0,0,0,0) for no display area.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1st Block	0	1	0	0	0	0	0	D	D	D	D	Start unit
	0	1	0	0	0	1	D	D	D	D	D	The display unit number
2nd Block	0	1	0	1	1	0	0	D	D	D	D	Start unit
	0	1	0	1	1	1	D	D	D	D	D	The display unit number

By input following instruction, the duty ratio is changed automatically and executes the partial display function.

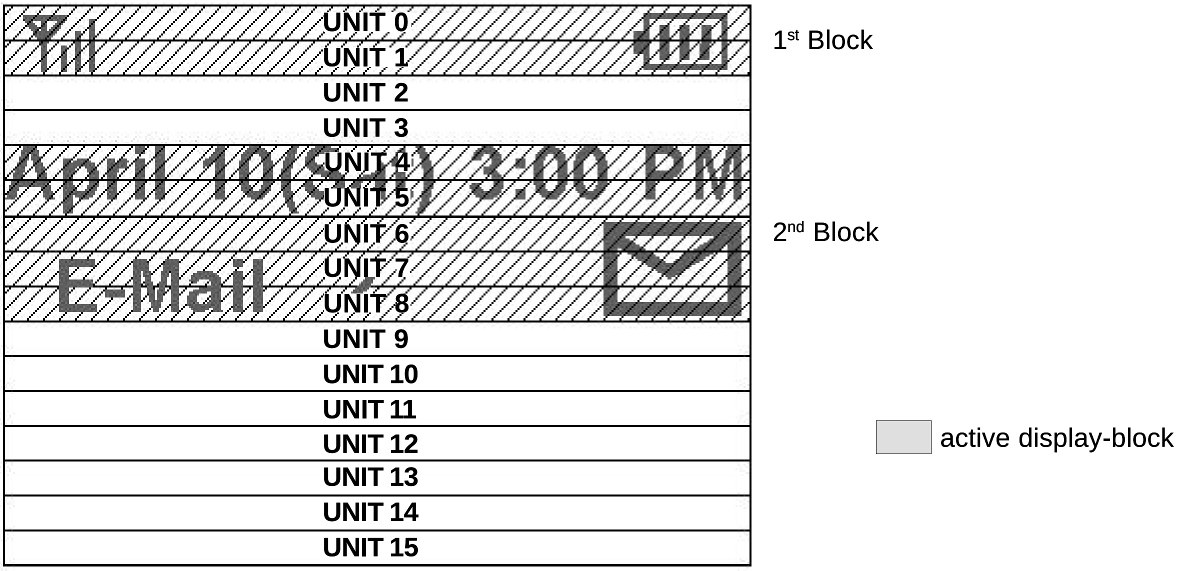
0	1	0	0	1	0	0	0	0	0	0	Partial display on

D :unit number (Hex.)

Notes) Attention followings due to prevent from mulfunction

- The input order of Partial Display instructions must follow above.
- Prohibits the overlap of the 1st partial display block and the 2nd.
- The Start Unit of the 1st partial display block must not be over 15.
- The total Display Unit Number (the sum of the 1st and 2nd partial display block Unit Num ber) must not be over 16.
- On the LCD panel, no active display area inserts between the 1st display block and the 2nd. However, the display data of the 1st display block and the 2nd must store continuously in the display data RAM.

Example of the Partial Display setting.



The above partial display condition is set as follows:

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set partial display conditions

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	0	0	0	0	0	1st Block, Set start unit to ”0”
0	1	0	0	0	1	0	0	0	1	0	1st Block, Set the display unit number to ”2”
0	1	0	1	1	0	0	0	1	0	0	2nd Block, Set start unit to ”4”
0	1	0	1	1	1	0	0	1	0	1	2nd Block, Set the display units number to ”5”
0	1	0	0	1	0	0	0	0	0	0	Execute Partial display.

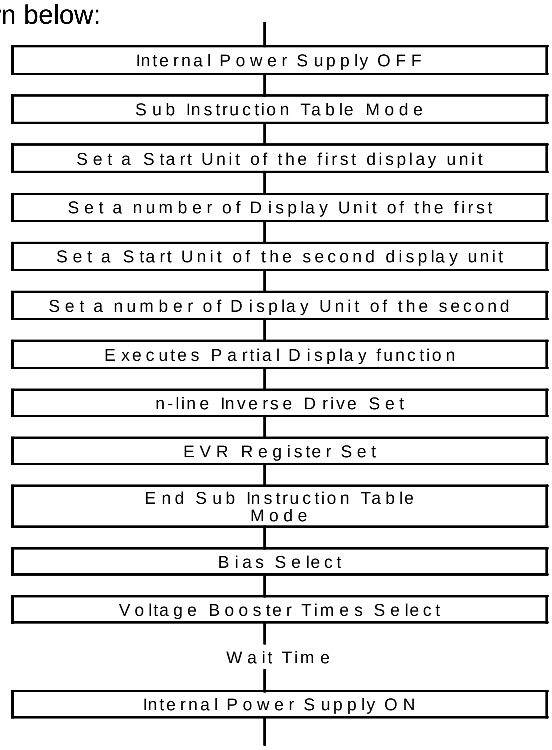
The Duty is changed to 1/56 automatically.

3)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

Duty is changed automatically when Partial Display execution. But LCD Driving Voltage, Bias, Driving form like as 2-frame alternating driving or n-line inverse are not changed. Therefore, Display Off should operate before Partial Display execution for prevention of unexpected display, and Voltage Booster Select instruction, E.V.R Register Set, Bias Select and n-line Inverse Driving Set should set optimum conditions for good display in the mean time of Partial Display instruction execution. The optimum conditions should fix refering the result of actual display eveluation.

-Set Partial Display flow is shown below:



(l) n-line Inverse Drive Mode

n-Line Inverse Register Set (refer +Functional Description Fig.3 n-line Inverse alternative drive mode)
It sets a line number to inverse the polarity of common driver and segment.
The instructions must be input in order of followings. These instructions are sub instruction sets and must be set after (j)Sub instruction table mode.

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set n-line Inverse number

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	0	1	*	*	A5	A4	Higher order
0	1	0	0	1	1	0	A3	A2	A1	A0	Low order

A5	A4	A3	A2	A1	A0	Inverse line
0	0	0	0	0	0	-(*)
0	0	0	0	0	1	2
			:			:
1	1	1	1	1	1	64

(*:2-frame alternating drive mode.)

3)Execute the n-line Inverse

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

4)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(m) EVR Register Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage "V5". By data setting into the EVR register, the LCD driving voltage "V5" selects out of 201 steps of regulated voltage. The voltage adjustable range of "V5" is fixed by the external resistors. For details, refer the section "(3-2) Voltage Adjust Circuits".

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set EVR Register

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A7	A6	A5	A4
0	1	0	1	0	0	1	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	VLCD
0	0	1	1	0	1	1	1	Low
			:					:
			:					:
1	1	1	1	1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$

When EVR doesn't use, set the EVR register to (1,1,1,1,1,1,1,1).

3)Execute the EVR

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

4)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(n) End of Sub instruction table mode

"End of sub instruction table mode" instruction switches instruction table from sub to main.
(k)Partial display, (l)n-line inverse drive mode, and (m)EVR are sub instruction sets on the sub instruction table. The instruction of "END of sub instruction mode" must be set after these sub instruction sets. The **NJU6679** may occur incorrect operation if any main instructions on the main instruction table are input in mode of sub instruction table.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	1

(o) Bias Select

This instruction sets the bias voltage.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

(*:Don't Care)

A3	A2	A1	A0	Bias
0	0	0	0	1/4
0	0	0	1	1/5
0	0	1	0	1/6
0	0	1	1	1/7
0	1	0	0	1/8
0	1	0	1	1/9
0	1	1	0	1/10
0	1	1	1	1/11
1	*	*	*	1/12

(p) Boost Level Select

This instruction sets the boost level (2 to 6 times). When “Partial Display Instruction” execution, the “Boost Level Select” also must be executed. If the external capasitors are connected as the lower than 6 times boost level, don’t set the boost level by the instruction over than the boost level by conecting capasitors. If set the boost level over than it, the device will make malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	A2	A1	A0

Command			Booster Multiple				
A2	A1	A0	6times external capacitors connections	5times external capacitors connections	4times external capacitors connections	3times external capacitors connections	2times external capacitors connections
0	0	0	2-time				
0	0	1	3-time	2-time			
0	1	0	4-time	3-time	2-time		
0	1	1	5-time	4-time	3-time	2-time	
1	*	*	6-time	5-time	4-time	3-time	2-time

(q) Read Modify Write/End

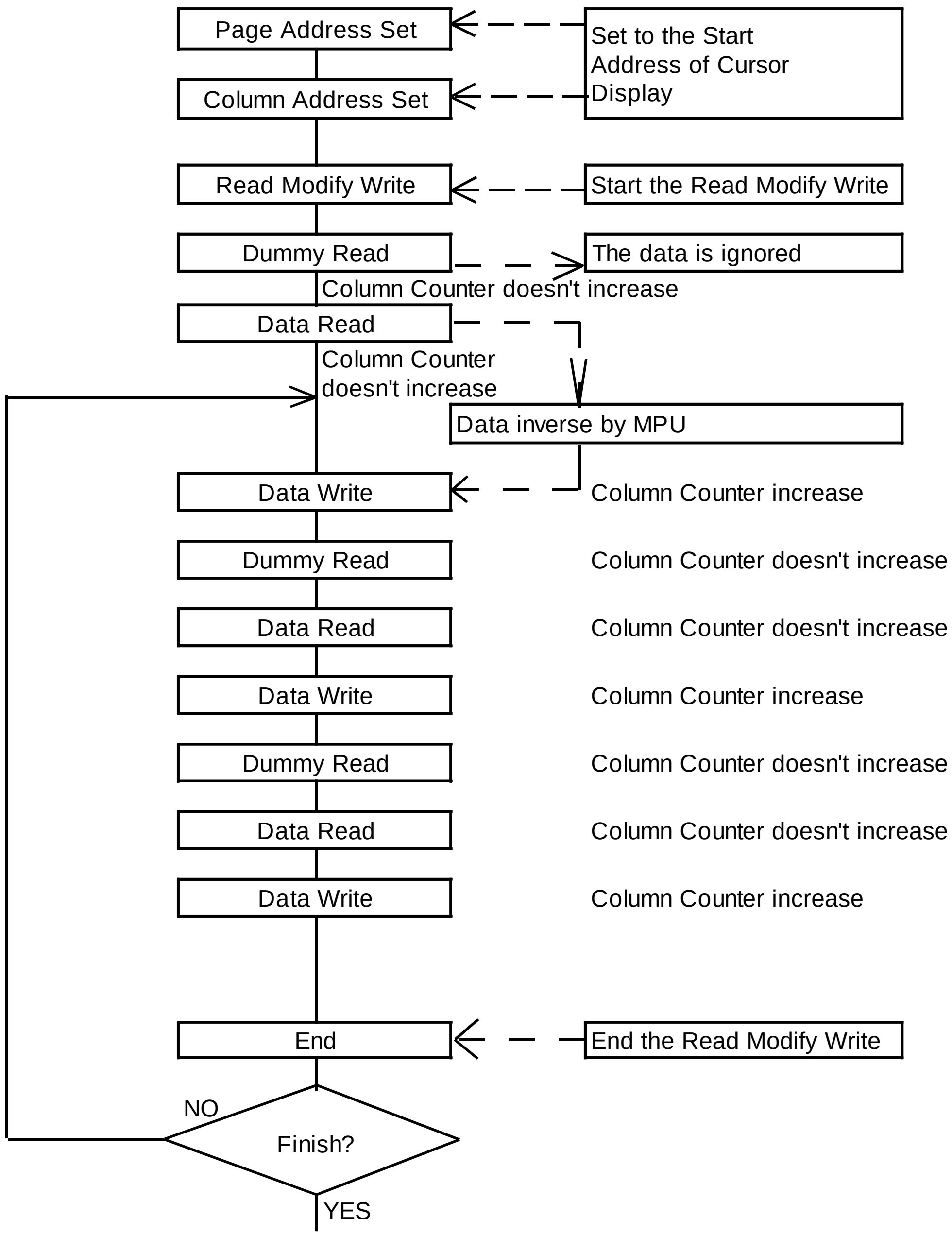
This instruction sets the Read Modify Write controlling the page address increment. In this mode, the Column Address only increments when execute the display data “Write” instruction; but no change when the display data “Read” Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Adddress goes back to the start address before the execution of this “Read Modify Write” instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink).

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	D

D 0 : Read Modify Write On
1 : End

Note) In this “Read Modify Write” mode, out of display dara “Read”/”Write”, any instructions except “Column Address Set” can be executed.

- The Example of Read Modify Write Sequence



(r) Reset

This instruction executes the following initialization.
The reset by the reset signal input to the $\overline{RES}$ terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

1 Set the Column Address Counter to 00_H
2 Set the Display Start Line Register to 00_H
3 Set the Page Address Register to page "0"
4 Set the EVR register to FF_H
5 Set the Partial Display(1/128 duty)
6 Set the Bias select(1/12 Bias)
7 Set the Voltage Booster(6 times)
8 Set the n-line inverse register to 0_H

The DD RAM is not affected by this initialization.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

(s) Internal Power Supply ON/OFF

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	D

D 0 : Internal Power Supply Off
1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, V_{DD} and V_{LCD}.
Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the (3-4) Fig.5)

(t) Driver Outputs ON/OFF

This instruction controlls ON/OFF of the LCD Driver Outputs.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	D

D 0 : LCD driving waveform output Off
1 : LCD driving waveform output On

The **NJU6679** implements low power LCD driving voltage generator circuit and requires the following Power Supply ON/OFF sequence.

- LCD Driving Power Supply ON/OFF Sequences

The sequences below are required when the power supply turns ON/OFF.
For the power supply turning on operation after the power-save mode, refer the "power save release sequence" mentioned after.

Turn ON sequence

EVR Register Set

Internal Power Supply ON
or
External Power supply ON

(Wait Time) *1

Drivier Outputs ON

Turn OFF sequence

Display OFF

Whole Display ON

Internal Power Supply OFF
or
External Power Supply OFF

Driver Outputs OFF

NJU6679 Power OFF

*1 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, VLCD=VDD-V5, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time correctly, test by using the actual LCD module.

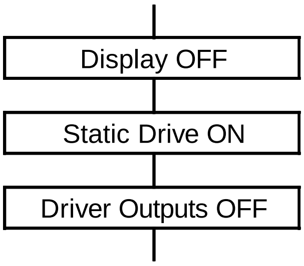
(u) Power Save (complex comand)

When Static Drive ON at the Display OFF status (inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current.
The internal status in the Power Save Mode is shown as follows;

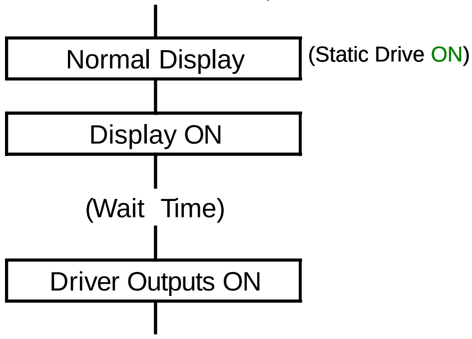
1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage (V1 to V5) is fixed to the V_{DD} level.

The power save and its release perform according to the following sequences.

Power Save Sequence



Power Save Release Sequence



The **NJU6679** constantly spends the current without the execution of the Driver Outputs OFF instruction. The LCD drive waveform is not output until the Driver Outputs ON instruction is executed.

*1 In the Power Save sequence, the Power Save Mode starts after the Static Drive ON command is executed.
*2 In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
*3 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5. To know the rise time cor rectly, test by using the actual LCD module.
*4 LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
*5 In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage. In this time, V_{OUT} terminal also should be made codition like as disconection or connection to V_{SS}.

(v) ADC Select

This instruction determines the correspondence of Column in the DD RAM with the Segment Driver Outputs. Segment Driver Output order is inversed when this instruction executes, therefore, the placement the **NJU6679** against the LCD panel becomes easy.

A0	$\overline{RD}$	R/W $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

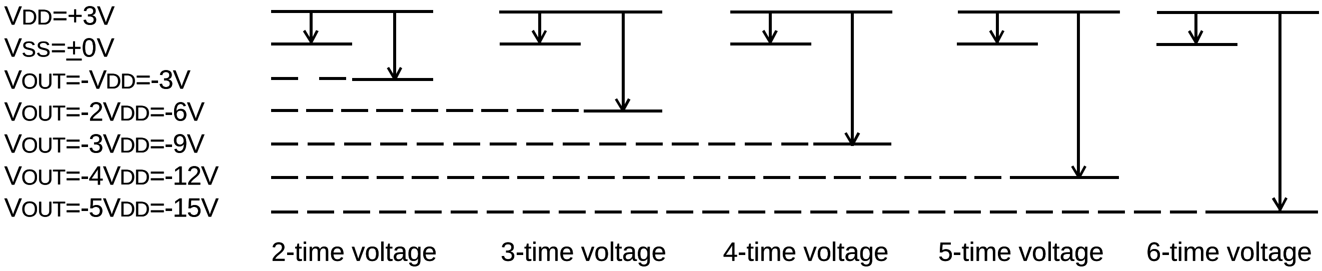
D 0 : Clockwise Output (Normal) Segment Driver S_0 to S_{131}
1 : Counterclockwise Output (Inverse) Segment Driver S_{131} to S_0

(3) Internal Power Supply

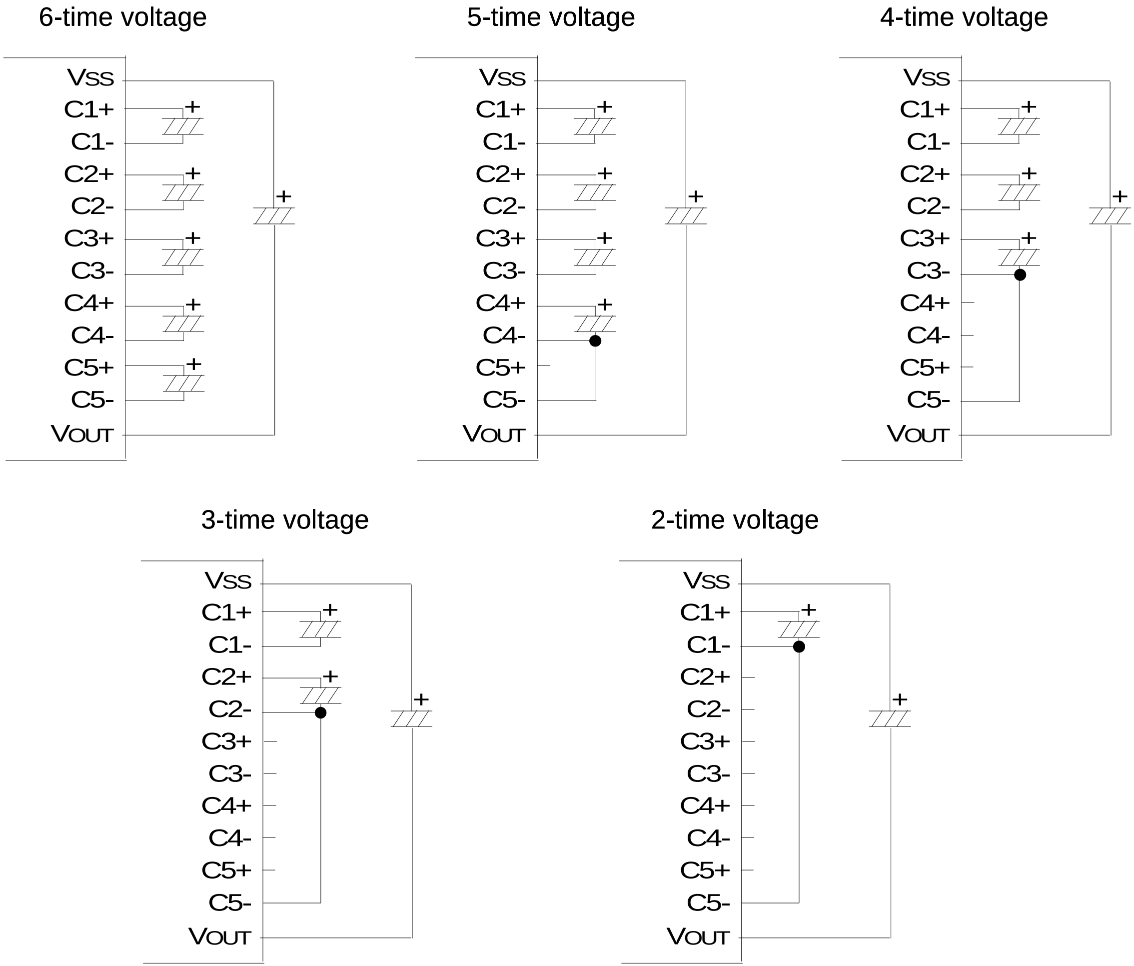
(3-1) 6-time voltage booster circuits

The 6-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 6 times of VDD-VSS from the VOUT terminal with connecting the six capacitors between C_1^+ and C_1^-, C_2^+ and C_2^-, C_3^+ and C_3^-, C_4^+ and C_4^-, C_5^+ and C_5^-, and V_{SS} and V_{OUT}. The boosting time is selected out of 2 times to 6 by the combination of changing the external capacitors connection and “Booster Level Select” instruction. (refer (2-1)Instruction (p)Voltage Boost time select)
Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal, therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.
The boosted voltage of V_{DD}-V_{OUT} must be 18V or less.
The boost voltage and the capacitor connection are shown below.

● The boosted voltage and V_{DD},V_{SS}



● Example of the external capacitor connection to the voltage booster circuits



(3-2)Voltage Adjust Circuits

The boosted voltage of V_{OUT} outputs V5 for LCD driving through the voltage adjust circuits. The output voltage of V5 is adjusted by Ra and Rb within the range of |V5| < |V_{OUT}|.
The output is calculated by the following formula(1).

$$V_{LCD} = V_{DD}\text{-}V_5 = (1+Rb/Ra)V_{REG} \qquad (1)$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder registance. V_{REG} is adjustable by EVR functions (see section 3-3).
For minor adjustment of V5, it is recommended that the Ra and Rb is composed of R2 as variable resistor and R1 and R3 as fixed resistors, constant should be connected to V_{DD} terminal,VR and V5 ,as shown below.

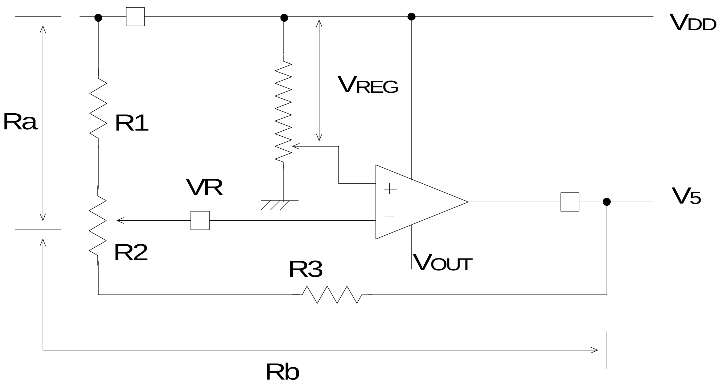


Fig. 4

< Design example for R1, R2 and R3 /Reference >
•R1+R2+R3=6MΩ
(Determind by the current between V_{DD}-V5)
•Variable voltage range by the R2. -7V to -11V (V_{LCD}=V_{DD}-V5 : 10V to 12V)
(Determind by the LCD electrical characteristics)
•VREG=3V
(In case of V_{DD}=3V and EVR=FFh)

R1,R2 and R3 are calculated by above conditions and the fomula of (1) to below;
R1=1.5MΩ
R2=0.3MΩ
R3=4.2MΩ

Note) V5 voltage is generated referencing with VREG voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above figure. Therefore, V_{LCD} (V_{DD}-V5) is affected including the gain (Rb/Ra) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V5 stable operation.

(3-3) Contrast Adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 201 conditions by setting 8-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V5.
A step with EVR is set like table shown below.
37_H to $4F_H$ available for use. If keeping 3% precision, sets EVR over $4F_H$.

EVR register		V_{REG}[V]	V_{LCD}
$3F_H$	(0,0,1,1,0,1,1,1)	(100/300) x (V_{DD}-V_{SS})	Low
:	:	:	:
$4F_H$	(0,1,0,0,1,1,1,1)	(124/300) x (V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
FD_H	(1,1,1,1,1,1,0,1)	(298/300) x (V_{DD}-V_{SS})	:
FE_H	(1,1,1,1,1,1,1,0)	(299/300) x (V_{DD}-V_{SS})	:
FF_H	(1,1,1,1,1,1,1,1)	(300/300) x (V_{DD}-V_{SS})	High

In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD}=3.0V, V_{SS}=0V
  Ra=1MΩ, Rb=4MΩ (Ra:Rb=1:4)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting $4F_H$ in the EVR register,

$$V_{LCD} = ((Ra+Rb)/Ra)V_{REG}$$
$$= (5/1) \times [(124/300) \times 3.0]$$
$$= 6.2V$$

In case of setting FF_H in the EVR register,

$$V_{LCD} = ((Ra+Rb)/Ra)V_{REG}$$
$$= (5/1) \times [(300/300) \times 3.0]$$
$$= 15.0V$$

	Min.4FH		Max.FFH
Adjustable Range	6.2	--------------------	15.0 [V]
Step Voltagre		50	[mV]

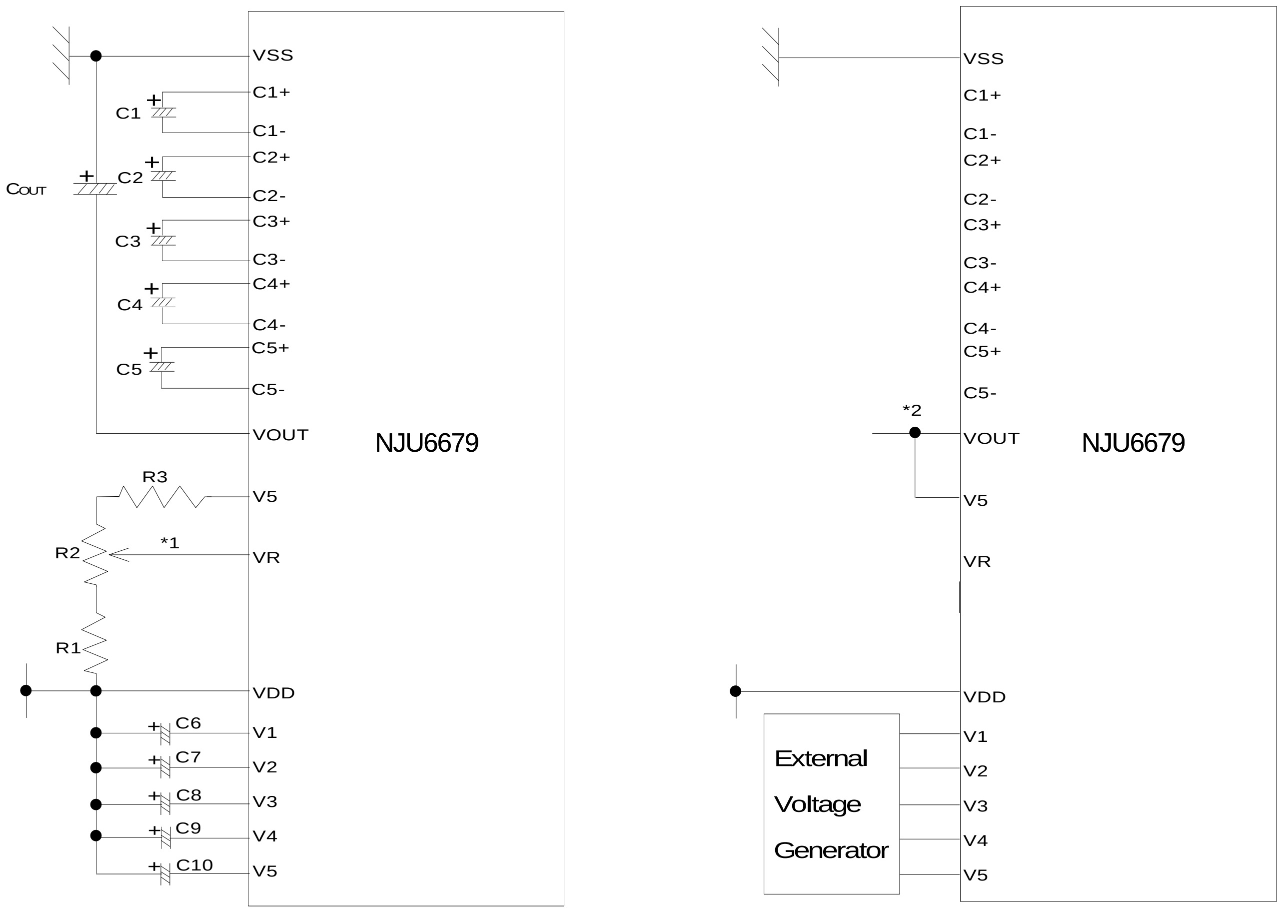
* In case of V_{DD}=3V

(3-4) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V1,V2,V3,V4 are generated by dividing the V5 voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.
As shown in Figure 5, five external capacitors are required to connect to each LCD driving voltage terminal for voltage stabilization. The value of capacitors (C6 to C10) should be determined after the actual LCD panel display evaluation.

Using the internal Power Supply

Using the external Power Supply



Reference set up value $V_{LCD}=V_{DD}-V5$ = 10 to 12V

COUT	to 1uF
C1 to C4, C9	to 1uF
C5 to C8	0.1 to 0.47uF
R1	1.5MΩ
R2	0.3MΩ
R3	4.2MΩ

Fig.5

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.
*2 Following connection of VOUT is required when external power supply using.

When VSS > V5 --- VOUT=V5

When VSS ≦ V5 --- VOUT=VSS

(4) MPU Interface

(4-1) Interface type selection

Two MPU interface types are available in the **NJU6679**: by 1) 8-bit bi-directional data bus (D7 to D0), 2) serial data input (SI:D7). The interface type (the 8 bit parallel or serial interface) is determined by the condition of the P/S terminals connecting to “H” or “L” level as shown in Table 5. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	Hi-Z

Parallel Interface

The **NJU6679** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S=”H”) is selected.
The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to “H” or “L” as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D0 to D7
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

(4-2) Discrimination of Data Bus Signal

The **NJU6679** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
H	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface.(P/S="L")

The serial interface of the **NJU6679** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($\overline{CS}$=L), the input to D7(SI) and D6(SCL) becomes available, and in case that the chip isn’t selected, the shift register and the counter are reset to the initial condition.
The data input from the terminal(SI) is MSB first like as the order of D7, D6, •••D0 by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.
It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0=H” and instruction by A0=”L”. A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.
However,in case of RES=“H” to “L” or $\overline{CS}$=”L” to ”H” with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.
The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

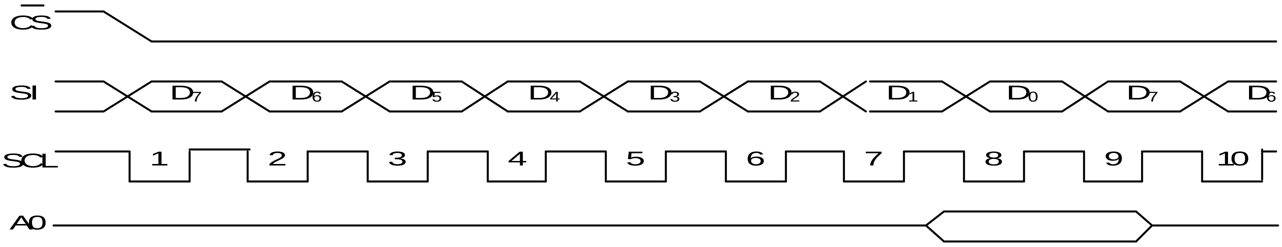


Fig. 6

(4-4) Access to the Display Data RAM and Internal Register.

The **NJU6679** transfers data to the CPU through the bus holder with the internal data bus.
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.
Therefore, the limitation of the access to **NJU6679** from MPU side is not access time (t_{ACC},t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the sutisfy condition in MPU.
When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 7)
The exsample of Read Modify Write operaion is mentioned in (2-1)Instruction –(q)The sequence of Inverse Display.

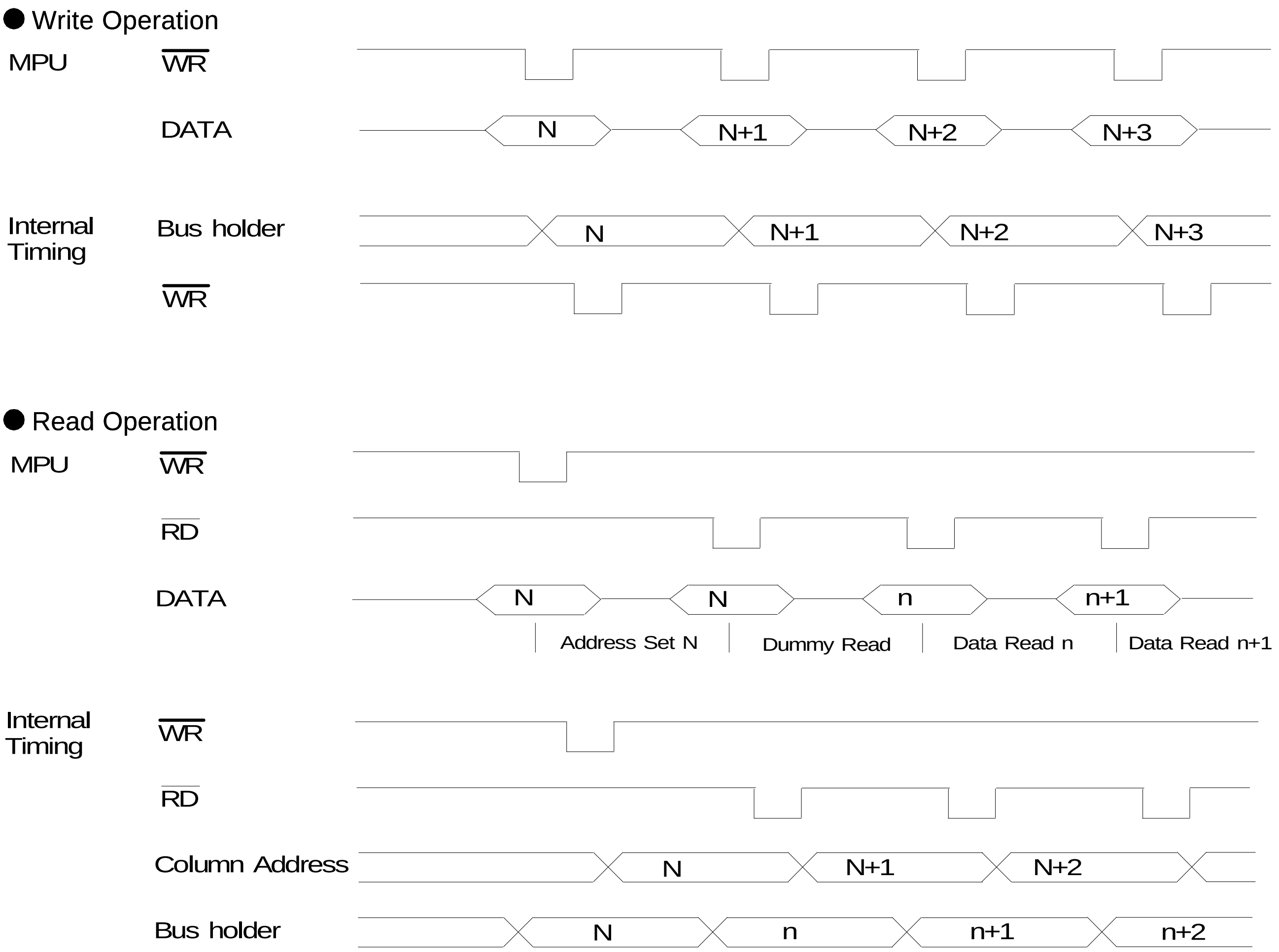


Fig.7

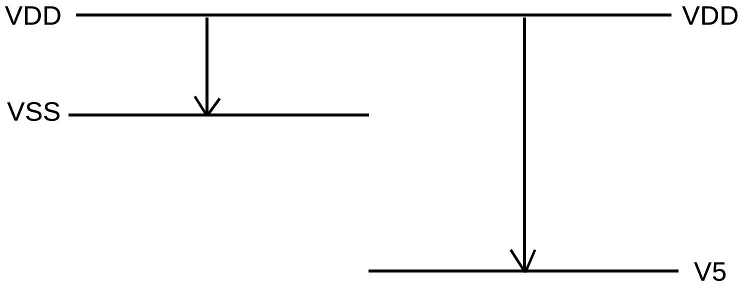
(4-6) Chip Select

$\overline{CS}$ is the Chip Select terminal. In case of $\overline{CS}$="L", the interface with MPU is available.
In case of $\overline{CS}$="H" (Chip is not selected), the terminals of D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, D_7(SI) and D_6(SCL) inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and the counter for the serial interface are reset.
However, the reset signal is always input and executed in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	-0.3 to +5.0	V
Supply Voltage (2)	V_5	V_{DD}-18.0 to V_{DD}+0.3	V
Supply Voltage (3)	V_1 to V_4	V_5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30 to +80	°C
Storage Temperature	T_{stg}	-55 to +125 (Chip)	°C
		-55 to +100 (TCP)	



Note 1) All voltage values are specified as V_{SS}=0V.

Note 2) The relation of V_{DD}≥V1≥V2≥V3≥V4≥V5>VOUT;V_{DD}>V_{SS}≥V_{OUT} must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to **NJU6679** at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .
In use of the voltage boost circuit, the condition that the supply voltage: 18.0V≥V_{DD}-V_{OUT} is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1)

(VDD=2.7V to 3.3V, VSS=0V, Ta=-30 to +80°C)

PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	Note
Operating Voltage(1)		V_{DD}			2.4		3.6	V	5
OperatingVoltage(2)		V_5			V_{DD}-18.0		V_{DD}-6.0	V	6
		V_1,V_2	V_{LCD}= V_{DD}-V_5		VDD-0.5VLCD		V_{DD}		
		V_3,V_4			V_5		VDD-0.5VLCD		
Input Voltage	High Level	V_{IHC1}	D_0...D_7,A0, CS,RES,RD,WR,SEL68, P/S Terminals		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC1}			V_{SS}		0.2V_{DD}	V	
Output Voltage	High Level	V_{OHC11}	D_0...D_7 Terminals	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC11}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}	V	
Input Leakage Current		I_{LIO}	All Input terminals		- 1.0		1.0	uA	
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=15.0V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Power save Mode			0.05	5	uA	8
Operating Current		I_{DD12}	Display V_{LCD}=15.0V			40	80	uA	
		I_{DD21}	Accessing f $_{CYC}$=200kHz			650	850		9
Input Terminal Capacitance		C_{IN}	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,SEL68, P/S,T1,T2,D_0...D_7 Ta=25°C			10		pF	10
Oscillation Frequency		f_{OSC}	Ta=25°C		31.7	39	46.3	kHz	

Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	11
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	12

Voltage Booster	Output Volt.	V_{OUT1}	V_{SS}-Vout, 6-time voltage booster, V_{DD}=3V	V_{DD}-15.0V		V_{DD}-14.5V	V	
	On-resistance	R_{TRI}	V_{DD}=3V;C_{OUT}=4.7uF 6-time voltage booster		2000	4000	Ω	
	Adjustment range of LCD Driving Volt.	V_{OUT2}	Voltage Booster Circuit "OFF"	V_{DD}-18.0V		V_{DD}-6.0V	V	13
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"	V_{DD}-18.0V		V_{DD}-6.0V	V	
	Operating Current	I_{OUT1}	V_{DD}=3V, V_{LCD}=12V COM/SEG Terminals Open No Access Display Checkered pattern		250	450	uA	14
		I_{OUT2}			45	90		
		I_{OUT3}			35	70		
	Voltage Reg.	$V_{REG\%}$	V_{DD}=3V,Ta=25°C, V_{REG}=4F to FF_H			3	%	

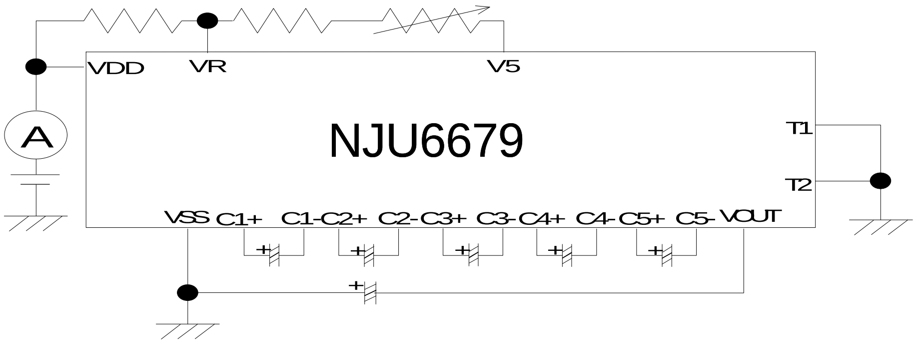
Note 5) Although the **NJU6679** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.
Note 6) The operating voltage when using external power supply.
Note 7) R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V1,V2,V3,V4) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).
Note 8,9) The value of after Driver Output On instruction execution.
Note 8,9) Refers to the current consumption of the IC itself; external power supply is used for the LCD driving. In case of not use internal power supply circuit,meaning current of IC's. LCD driving power supply are external power supply.
Note 8) Applicable in case of not accessing to the MPU.
Note 9) The operating current when writing a vertical stripe pattern on the tcyc. Current consumption during the access is approximately proportional to the access frequency. When not accessed, it consumpts only I_{DD01}
Note 10) Apply to A0, D_0-D_7, $\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,P/S,T_1,T_2 terminals.

Note 11) t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the $\overline{RES}$ signal.
Note 12) Apply minimum pulse width of the $\overline{RES}$ signal. To reset, the "L" pulse over t_{RW} shall be input. .
Note 13) The voltage adjustment circuit controls V5 within the range of the voltage follower operating voltage.
Note 14) Each operating current shall be defined as being measured in the following condition.

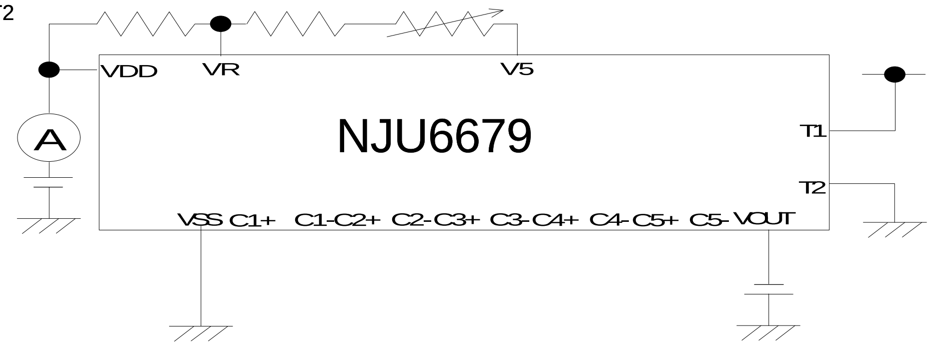
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Booster	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	L/H	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V_5)

MEASUREMENT BLOCK DIAGRAM

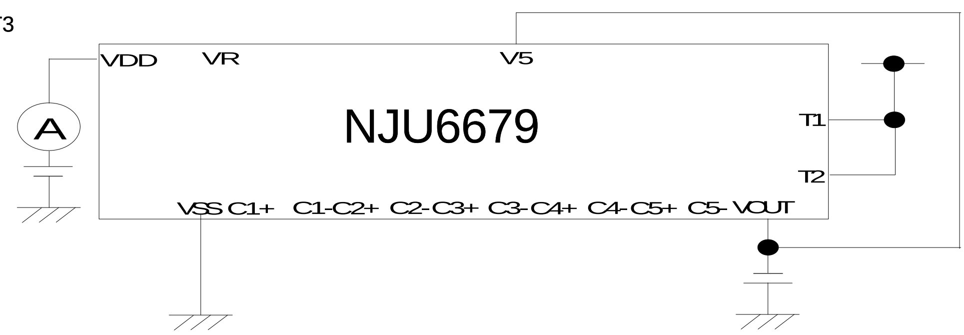
:I_{OUT1}



:I_{OUT2}

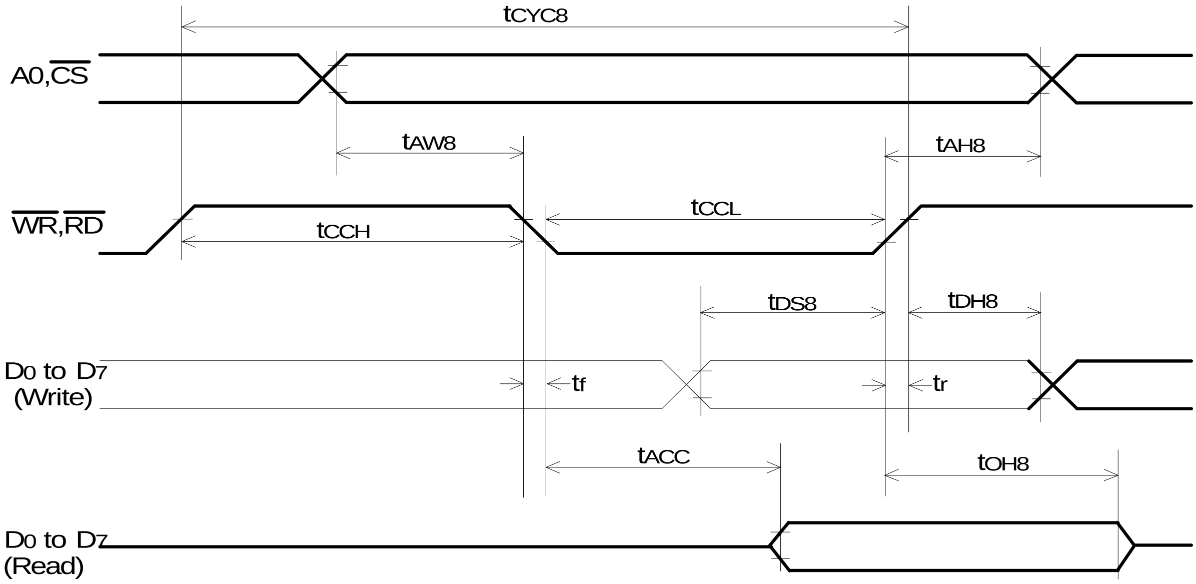


:I_{OUT3}



■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)

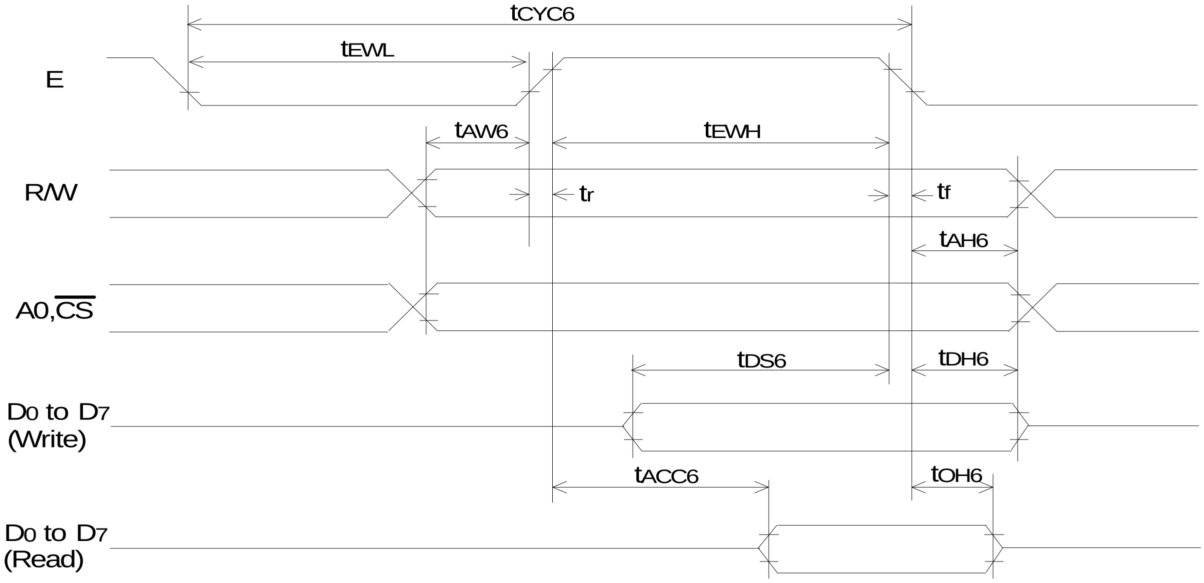


(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,$\overline{\text{CS}}$ Terminals	t_{AH8}	10				ns
Address Set Up Time			t_{AW8}	0				ns
System Cycle Time	WR	$\overline{\text{WR}}$,$\overline{\text{RD}}$ Terminals	t_{CYC8} (W)	270	220			ns
	RD		t_{CYC8} (R)	350				ns
Control Pulse Width	WR,"L"		t_{CCL}(W)	50				ns
	RD,"L"		t_{CCL}(R)	200				ns
	WR,"H"		t_{CCH}(W)	220	160			ns
	RD,"H"		t_{CCH}(R)	150				ns
Data Set Up Time		D0 to D7 Terminals	t_{DS8}	35				ns
Data Hold Time			t_{DH8}	15				ns
$\overline{\text{RD}}$ Access Time			t_{ACC8}			120	CL=100pF	ns
Output Disable Time			t_{OH8}	0		50		ns
Rise Time, Fall Time		$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, A0, D0 to D7 Terminals	t_r,t_f			15		ns

Note 15) All timing based on 20% and 80% of VDD voltage level.

- Read/Write operation sequence (68 Type MPU)



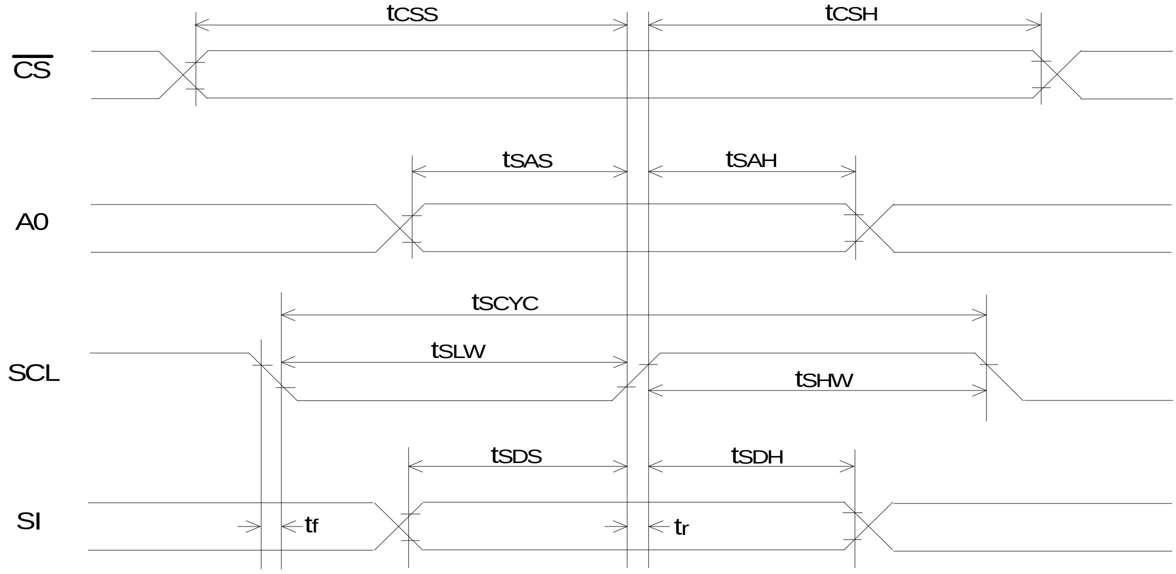
(V_{DD}=2.4V to 3.6V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,$\overline{CS}$,R/W Terminals	t_{AH6}	10				ns
Address Set Up Time			t_{AW6}	0				ns
System Cycle Time(W)			t_{CYC6}(W)	270	220			ns
System Cycle Time(R)			t_{CYC}6(R)	350				ns
Enable Pulse Width	Read"H"	E Terminal	t_{EWH}	200				ns
	Write"H"			50				ns
	Read"L"		t_{EWL}	220	160			ns
	Write"L"			150				ns
Data Set Up Time		D_0 to D_7 Terminals	t_{DS6}	35				ns
Data Hold Time			t_{DH6}	15				ns
Access Time			t_{ACC6}			200	CL=100pF	ns
Output Disable Time			t_{OH6}	0		50		ns
Rise Time, Fall Time		A0, $\overline{CS}$, R/W, E, D0 to D7 Terminals	t_r,t_f			15		ns

Note 16) All timing are based on 20% and 80% of V_{DD} voltage level.

Note 17) t_{CYC6} shows the cycle of the E signal in active $\overline{CS}$.

- Write operation sequence (Serial Interface)

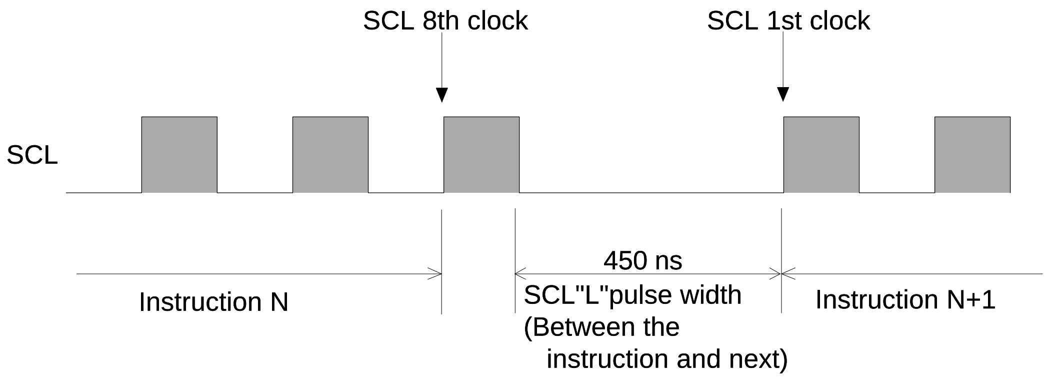


(VDD=2.4V to 3.6V,Ta=-30 to +80°C)

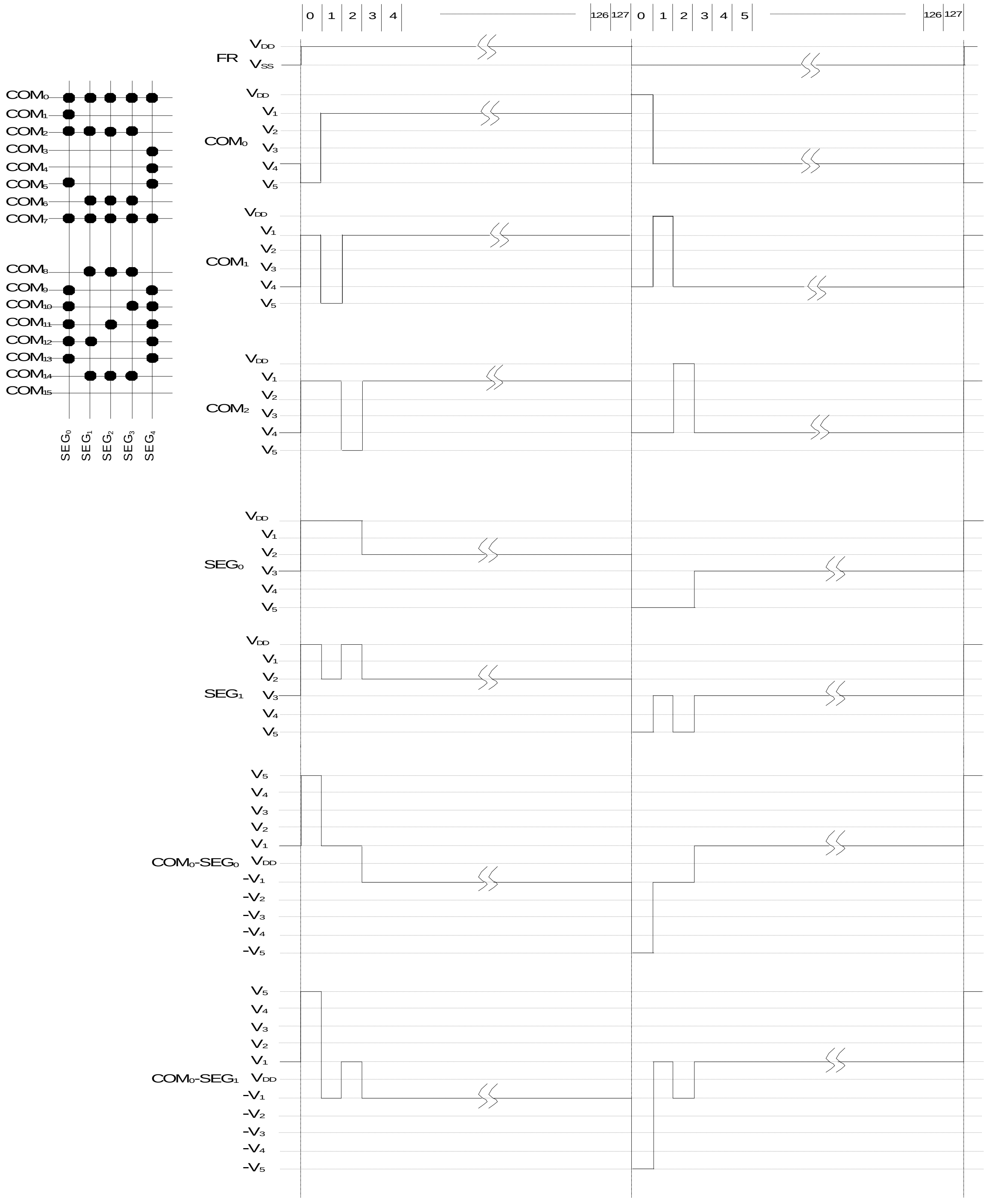
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	60				ns
SCL "H" pulse width		t_{SHW}	30				ns
SCL "L" pulse width		t_{SLW}	30				ns
Address Set Up Time	A0 Terminal	t_{SAS}	25				ns
Address Hold Time		t_{SAH}	150				ns
Data Set Up Time	SI Terminal	t_{SDS}	25				ns
Data Hold Time		t_{SDH}	10				ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	t_{CSS}	10				ns
		t_{CSH}	300				ns
Rise Time, Fall Time	SCL, A0, $\overline{CS}$, SI Terminals	t_r,t_f			15		ns

Note 18) All timing are based on 20% and 80% of VDD voltage level.

Note 19) When inputting an instruction continuously, keep 450nS as the cycle of SCL between the instructions as follows



■ LCD DRIVING WAVEFORM



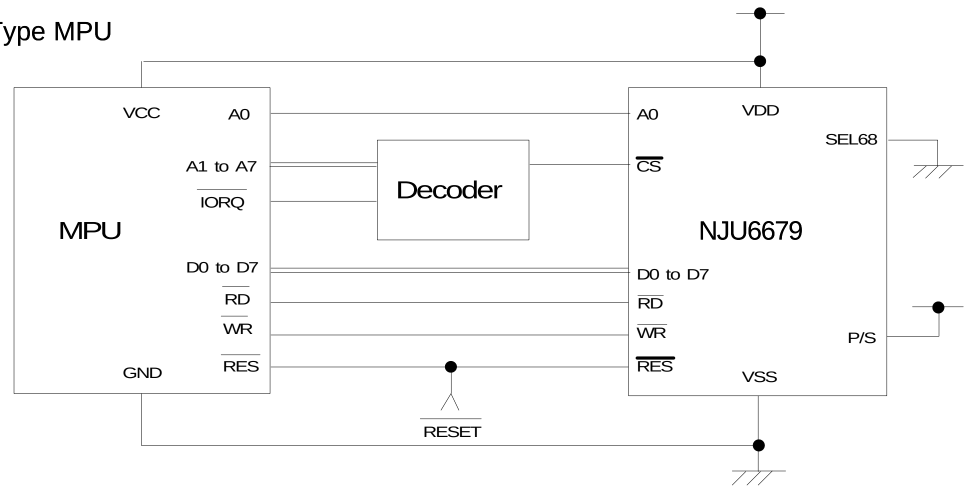
■ APPLICATION CIRCUIT

MPU Interface (examples)

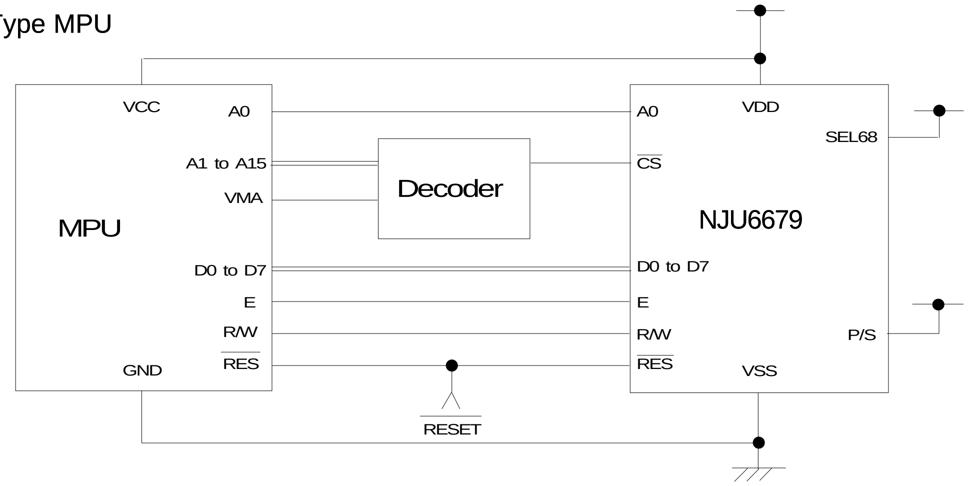
The **NJU6679** is connectable to 80-type MPU or 68-type. In use of Serial Interface, it is possible to be controlled by the signal line with the more small being.

*:SEL68 terminal shall be connected to V_{DD} or V_{SS}.

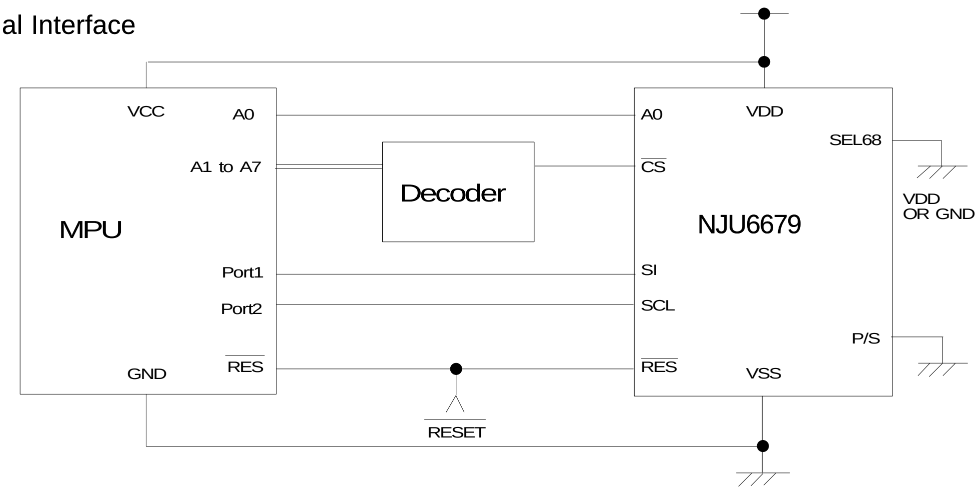
- 80 Type MPU



- 68 Type MPU



- Serial Interface



■ LCD Panel Interface Example