

# Octal bus transceiver, non-inverting (open collector)

74F621

## FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Octal bidirectional bus interface
- Open collector outputs sink 64mA
- Non-inverting

## DESCRIPTION

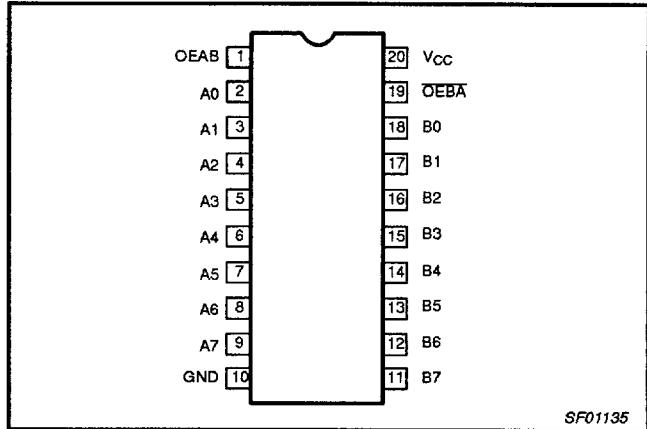
The 74F621 is an octal transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OEBA and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 74F621 the capability to store data by the simultaneous enabling of OEBA and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F621N	SOT146-1
20-pin plastic SOL <sup>1</sup>	N74F621D	SOT163-1

### NOTE:

1. Thermal mounting techniques are recommended. See *SMD Process Applications* for a discussion of thermal considerations for surface mounted device.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

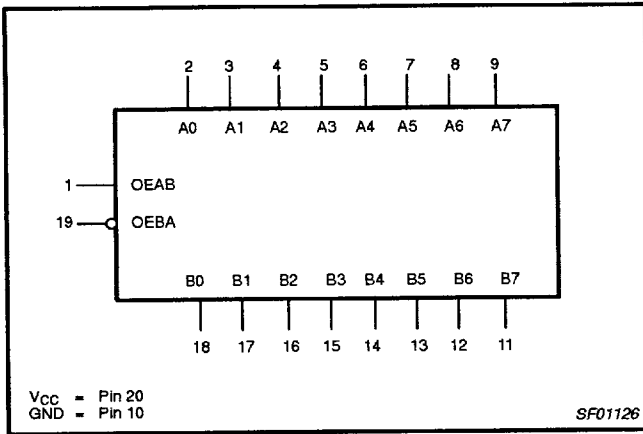
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	1.0/0.033	20µA/20µA
OEBA, OEAB	Output Enable inputs	1.0/0.033	20µA/20µA
A0 - A7	Data outputs	OC/40	OC/24mA
B0 - B7	Data outputs	OC/106.7	OC/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

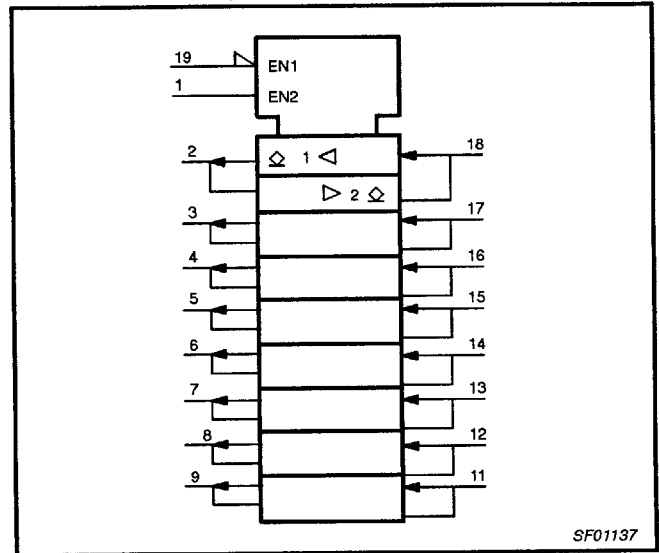
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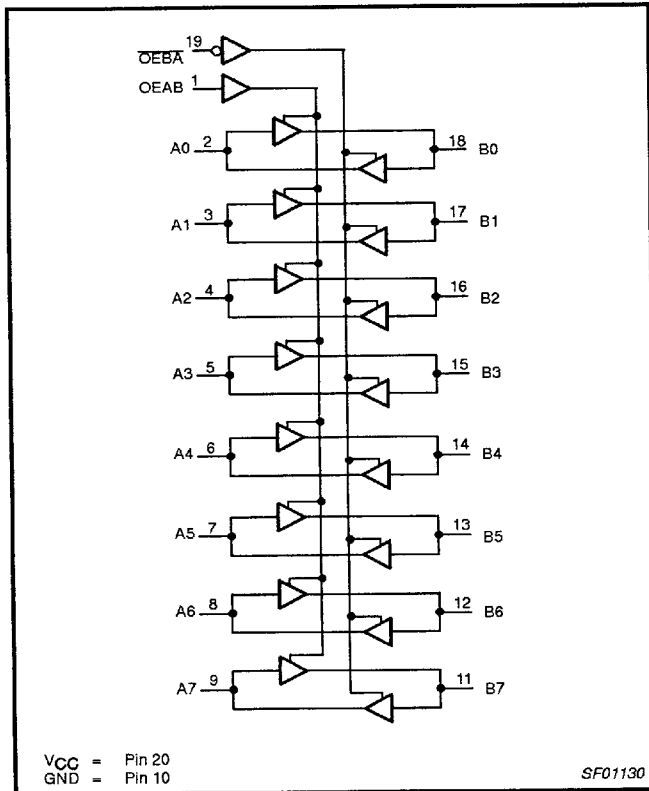
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES
OEBA	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	OFF
L	H	B data to A bus
		A data to B bus

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 OFF= High if pull-up resistor is connected to open collector output

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +7.0	V
$V_{IN}$	Input voltage		-0.5 to +7.0	V
$I_{IN}$	Input current		-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to +5.5	V
$I_{OUT}$	Current applied to output in Low output state	A0-A7	48	mA
		B0-B7	128	mA
$T_{amb}$	Operating free-air temperature range		0 to +70	°C
$T_{stg}$	Storage temperature range		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$V_{OH}$	High-level output current			4.5	V
$I_{OL}$	Low-level output current	A0-A7		24	mA
		B0-B7		64	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
$I_{OH}$	High-level output current	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = \text{MAX}$			250	$\mu\text{A}$	
$V_{OL}$	Low-level output voltage	A0-A7	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = 24\text{mA}$	$\pm 10\% V_{CC}$	0.35	0.50	V
				$\pm 5\% V_{CC}$	0.35	0.50	V
		B0-B7	$I_{OL} = 48\text{mA}$	$\pm 10\% V_{CC}$	0.38	0.55	V
			$I_{OL} = 64\text{mA}$	$\pm 5\% V_{CC}$	0.42	0.55	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	OEBA, OEAB	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	$\mu\text{A}$
		others	$V_{CC} = 0.0\text{V}, V_I = 5.5\text{V}$			1	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-20	$\mu\text{A}$	
$I_{CC}$	Supply current (total)	$I_{CCH}$	$V_{CC} = \text{MAX}$	OEBA = OEAB = A0-A7 = 4.5V	105	140	mA
		$I_{CCL}$			OEBA = OEAB = 4.5V, A0-A7 = GND	105	140

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$ .

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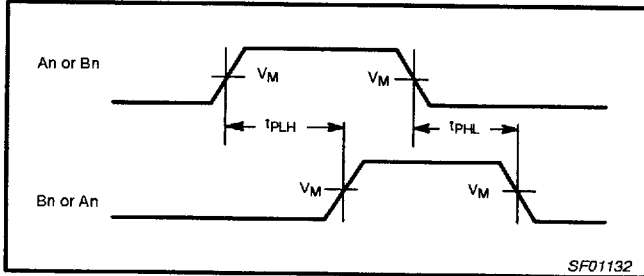
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AC ELECTRICAL CHARACTERISTICS

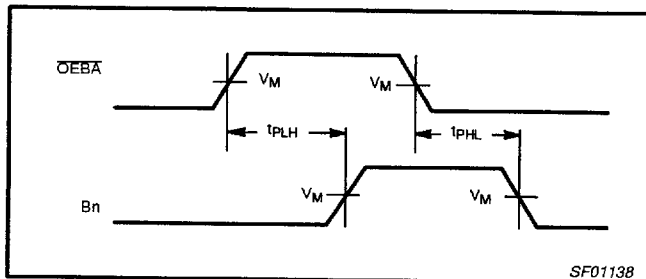
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Bn	Waveform 1	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Bn to An	Waveform 1	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay OEBA to An	Waveform 2	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay OEAB to Bn	Waveform 3	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

AC WAVEFORMS

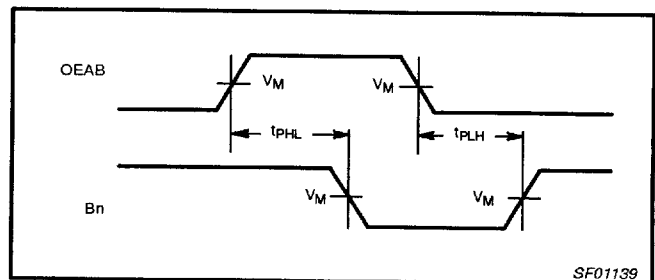
For all waveforms, V<sub>M</sub> = 1.5V.



Waveform 1. For Non-Inverting Outputs



Waveform 2. Propagation Delay, OEBA to An

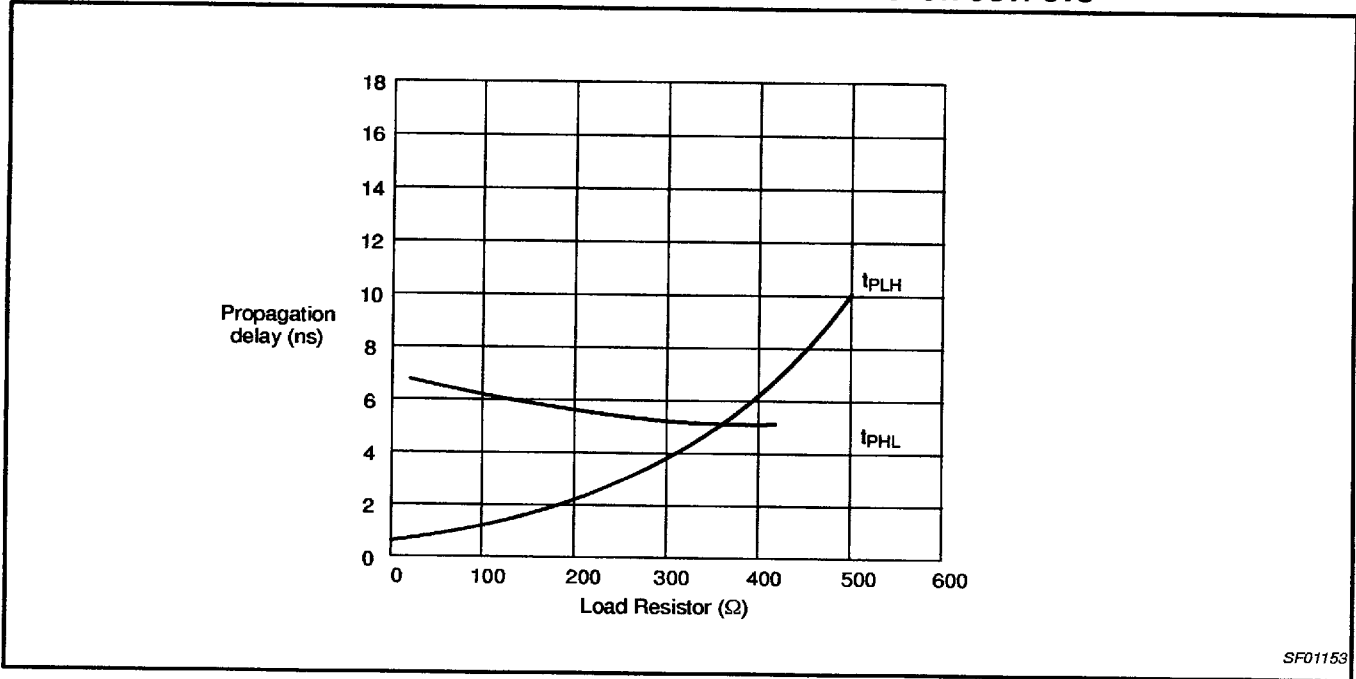


Waveform 3. Propagation Delay, OEAB to Bn

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## TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



SF01153

**NOTE:**

When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t<sub>PLH</sub>. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t<sub>PLH</sub> up to 50% with only slight increase in the t<sub>PHL</sub>. However, if the pull-up resistor is changed, the user must take certain that the total I<sub>OL</sub> current through the resistor and the total I<sub>IL</sub>'s of the receivers do not exceed the I<sub>OL</sub> maximum specification.

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Open Collector Outputs**

**DEFINITIONS:**  
 R<sub>L</sub> = Load resistor; see AC electrical characteristics for value.  
 C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027