DPS4X16

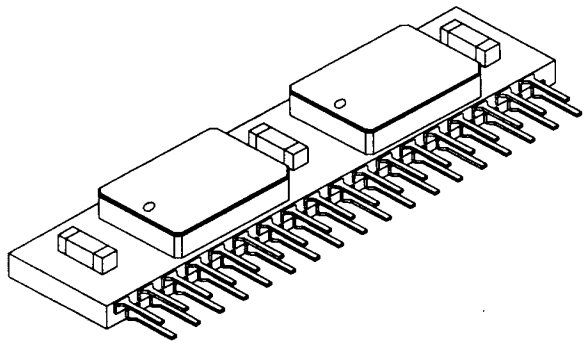
4K X 16 CMOS SRAM MODULE

NOT RECOMENDED FOR NEW DESIGNS

DESCRIPTION:

The DPS4X16 is a 4K X 16 SRAM module built with fout 4K X 8 CMOS SRAMs in ceramic LCC packages suface mounted on a 28-pin, 0.600" wide Co-Fired DIP substrate. The memory utilizes asyncronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS4X16 is ideal for use in microprocessor systems and applications where high speed and/or board space is a prime concern.



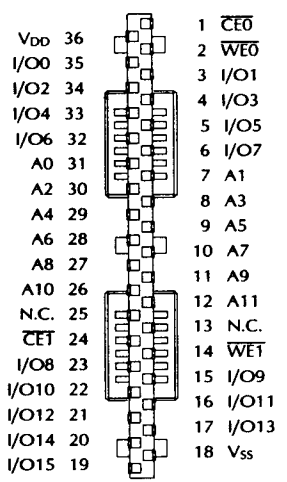
FEATURES:

- 4K X 16 Organization
- Access Times: 25, 35, 45, 55ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- TTL-compatible Inputs and Outputs
- Common Data Inputs and Outputs
- Single +5V Operation (± 10% Tolerance)
- Available with All Semiconductor Components used in the Construction of the Module Compliant to MIL-STD-883; Class B
- 36-Pin, Ceramic ZIP Package

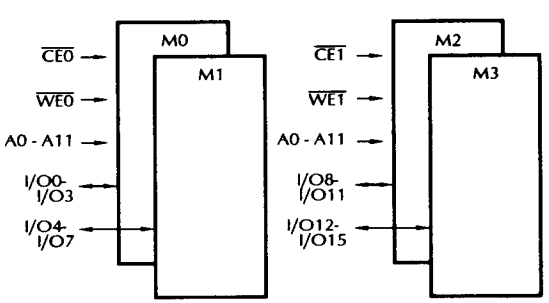
PIN NAMES	
A0 - A11	Address Inputs
I/O0 - I/O15	Data Inputs/Outputs
$\overline{CE0}$ / $\overline{CE1}$	Chip Enables
$\overline{WE0}$ / $\overline{WE1}$	Write EnableS
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

(BOTTOM VIEW)



FUNCTIONAL BLOCK DIAGRAM



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RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Temperature Range	0		+70	°C

ABSOLUTE MAXIMUM RATINGS[3]		
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

TRUTH TABLE				
Mode	$\overline{CE}$	$\overline{WE}$	I/O	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	25	pF	V_{IN} = 0V
C_{CE}	Chip Enable	45		
C_{WE}	Write Enable	25		
$C_{I/O}$	Data Input/Output	20		

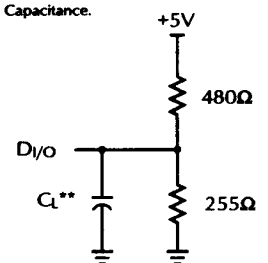
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	30 pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



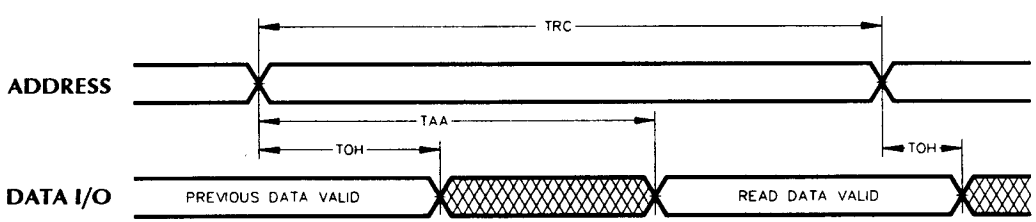
DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-20	+20	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	-20	+20	-20	+20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		305		360		410	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		445		475		590	mA
I_{SB1}	Full Standby Supply Current (CMOS)	V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} -0.2V, $\overline{CE}$ ≥ V_{DD} -0.2V		7.5		10.0		15.0	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}		45		50		55	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	2.4		2.4		2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges										
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		ns
2	t_{AA}	Address Access Time		25		35		45		55	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55	ns
4	t_{OH}	Output Hold from Address Change	5		5		5		5		ns
5	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns
6	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]	0	15	0	20	0	20	0	25	ns
7	t_{AS}	Address Set-up Time *	0		0		0		0		ns
8	t_{OC}	Output Hols from Chip Enable	0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges										
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
9	t_{WC}	Write Cycle Time	25		35		45		55		ns
10	t_{AW}	Address Valid to End of Write	20		30		40		50		ns
11	t_{CW}	Chip Enable to End of Write	20		30		40		50		ns
12	t_{DW}	Data Valid to End of Write	10		15		20		25		ns
13	t_{DH}	Data Hold Time	3		3		3		3		ns
14	t_{WP}	Write Pulse Width	20		30		40		50		ns
15	t_{AH}	Address Hold Time	2		5		5		5		ns
16	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]	0	15	0	15	0	20	0	25	ns
17	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns

* Valid for both Read and Write cycles.

READ CYCLE 1: Address Controlled. $\overline{CE}$ is LOW. $\overline{WE}$ is HIGH.



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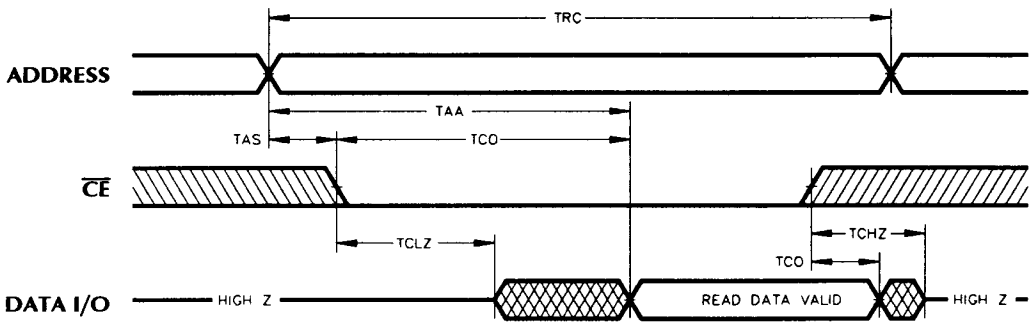
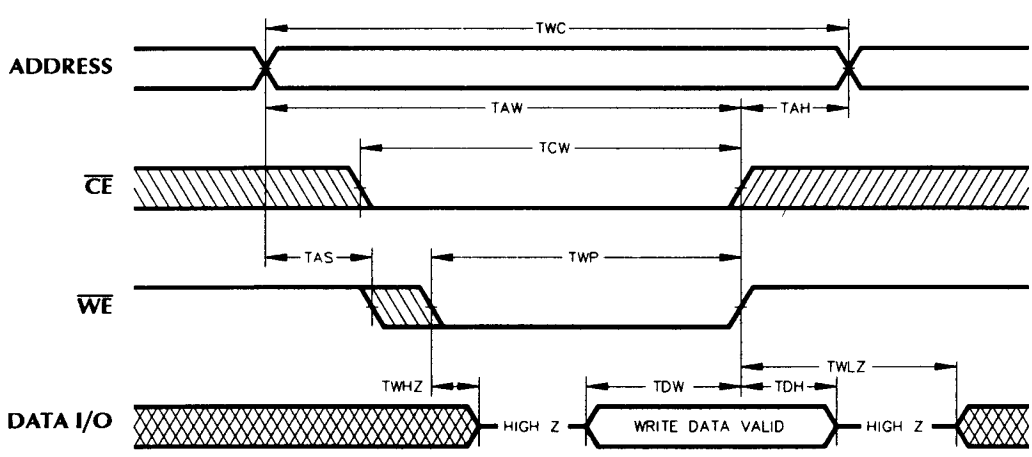
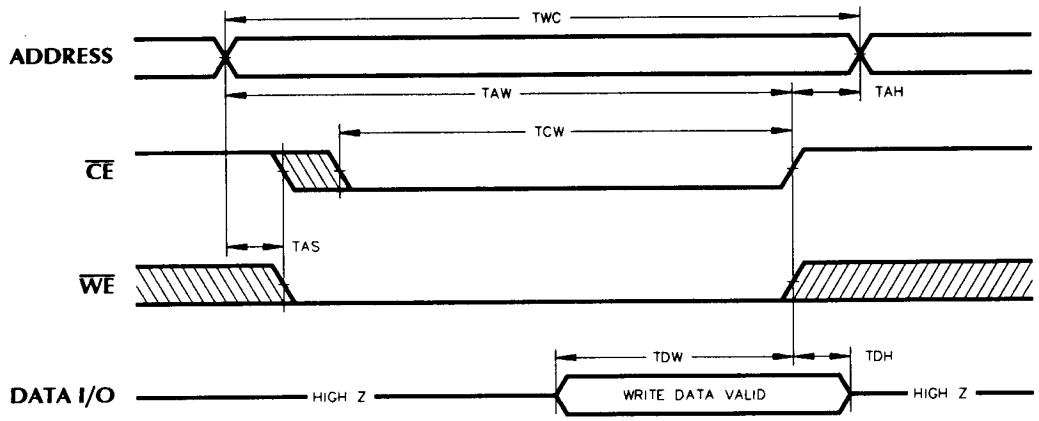
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled.



WRITE CYCLE 2: $\overline{CE}$ Controlled.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

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WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

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ORDERING INFORMATION

DP S4X16 – XX X

PREFIX | DEVICE TYPE | SPEED | GRADE

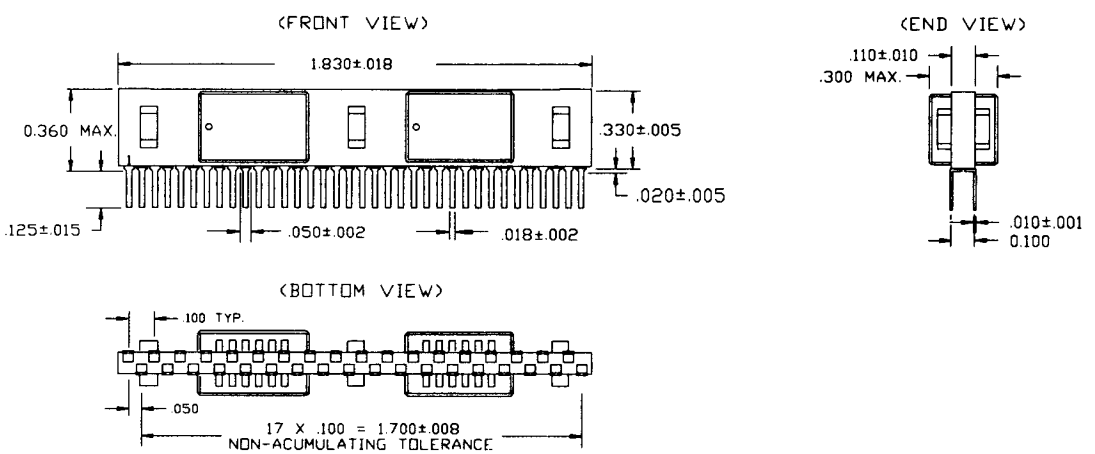
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B*	MIL−PROCESSED	−55°C to +125°C

25	25ns
35	35ns
45	45ns
55	55ns

4KX16 CMOS SRAM 36−PIN CERAMIC ZIP

* B grade modules built with 883 devices.

MECHANICAL DRAWING



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