CS43L41

Low Power 24-Bit, 96 kHz DAC with Volume Control

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- ATAPI Mixing
- 101 dB Dynamic Range
- 89 dBFS THD+N
- Low Clock Jitter Sensitivity
- +2.4 V to +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis for 32, 44.1, and 48 kHz
- Digital Volume Control with Soft Ramp
  - 94 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- 24 mW with 2.4 V supply

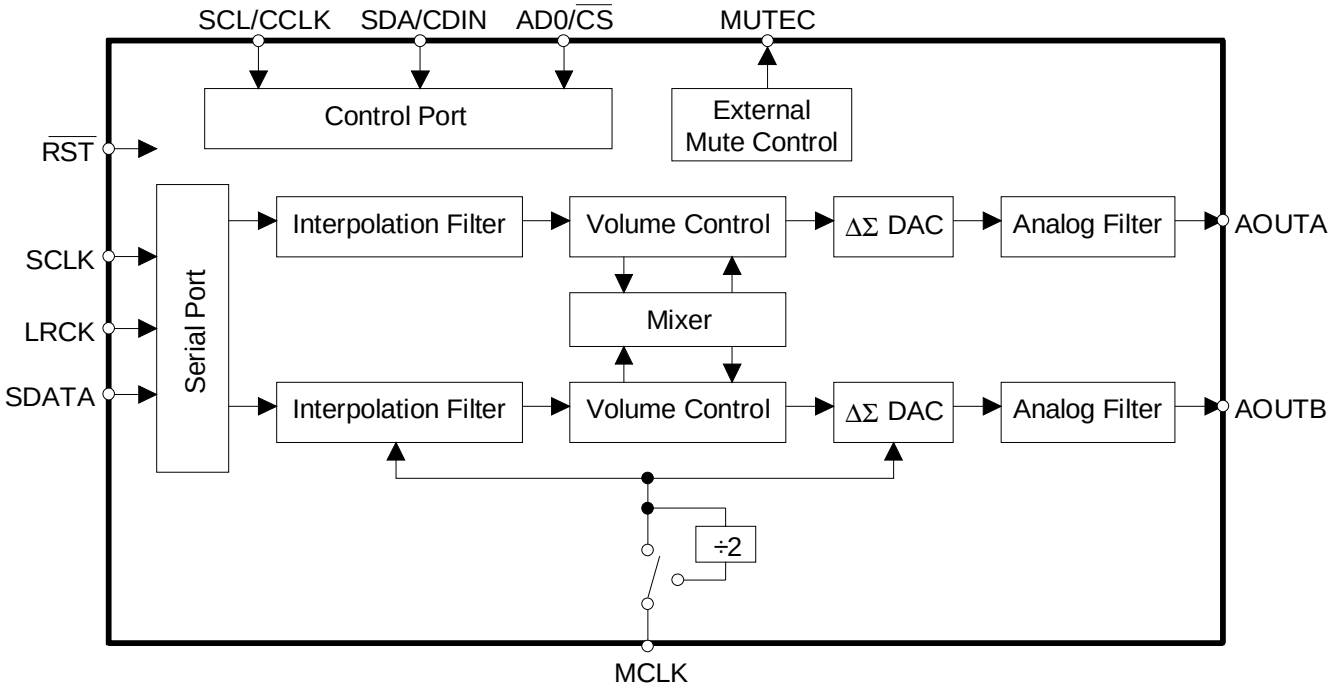
Description

The CS43L41 is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS43L41 accepts data at audio sample rates from 2 kHz to 100 kHz, consumes very little power and operates over a wide power supply range. These features are ideal for portable DVD, portable MP3, Mini-Disc, and mobile phones.

ORDERING INFORMATION

CS43L41-KZ 16-pin TSSOP, -10 to 70 °C



Advanced Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; Logic "1" = VA; Logic "0" = AGND;

Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 40 kHz, unless otherwise specified. Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 17)),

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Dynamic Performance for VA = 5 V								
Specified Temperature Range	T_A	-10	-	70	-10	-	70	°C
Dynamic Range (Note 1)								
18 to 24-Bit								
unweighted		92	97	-	91	96	-	dB
A-Weighted		96	101	-	95	100	-	dB
16-Bit unweighted		-	95	-	-	94	-	dB
A-Weighted		-	99	-	-	98	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit 0 dB		-	-89	-84	-	-89	-84	dB
-20 dB		-	-77	-72	-	-74	-69	dB
-60 dB		-	-37	-32	-	-36	-31	dB
16-Bit 0 dB		-	-88	-	-	-89	-	dB
-20 dB		-	-75	-	-	-73	-	dB
-60 dB		-	-35	-	-	-34	-	dB
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Dynamic Performance for VA = 2.4 V								
Specified Temperature Range	T_A	-10	-	70	-10	-	70	°C
Dynamic Range (Note 1)								
18 to 24-Bit								
unweighted		TBD	92	-	TBD	91	-	dB
A-Weighted		TBD	95	-	TBD	95	-	dB
16-Bit unweighted		-	91	-	-	90	-	dB
A-Weighted		-	94	-	-	94	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit 0 dB		-	-91	TBD	-	-89	TBD	dB
-20 dB		-	-72	TBD	-	-71	TBD	dB
-60 dB		-	-32	TBD	-	-31	TBD	dB
16-Bit 0 dB		-	-90	-	-	-88	-	dB
-20 dB		-	-71	-	-	-70	-	dB
-60 dB		-	-31	-	-	-30	-	dB
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB

Notes: 1. One-half LSB of triangular PDF dither is added to data.

ANALOG CHARACTERISTICS (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Analog Output					
Full Scale Output Voltage		0.63•VA	0.7•VA	0.77•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
AC-Load Resistance (Note 2)	R_L	3	-	-	kΩ
Load Capacitance (Note 2)	C_L	-	-	100	pF

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Combined Digital and On-chip Analog Filter Response (Note 3)								
Passband (Note 4)								
to -0.05 dB corner		0	-	.4535	-	-	-	Fs
to -0.1 dB corner		-	-	-	0	-	.4621	Fs
to -3 dB corner		0	-	.4998	0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz		-.02	-	+.08	-0.06	-	0	dB
StopBand		.5465	-	-	.577	-	-	Fs
StopBand Attenuation (Note 5)		50	-	-	55	-	-	dB
Group Delay	tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation 0 - 40 kHz		-	-	-	-	±1.39/Fs	-	s
0 - 20 kHz		-	±0.36/Fs	-	-	±0.23/Fs	-	s
De-emphasis Error Fs = 32 kHz		-	-	+.2/-.1				dB
(Relative to 1 kHz) Fs = 44.1 kHz		-	-	+.05/-.14		(Note 6)		dB
Fs = 48 kHz		-	-	+0/-.22				dB

Notes:
2. Refer to Figure 18.
3. Filter response is guaranteed by design.
4. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 9-16) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
5. For Base-Rate Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For High-Rate Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
6. De-emphasis is not available in High-Rate Mode.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current VA = 5 V	normal operation power-down state	I_A I_A	- -	15 60	17 -	mA µA
Power Dissipation VA = 5 V	(Note 7) normal operation power-down		 - -	 75 0.3	 85 -	 mW mW
Power Supply Current VA = 2.4 V	normal operation power-down state	I_A I_A	- -	10 30	TBD -	mA µA
Power Dissipation VA = 2.4 V	(Note 7) normal operation power-down		 - -	 24 0.07	 TBD -	 mW mW
Package Thermal Resistance		θ_{JA}	-	110	-	°C/Watt
Power Supply Rejection Ratio (1 kHz)	(Note 8) (60 Hz)	PSRR	- -	60 40	- -	dB dB

Notes: 7. Refer to Figure 19.

8. Valid with the recommended capacitor values on FILT+ and V_Q as shown in Figure 1.

DIGITAL CHARACTERISTICS (T_A = 25°C; VA = 2.28V - 5.5V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VA = 5 V VA = 2.4 V	V_{IH}	2.0 2.0	- -	- -	V V
Low-Level Input Voltage	VA = 5 V VA = 2.4 V	V_{IL}	- -	- -	0.8 0.8	V V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VA	2.28	5.0	5.5	V

SWITCHING CHARACTERISTICS (T_A = -10 to 70°C; VA = 2.4V - 5.5V; Inputs: Logic 0 = 0V, Logic 1 = VA, C_L = 20pF)

Parameters	Symbol	Min	Typ	Max	Units
Input Sample Rate	Fs	2	-	100	kHz
MCLK Pulse Width High MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width Low MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 256 or 128		31	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 256 or 128		31	-	1000	ns
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		40	50	60	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Period MCLK / LRCK = 512, 256 or 384	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period MCLK / LRCK = 128 or 192	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 9)		-	50	-	%
SCLK Period (Note 10)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 9. In Internal SCLK Mode, the Duty Cycle must be 50% ±1/2 MCLK Period.

10. The SCLK / LRCK ratio may be either 32, 48, or 64. This ratio depends on part type and MCLK/LRCK ratio. (See Figures 20-26)

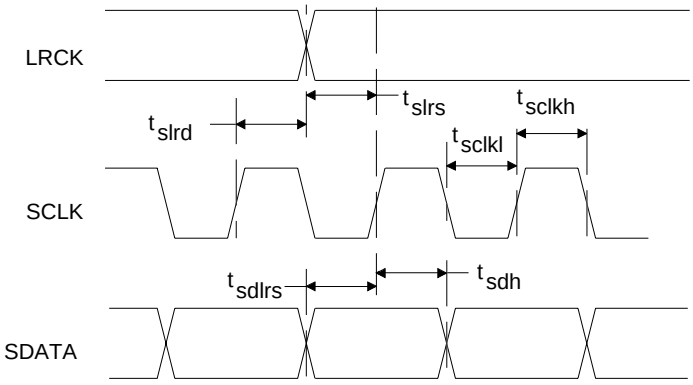


Figure 1. External Serial Mode Input Timing

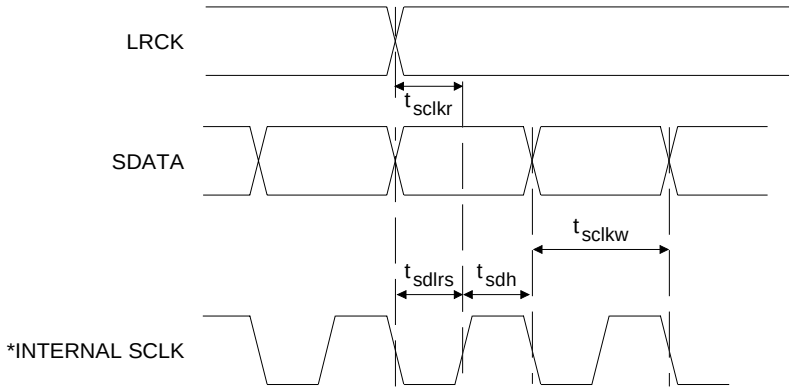


Figure 2. Internal Serial Mode Input Timing
*The SCLK pulses shown are internal to the CS43L41.

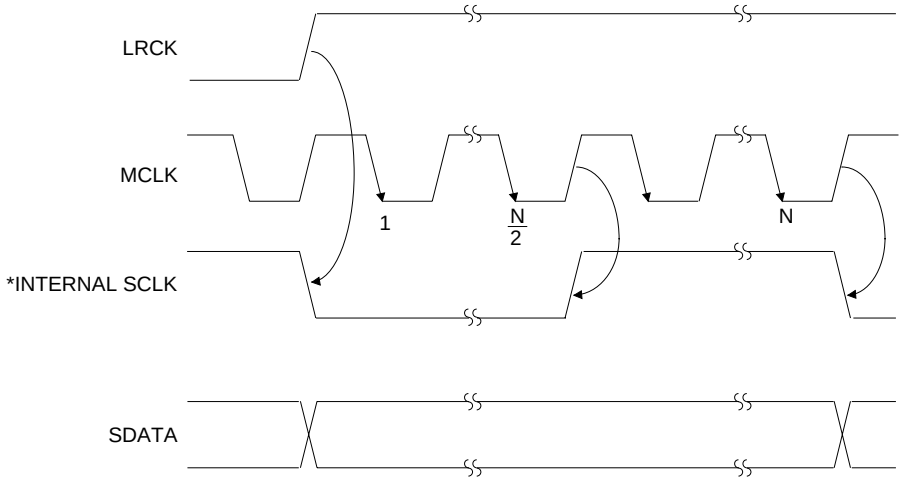


Figure 3. Internal Serial Clock Generation
* The SCLK pulses shown are internal to the CS43L41.
N equals MCLK divided by SCLK

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25 °C; VA = +5 V ±5%; Inputs: logic 0 = AGND, logic 1 = VA, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
I²C® Compatible Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 11)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

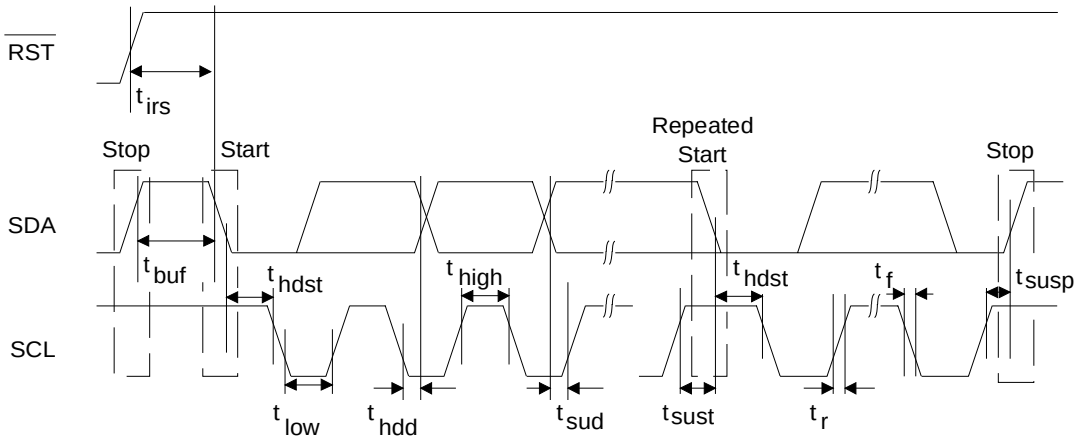


Figure 4. I²C Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25 °C; VA = +5 V ±5%; Inputs: logic 0 = AGND, logic 1 = VA, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI® Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 12)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 13)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 14)	t_{f2}	-	100	ns

Notes: 12. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

13. Data must be held for sufficient time to bridge the transition time of CCLK.

14. For F_{SCK} < 1 MHz

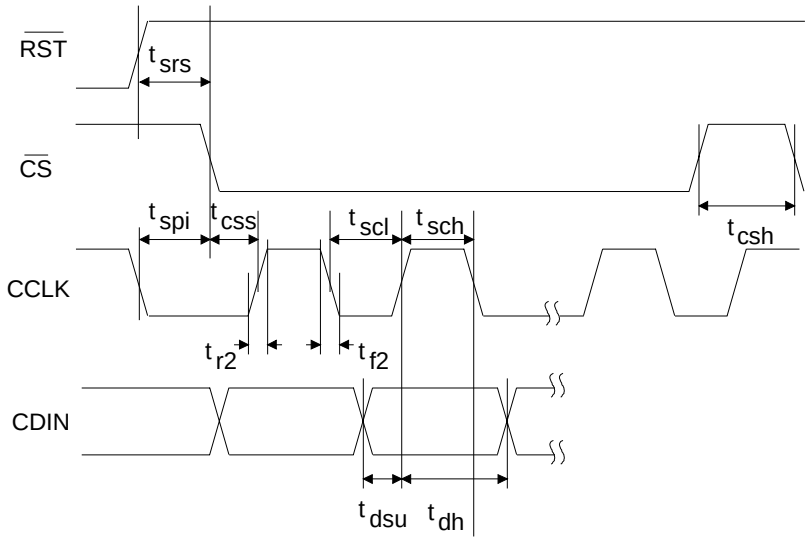


Figure 5. SPI Control Port Timing

2. TYPICAL CONNECTION DIAGRAM

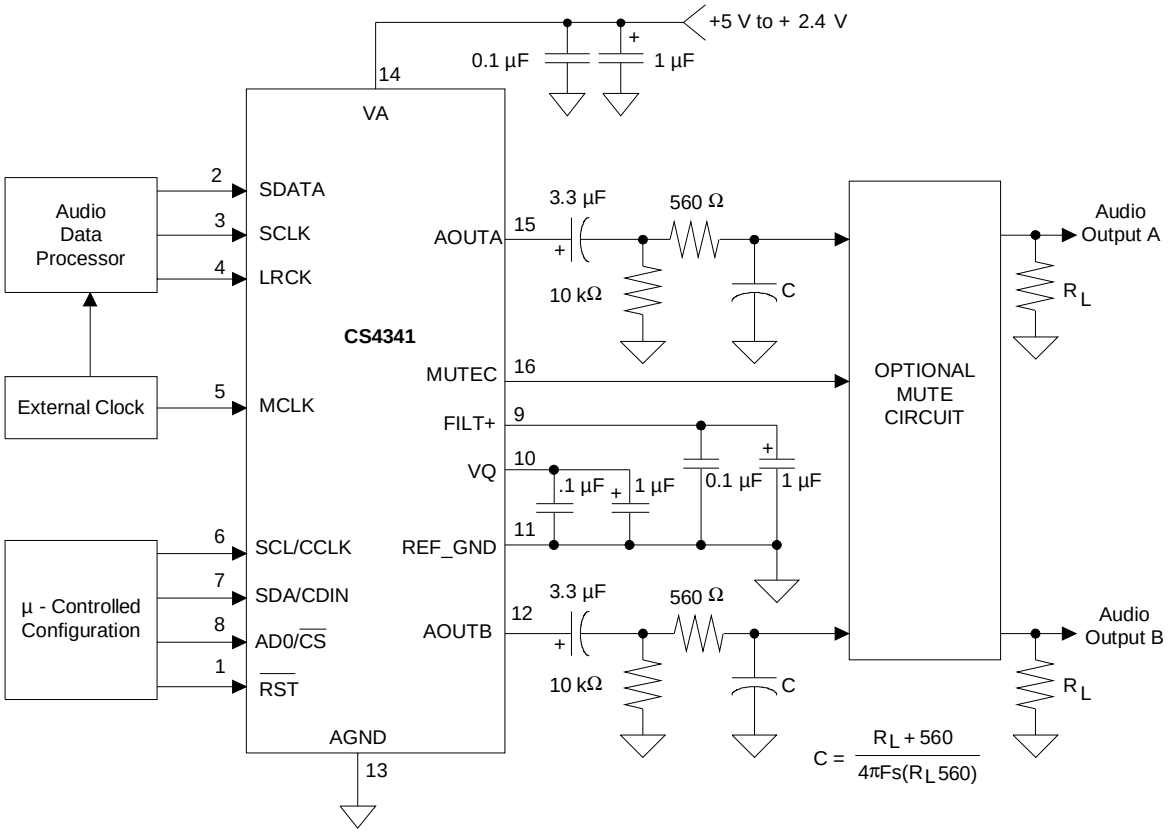


Figure 6. Typical Connection Diagram

3. REGISTER QUICK REFERENCE

** “default” ==> bit status after power-up-sequence or reset.

3.1 MCLK Control (address 00h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLKDIV	Reserved
0	0	0	0	0	0	0	0

MCLKDIV (MCLK Divide-by-2 Enable)

Default = ‘0’.
0 - Disabled
1 - Enabled

3.2 Mode Control (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN
1	0	0	0	0	0	1	1

AMUTE (Auto-mute)

Default = ‘1’.
0 - Disabled
1 - Enabled

DIF2, DIF1 and DIF0 (Digital Interface Format)

Default = ‘0’.
0 - Format 0, I^2S, up to 24-bit data, 64 x Fs Internal SCLK
1 - Format 1, I^2S, up to 24-bit data, 32 x Fs Internal SCLK
2 - Format 2, Left Justified, up to 24-bit data
3 - Format 3, Right Justified, 24-bit Data
4 - Format 4, Right Justified, 20-bit Data
5 - Format 5, Right Justified, 16-bit Data
6 - Format 6, Right Justified, 18-bit Data
7 - Identical to Format 1

DEM 1, DEM 0 (De-Emphasis Mode)

Default = ‘0’.
0 - Disabled
1 - 44.1 kHz De-Emphasis
2 - 48 kHz De-Emphasis
3 - 32 kHz De-Emphasis

POR (Power on/off Quiescent Voltage ramp)

Default = ‘1’.
0 - Disabled
1 - Enabled

PDN (Power-Down)

Default =’1’.
0 - Disabled
1 - Enabled

3.3 Volume and Mixing Control (address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	1	0	0	1	0	0	1

A = B (Channel A Volume = Channel B Volume)

Default = '0'.

0 - AOUTA volume is determined by register 03h and AOUTB volume is determined by register 04h.

1 - AOUTA and AOUTB volumes are determined by register 03h and register 04h is ignored.

Soft & Zero Cross (Soft control and zero cross detection control)

Default = '10'.

Soft	Zero Cross	Mode
0	0	Changes take effect immediately
0	1	Changes take effect on zero crossings
1	0	Changes take effect with a soft ramp (default)
1	1	Changes take effect in 1/8 dB steps on each zero crossing

ATAPI 0-4 (Channel mixing and muting)

(refer to Table 9)
Default = '01001', (Stereo)
AOUTA = Left Channel
AOUTB = Right Channel

3.4 Channel A Volume Control (address 03h)

3.5 Channel B Volume Control (address 04h)

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

MUTE

Default = '0'
0 - Disabled
1 - Enabled

Volume

Default = '0'
(Refer to Table 11)

4. REGISTER BIT DESCRIPTION

4.1 MASTER CLOCK DIVIDE ENABLE

MCLK Control Register (address 00h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCLKDIV	Reserved

Access:

R/W in I^2C and write only in SPI.

Default:

0 - Disabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2.
Note: This feature is present on revision C and newer devices. For backward compatibility with previous revision devices, this bit defaults to zero.

MCLKDIV	MODE
0	Disabled
1	Enabled

Table 1. Master Clock Divide Enable

4.2 AUTO-MUTE

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN

Access:

R/W in I^2C and write only in SPI.

Default:

1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-zero data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is effected, similar to volume control changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

AMUTE	MODE
0	Disabled
1	Enabled

Table 2. Auto-Mute Enable

4.3 DIGITAL INTERFACE FORMAT

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN

Access:

R/W in I^2C and write only in SPI.

Default:

0 - Format 0 (I^2S, up to 24-bit data, 64 x Fs Internal SCLK)

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 20-26.

DIF2	DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	0	I^2S, up to 24-bit data, 64 x Fs Internal SCLK	0	20
0	0	1	I^2S, up to 24-bit data, 32 x Fs Internal SCLK	1	21
0	1	0	Left Justified, up to 24-bit data	2	22
0	1	1	Right Justified, 24-bit Data	3	23
1	0	0	Right Justified, 20-bit Data	4	24
1	0	1	Right Justified, 16-bit Data	5	25
1	1	0	Right Justified, 18-bit Data	6	26
1	1	1	Identical to Format 1	7	20

Table 3. Digital Interface Formats

4.4 DE-EMPHASIS CONTROL

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN

Access:

R/W in I^2C and write only in SPI.

Default:

0 - Disabled

Function:

Implementation of the standard 15µs/50µs digital de-emphasis filter response, Figure 27, requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. NOTE: De-emphasis is not available in High-Rate Mode.

DEM1	DEMO	DESCRIPTION
0	0	Disabled
0	1	44.1kHz
1	0	48kHz
1	1	32kHz

Table 4. De-emphasis Filter Configurations

4.5 POWER ON/OFF QUIESCENT VOLTAGE RAMP

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN

Access:

R/W in I^2C and write only in SPI.

Default:

1 - Enabled

Function:

The power On/Off Quiescent Voltage Ramp allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-off. Please refer to the applications section for details of implementing this feature.

POR	MODE
0	Disabled
1	Enabled

Table 5. Power On/Off Ramp Enable

4.6 POWER DOWN

Mode Control Register (address 01h)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	POR	PDN

Access:

R/W in I^2C and write only in SPI.

Default:

1 - Enabled

Function:

The device will enter a low-power state whenever this function is activated. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained in this mode.

PDN	MODE
0	Disabled
1	Enabled

Table 6. Power Down Enable

4.7 CHANNEL A VOLUME = CHANNEL B VOLUME

Volume and Mixing Control Register (address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0

Access:

R/W in I^2C and write only in SPI.

Default:

0 - Disabled

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

A = B	MODE
0	Disabled
1	Enabled

Table 7. A=B Volume Control Enable

4.8 SOFT RAMP OR ZERO CROSS ENABLE

Volume and Mixing Control Register (address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0

Access:

R/W in I^2C and write only in SPI.

Default:

10 - Soft Ramp enabled.

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

SOFT	ZERO	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled

Table 8. Soft Ramp and Zero Cross Enable

4.9 ATAPI CHANNEL MIXING AND MUTING

Volume and Mixing Control Register (address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0

Access:

R/W in I^2C and write only in SPI.

Default:

01001 - AOUTA=aL, AOUTB=bR (Stereo)

Function:

The CS43L41 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 9 and Figure 28 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR

Table 9. ATAPI Decode

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 9. ATAPI Decode (Continued)

4.10 MUTE

Channel A Volume Control Register (address 03h)

Channel B Volume Control Register (address 04h)

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Access:

R/W in I^2C and write only in SPI.

Default:

0 - Disabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The MUTEC will go active during the mute period if the Mute function is enabled for both channels.

MUTE	MODE
0	Disabled
1	Enabled

Table 10. Mute Enable

4.11 VOLUME CONTROL

Channel A Volume Control Register (address 03h)

Channel B Volume Control Register (address 04h)

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Access:

R/W in I^2C and write only in SPI.

Default:

0 - 0 dB (No attenuation)

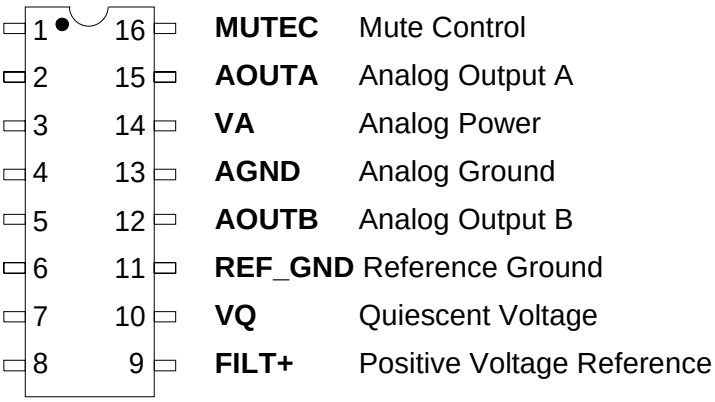
Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -90 dB. Volume settings are decoded as shown in Table 11. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Volume and Mixing Control register. All volume settings less than - 94 dB are equivalent to enabling the Mute bit.

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 11. Digital Volume Settings

5. PIN DESCRIPTION



Analog Power - VA

Pin 14, Input

Function:

Analog power supply. Typically 2.4 to 5VDC.

Analog Ground - AGND

Pin 13, Input

Function:

Analog ground reference.

Analog Output - AOUTA and AOUTB

Pins 12 and 15, Output

Function:

The full scale analog output level is specified in the Analog Characteristics specifications table.

Reference Ground - REF_GND

Pin 11, Input

Function:

Ground reference for the internal sampling circuits. Must be connected to analog ground.

Positive Voltage Reference - FILT+

Pin 9, Output

Function:

Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 6. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.

Quiescent Voltage - VQ

Pin 10, Output

Function:

Filter connection for internal quiescent reference voltage, typically 50% of VA. Capacitors must be connected from V_Q to analog ground, as shown in Figure 6. V_Q is not intended to supply external current. V_Q has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.

Master Clock - MCLK

Pin 5, Input

Function:

The master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Base Rate Mode (BRM) and 128x, 192x, 256x or 384x the input sample rate in High Rate Mode (HRM). Note that some multiplication factors require setting the MCLKDIV bit in the MCLK Control Register. Table 12 illustrates several standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)								
	HRM				BRM				
	128x	192x	256x*	384x*	256x	384x	512x	768x*	1024x*
32	4.0960	6.1440	8.1920	12.2880	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	5.6448	8.4672	11.2896	16.9344	11.2896	16.9344	22.5792	32.7680	45.1584
48	6.1440	9.2160	12.2880	18.4320	12.2880	18.4320	24.5760	36.8640	49.1520
64	8.1920	12.2880	16.3840	24.5760	-	-	-	-	-
88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	-	-
96	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-

* Requires MCLKDIV bit = 1 in MCLK Control Register (address 00h)

Table 12. Common Clock Frequencies

Left/Right Clock - LRCK

Pin 4, Input

Function:

The Left/Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-26.

Serial Audio Data - SDATA

Pin 2, Input

Function:

Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-26.

Serial Clock - SCLK

Pin 3, Input

Function:

Clocks the individual bits of the serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Mode Control Byte and the options are detailed in Figures 20-26.

The CS43L41 supports both internal and external serial clock generation modes. The Internal Serial Clock Mode eliminates possible clock interference from an external SCLK. Use of the Internal Serial Clock Mode is always preferred.

Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with the master clock and left/right clock. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending upon data format, as shown in Figures 20-26. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK.

External Serial Clock Mode

The CS43L41 will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK.

Reset - $\overline{\text{RST}}$

Pin 1, Input

Function:

The device enters a low power mode and all internal registers are reset to the default settings, including the control port, when low. When high, the control port becomes operational and the PDN bit must be cleared before normal operation will occur. The control port can not be accessed when reset is low.

Serial Control Interface Clock - SCL/CCLK

Pin 6, Input

Function:

Clocks the serial control data into or from SDA/CDIN.

Serial Control Data I/O - SDA/CDIN

Pin 7, Input/Output

Function:

In I^2C mode, SDA is a data I/O line. CDIN is the input data line for the control port interface in SPI mode.

Address Bit / Chip Select - AD0/$\overline{\text{CS}}$

Pin 8, Input

Function:

In I^2C mode, AD0 is a chip address bit. $\overline{\text{CS}}$ is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain until either the part is reset or undergoes a power-down cycle.

Mute Control - MUTEC

Pin 16, Output

Function:

The Mute Control pin goes high during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

6. APPLICATIONS

6.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS43L41 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 6 shows the recommended power arrangement with VA connected to a clean supply. Decoupling capacitors should be located as close to the device package as possible.

6.2 Oversampling Modes

The CS43L41 operates in one of two oversampling modes based on the input sample rate and the state of the MCLKDIV bit in the MCLK Control Register. Base Rate Mode (BRM) supports input sample rates up to 50 kHz while High Rate Mode (HRM) supports input sample rates up to 100 kHz. When the MCLKDIV bit is cleared, the devices operate in BRM when MCLK/LRCK is 256, 384 or 512 and in HRM when MCLK/LRCK is 128 or 192. When the MCLKDIV bit is set, the devices operate in BRM when MCLK/LRCK is 512, 768 or 1024 and in HRM when MCLK/LRCK is 256 or 384.

6.3 Recommended Power-up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and V_Q will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with V_Q low and the control port accessible. The desired register settings can be loaded while keeping the PDN bit set to 1.

3. Set the PDN bit to 0 which will initiate the power-up sequence, which requires approximately 50 µs when the POR bit is set to 0. If the POR bit is set to 1, see Section 6.4 for total power-up timing.

6.4 Use of the Power ON/OFF Quiescent Voltage Ramp

The CS43L41 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technique, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters.

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 left/right clock cycles later, the outputs reach VQ and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient.

To prevent transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning off the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

Use of the Mute Control function is recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute

Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit.

7. CONTROL PORT INTERFACE

The control port is used to load all the internal settings of the CS43L41. The operation of the control port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required. *

The control port has 2 modes: SPI and I^2C compatible, with the CS43L41 operating as a slave device in both modes. If I^2C operation is desired, AD0/$\overline{CS}$ should be tied to VA or AGND. If the CS43L41 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up, SPI mode will be selected. The control port registers are write-only in SPI mode.

7.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS43L41 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 7 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP.

The CS43L41 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

7.2 I^2C Compatible Mode

In I^2C compatible mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 8. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VA or AGND as required. The upper 6 bits of the 7-bit address field must be 001000. To communicate with the CS43L41 the LSB of the chip address field, which is the first byte sent to the CS43L41, should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS43L41 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

For more information on I^2C, please see "The I^2C-Bus Specification: Version 2.0", listed in the References section.

* The MCLK is required for both control port interfaces.

7.3 MEMORY ADDRESS POINTER (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR (Auto MAP Increment Enable)

Default = '0'.

0 - Disabled

1 - Enabled

MAP0-2 (Memory Address Pointer)

Default = '000'.

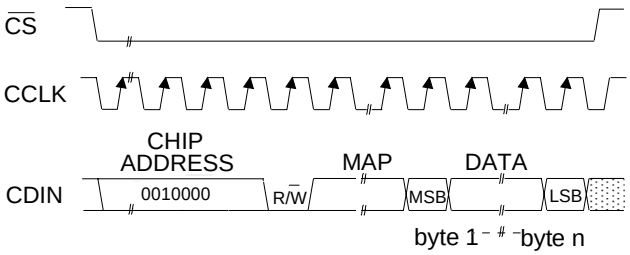
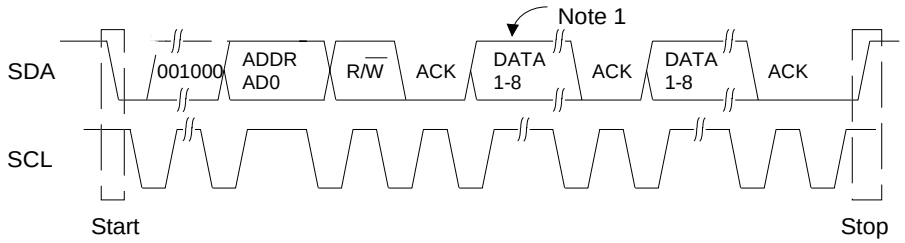


Figure 7. SPI Mode Control Port Formatting



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 8. I^2C Mode Control Port Formatting

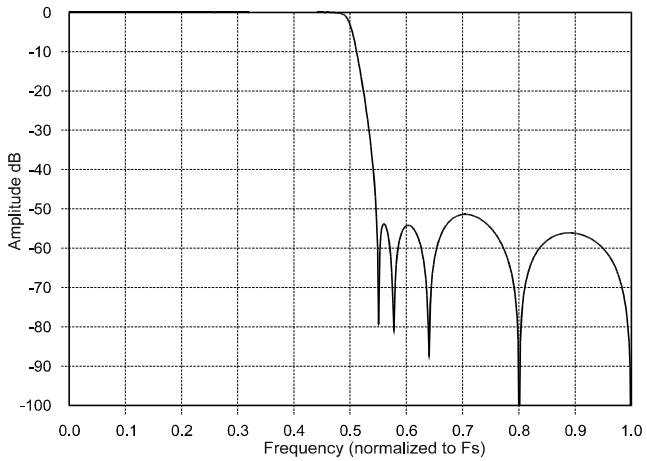


Figure 9. Base-Rate Stopband Rejection

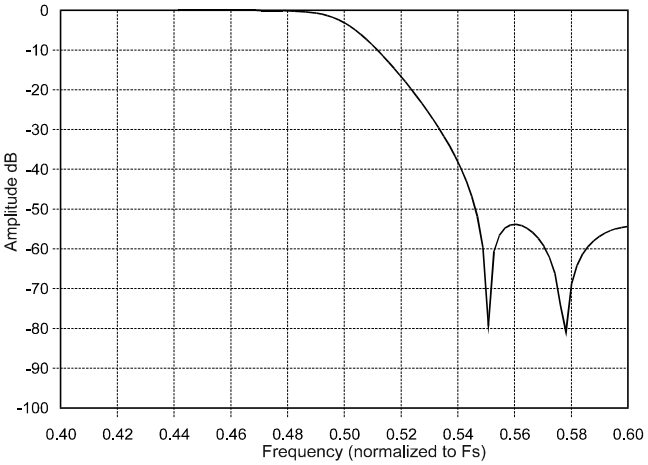


Figure 10. Base-Rate Transition Band

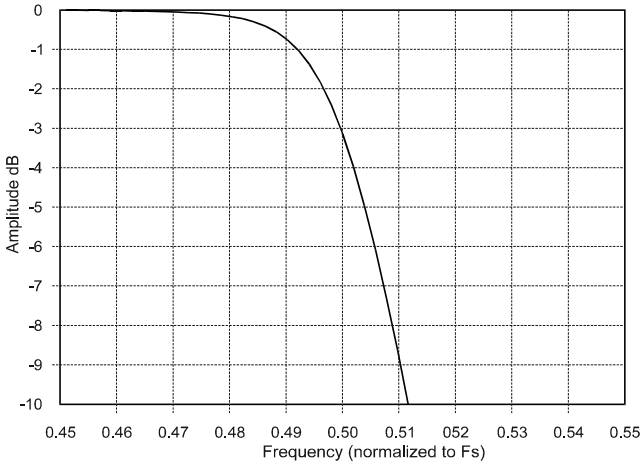


Figure 11. Base-Rate Transition Band (Detail)

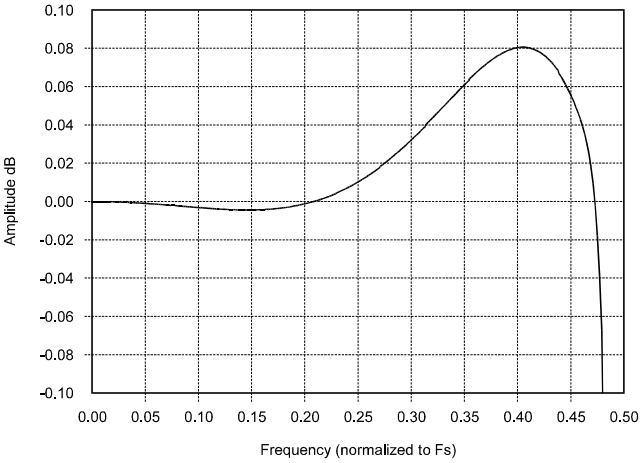


Figure 12. Base-Rate Passband Ripple

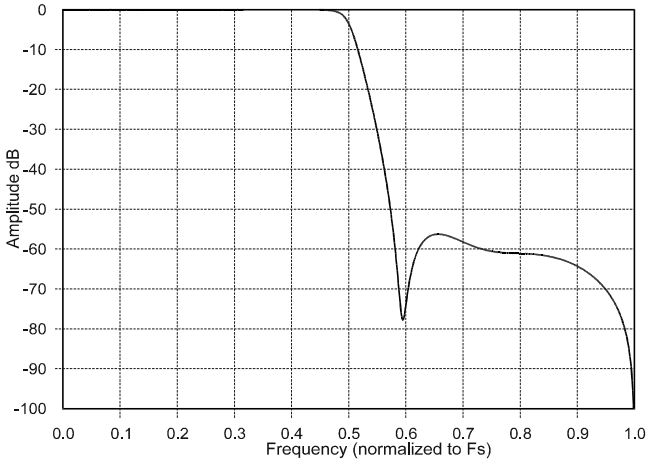


Figure 13. High-Rate Stopband Rejection

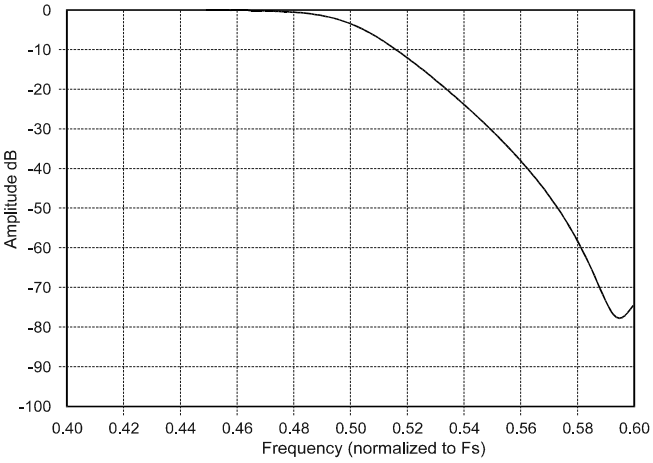


Figure 14. High-Rate Transition Band

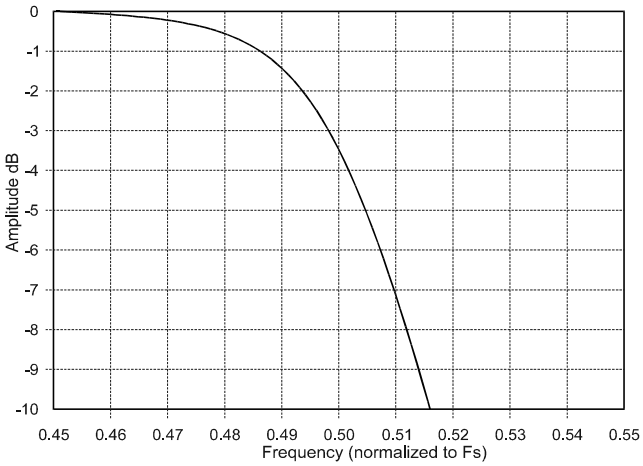


Figure 15. High-Rate Transition Band (Detail)

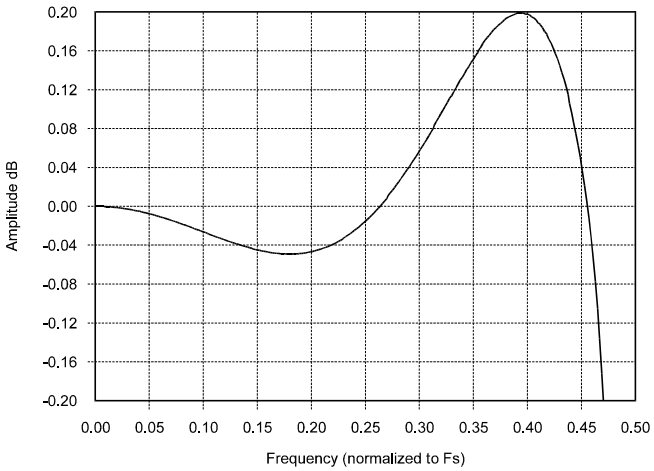


Figure 16. High-Rate Passband Ripple

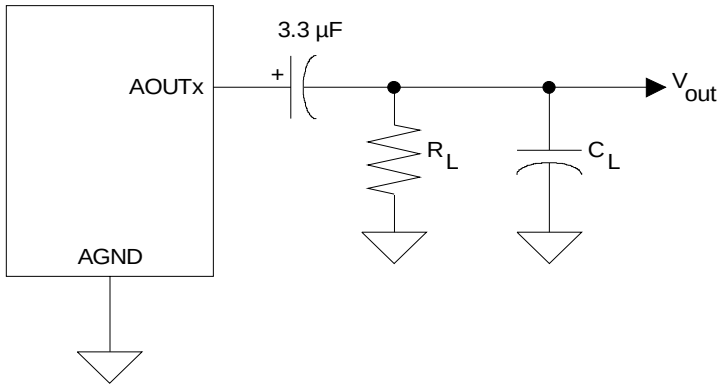


Figure 17. Output Test Load

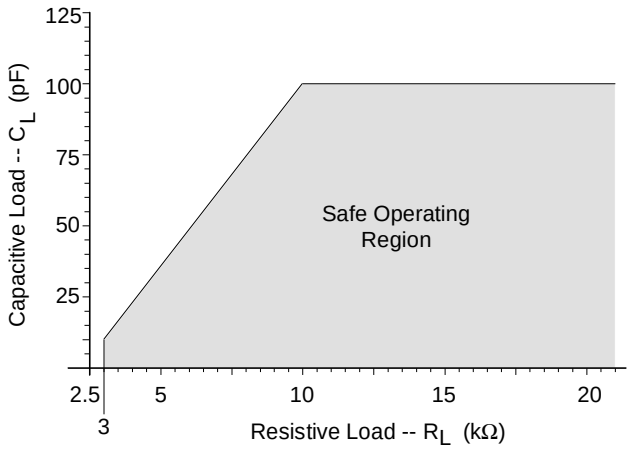


Figure 18. Maximum Loading

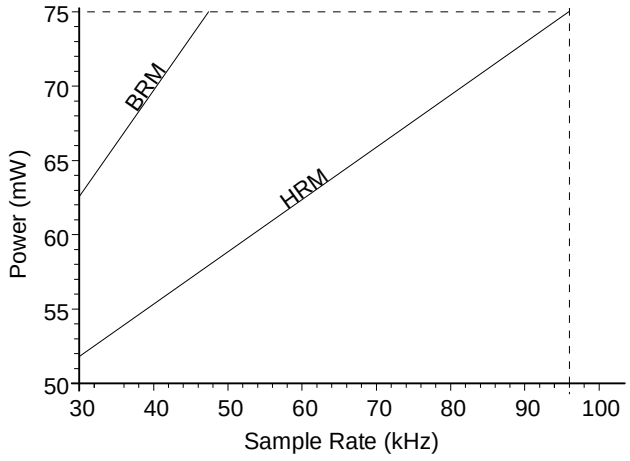
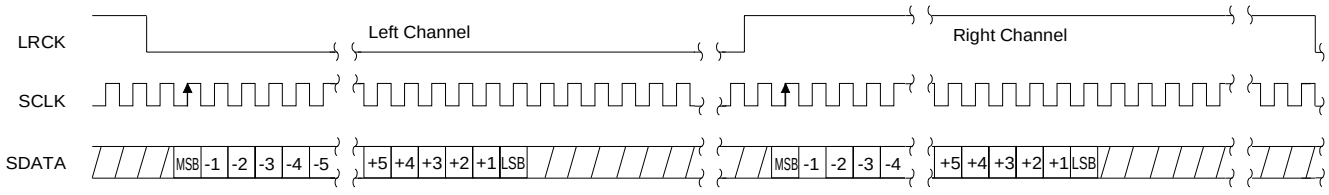
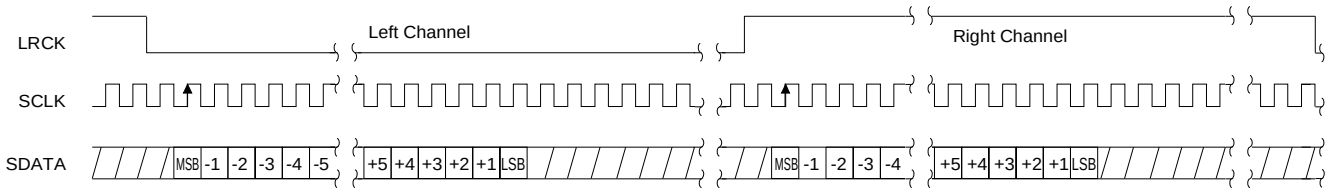


Figure 19. Power vs. Sample Rate (VA = 5V)



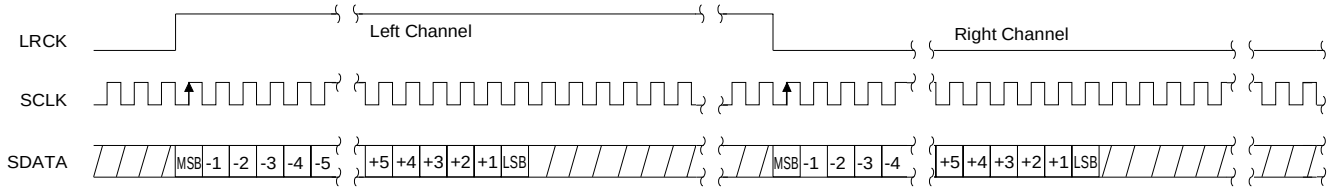
Internal SCLK Mode	External SCLK Mode
I^2S, Up to 24-Bit data and INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	I^2S, up to 24-Bit DataData Valid on Rising Edge of SCLK

Figure 20. CS43L41 Format 0 (I^2S)



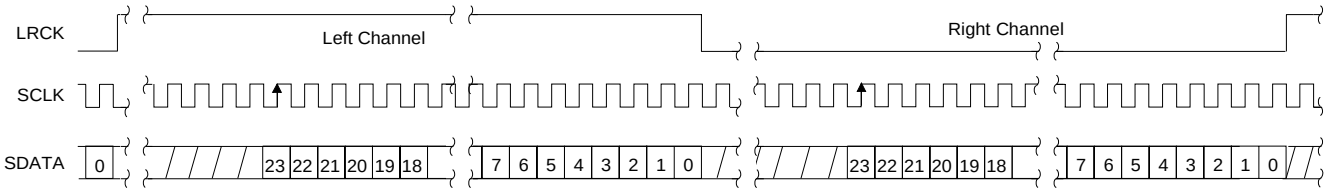
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	I^2S, up to 24-Bit DataData Valid on Rising Edge of SCLK

Figure 21. CS43L41 Format 1 (I^2S)



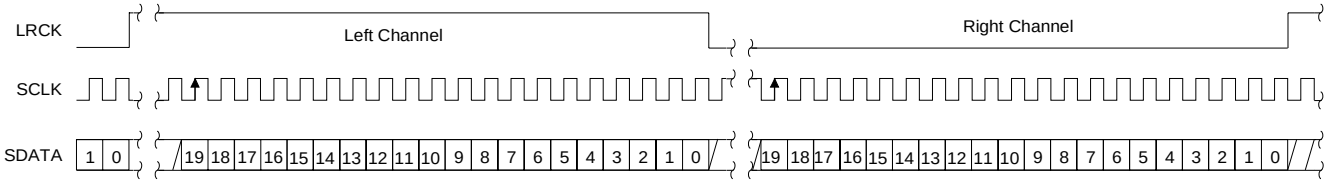
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit DataINT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Left Justified, up to 24-Bit DataData Valid on Rising Edge of SCLK

Figure 22. CS43L41 Format 2



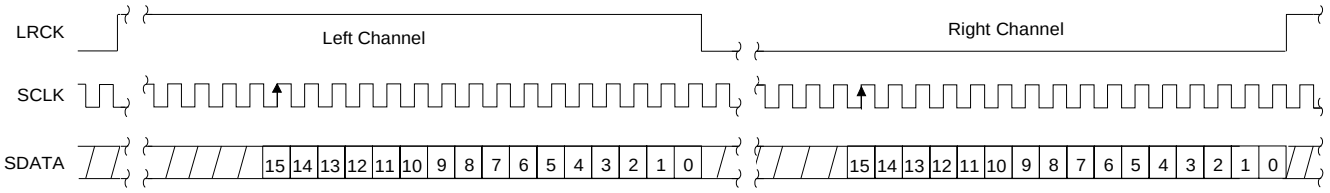
Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit DataINT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 24-Bit DataData Valid on Rising Edge of SCLKSCLK Must Have at Least 48 Cycles per LRCK Period

Figure 23. CS43L41 Format 3



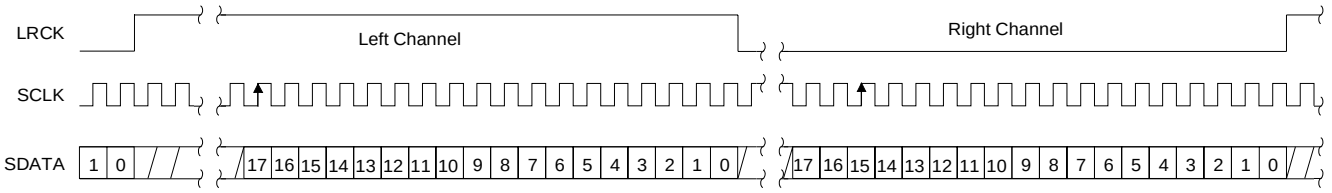
Internal SCLK Mode	External SCLK Mode
Right Justified, 20-Bit DataINT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 20-Bit DataData Valid on Rising Edge of SCLKSCLK Must Have at Least 40 Cycles per LRCK Period

Figure 24. CS43L41 Format 4



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit DataINT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 16-Bit DataData Valid on Rising Edge of SCLKSCLK Must Have at Least 32 Cycles per LRCK Period

Figure 25. CS43L41 Format 5



Internal SCLK Mode	External SCLK Mode
Right Justified, 18-Bit DataINT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 18-Bit DataData Valid on Rising Edge of SCLKSCLK Must Have at Least 36 Cycles per LRCK Period

Figure 26. CS43L41 Format 6

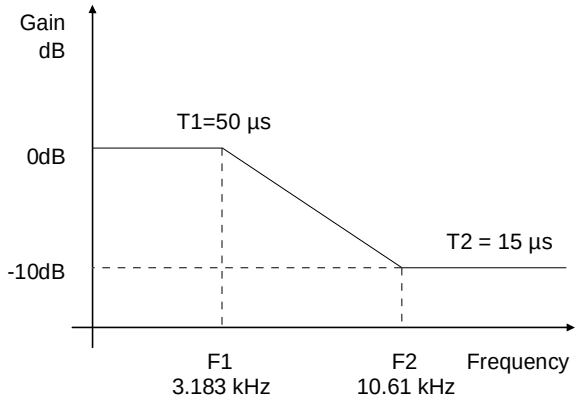


Figure 27. De-Emphasis Curve

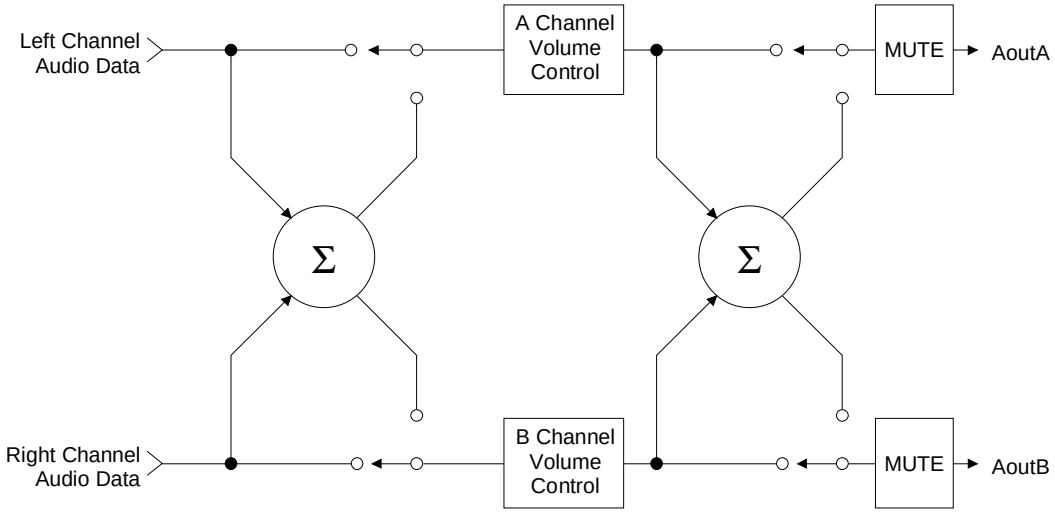


Figure 28. ATAPI Block Diagram

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

9. REFERENCES

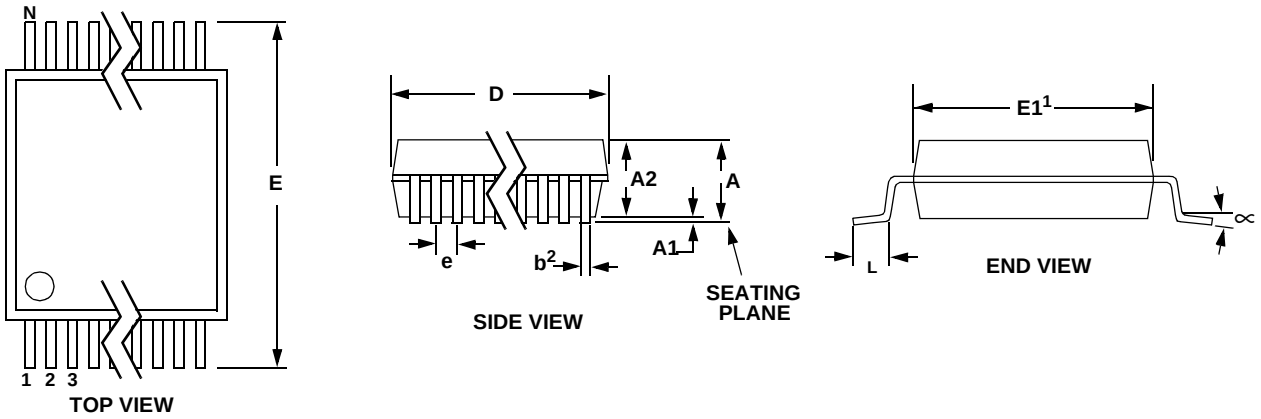
1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) CDB43L41 Evaluation Board Datasheet

3) "The I^2C Bus Specification: Version 2.0" Philips Semiconductors, December 1998. http://www.semiconductors.philips.com

10. PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.043	--	1.10	
A1	0.002	0.006	0.05	0.15	
A2	0.034	0.037	0.85	0.95	
b	0.008	0.012	0.19	0.30	2,3
D	0.193	0.201	4.90	5.10	1
E	0.248	0.256	6.30	6.50	
E1	0.169	0.177	4.30	4.50	1
e	--	0.026	--	0.65	
L	0.020	0.028	0.50	0.70	
∝	0°	8°	0°	8°	

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

• Notes •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