SSI 32R501/501R
4, 6, 8-Channel Ferrite Read/Write Device

1

July, 1990

DESCRIPTION

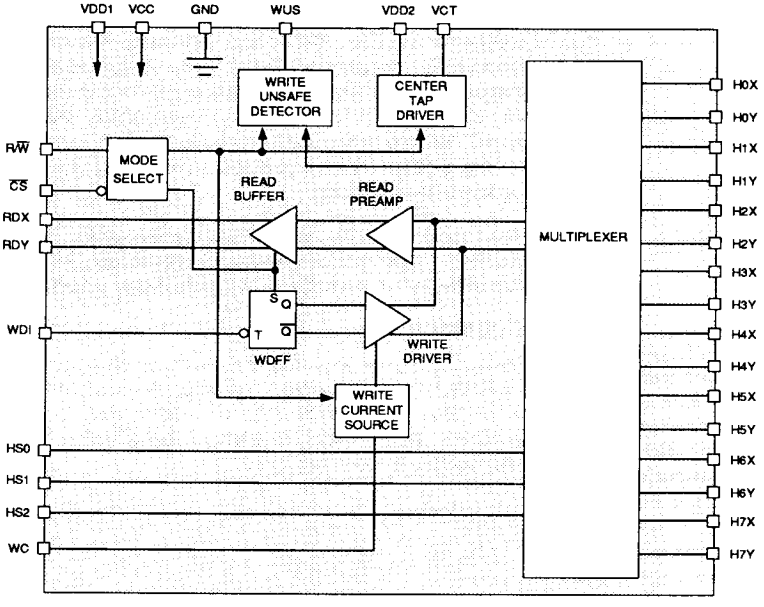
The SSI 32R501 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 8 channels. The SSI 32R501 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R501R performs the same function as the SSI 32R501 with the addition of internal damping resistors.

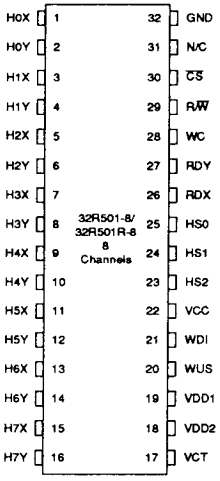
FEATURES

- **Single or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **1.5 nV/√Hz maximum input noise voltage**
- **+5V, +12V power supplies**
- **Mirror image package option**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW

CAUTION: Use handling procedures necessary for a static sensitive component.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

CIRCUIT OPERATION

The SSI 32R501 gives the user the ability to address up to eight center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in Tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R501 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

$$Iw = K/Rwc, \text{ where } K = \text{Write Current Constant}$$

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 120Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R501 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC		Write Current: used to set the magnitude of the write current
VCT		Voltage Center Tap: voltage source for head center tap
VCC		+5V
VDD1		+12V
VDD2		Positive power supply for the center tap voltage source
GND		Ground

* When more than one R/$\overline{W}$ device is used these signals can be wire OR'ed.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	Iw	60	mA
Output Current	RDX, RDY Io	-10	mA
Output Current	Ivct	-60	mA
Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temp. PDIP, Flatpack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

Powered by ICminer.com Electronic-Library Service CopyRight 2003

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R501 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 50 mA	114	120	126	Ω
Write Current	Iw		22		50	mA
Junction Temperature Range	Tj		+25		+135	°C
*For Iw = 50 mA. At other Iw levels refer to Applications Information that follows this specification.						

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			25	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			25	mA
(sum of VDD1 and VDD2)	Read Mode			50	mA
	Write Mode			30 + Iw	mA
Power Dissipation (Tj = +135°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 50 mA, RCT = 0Ω			1050	mW
	Write Mode, Iw = 50 mA RCT = 120Ω			750	mW

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DC CHARACTERISTICS (Continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage		-0.3		0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			85	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		6.0		VDC
Write Current Range		10		50	mA
Write Current Constant "K"		129		151	
Iwc to Head Current Gain			20		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		4.3		VDC
RDX, RDY Leakage	3.0 < RDX, RDY < 8.0V Write/Idle Mode	-50		+50	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode		4.0		VDC
Input Bias Current (differential)				100	µA
Output Offset Voltage	Read Mode	-480		+480	mV
Common Mode Output Voltage	Read Mode	5		7	VDC

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and Iw = 45 mA, Lh = 10 µH, Rd = 750Ω 32R501 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.5			V(pk)
Unselected Head Transient Current	5 µH ≤ Lh ≤ 9.5 µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R501	10K			Ω
	32R501R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 kΩ	80		120	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 KHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			23	pF
Differential Input Resistance	32R501, f = 5 MHz	2K			Ω
Differential Input Resistance	32R501R, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω

Powered by ICminer.com Electronic-Library Service CopyRight 2003

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Current	AC Coupled Load, RDX to RDY	2.0			mA
External Resistance Load	AC coupled to output per side to GND	100			Ω
Center tap output impedance	$0 \le f \le 5$ MHz			150	Ω

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			600	ns
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			600	ns
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			600	ns
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
WUS-Safe to Unsafe - TD1	Iw = 50 mA	1.6		8.0	µs
WUS-Unsafe to Safe - TD2	Iw = 20 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			30	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

Powered by ICminer.com Electronic-Library Service CopyRight 2003

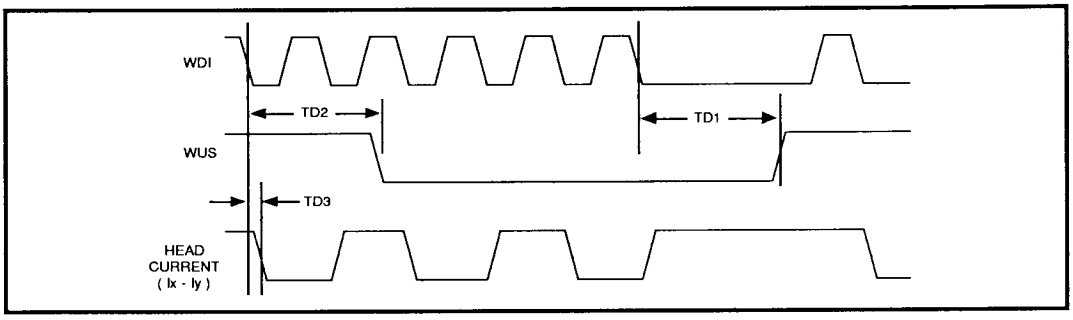
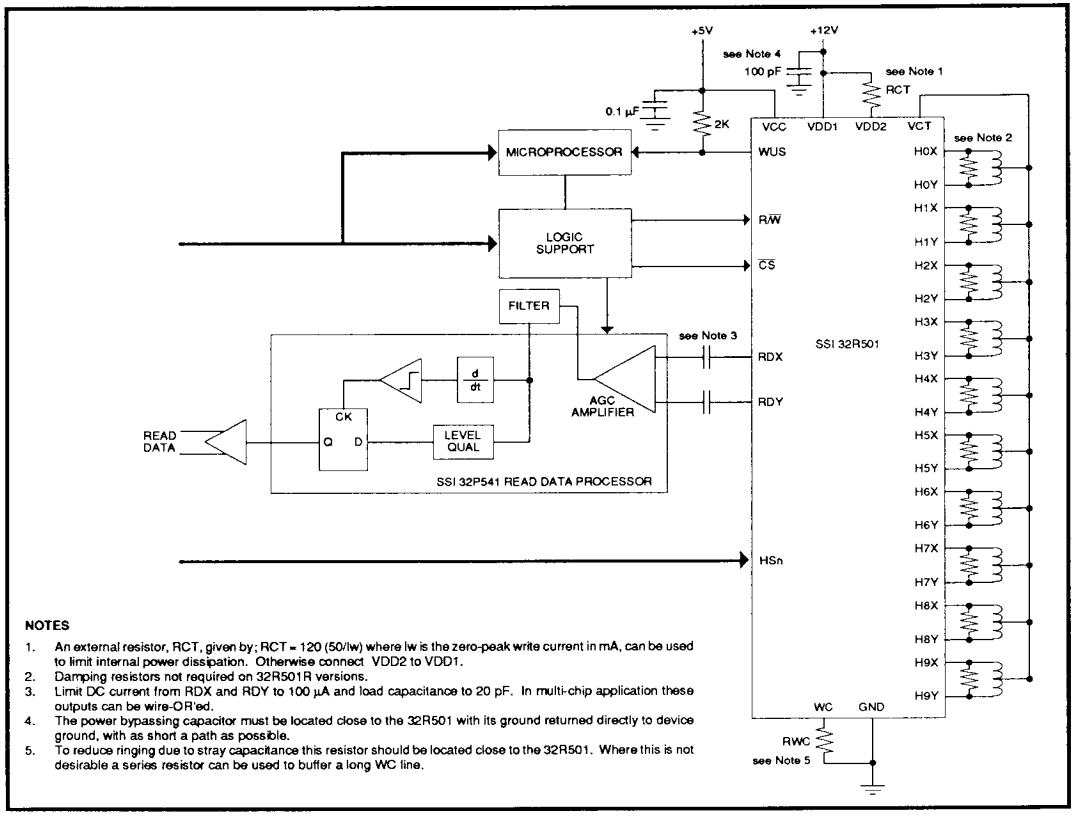


FIGURE 1: Write Mode Timing Diagram



NOTES

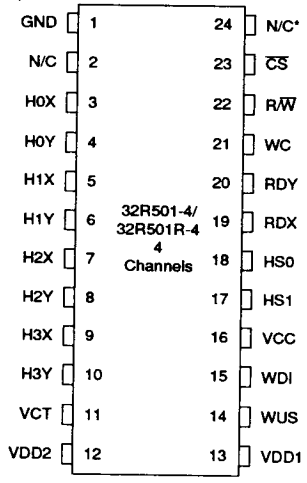
1. An external resistor, RCT, given by; RCT = 120 (50/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R501R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R501 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R501. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Applications Information

Powered by ICminer.com Electronic-Library Service CopyRight 2003

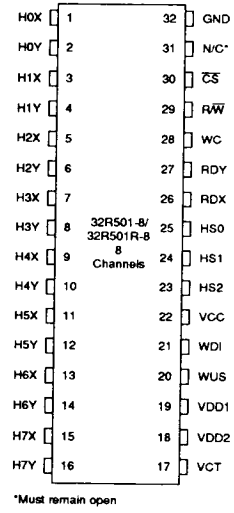
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



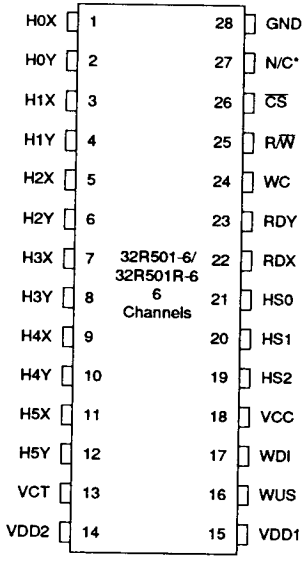
* Must remain open

24-Lead SOL



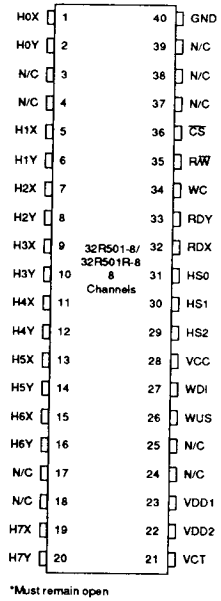
*Must remain open

32-Lead Flatpack, SOW



*Must remain open

28-Lead PDIP, SOL, Flatpack



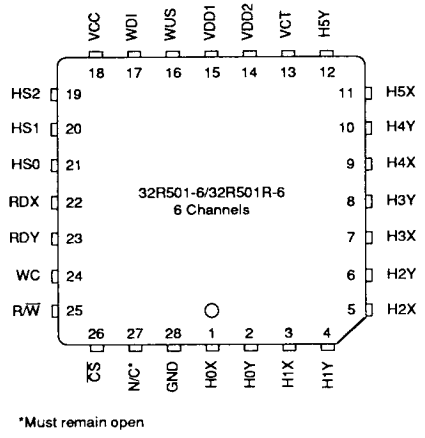
*Must remain open

40-Lead PDIP

Powered by ICminer.com Electronic-Library Service CopyRight 2003

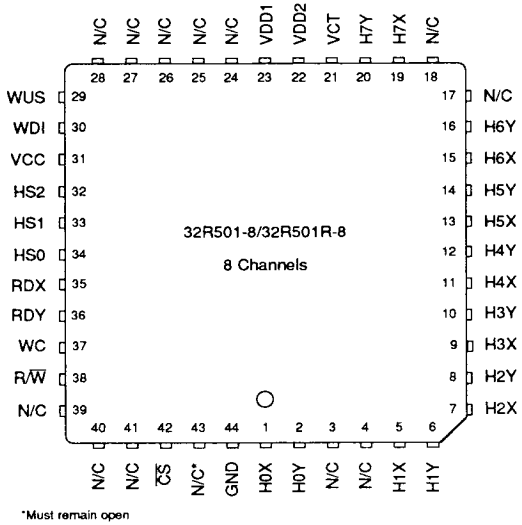
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



*Must remain open

28-Lead PLCC



*Must remain open

44-Lead PLCC

Powered by ICminer.com Electronic-Library Service CopyRight 2003

THERMAL CHARACTERISTICS: θja

24-lead	SOL	80°C/W	32-lead	FLATPACK	60°C/W
28-lead	PDIP	55°C/W		SOW	55°C/W
	PLCC	65°C/W	40-lead	PDIP	45°C/W
	SOL	70°C/W	44-lead	PLCC	60°C/W
	Flatpack	65°C/W			

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R501		
4-Channel SOL	SSI 32R501-4CL	32R501-4CL
6-Channel Flatpack	SSI 32R501-6F	32R501-6F
6-Channel PLCC	SSI 32R501-6CH	32R5O1-6CH
6-Channel SOL	SSI 32R501-6CL	32R501-6CL
6-Channel PDIP	SSI 32R501-6CP	32R501-6CP
8-Channel Flatpack	SSI 32R501-8F	32R501-8F
8-Channel SOW	SSI 32R501-8CW	32R501-8CW
8-Channel PDIP	SSI 32R501-8CP	32R501-8CP
8-Channel PLCC	SSI 32R501-8CH	32R501-8CH
SSI 32R501R		
4-Channel SOL	SSI 32R501R-4CL	32R501R-4CL
6-Channel Flatpack	SSI 32R501R-6F	32R501R-6F
6-Channel PLCC	SSI 32R501R-6CH	32R501R-6CH
6-Channel SOL	SSI 32R501R-6CL	32R501R-6CL
6-Channel PDIP	SSI 32R501R-6CP	32R501R-6CP
8-Channel Flatpack	SSI 32R501R-8F	32R501R-8F
8-Channel SOW	SSI 32R501R-8CW	32R501R-8CW
8-Channel PDIP	SSI 32R501R-8CP	32R501R-8CP
8-Channel PLCC	SSI 32R501R-8CH	32R501R-8CH

No responsibility is assumed by Silicon Systems for use of this product nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. No license is granted under any patents, patent rights or trademarks of Silicon Systems. Silicon Systems reserves the right to make changes in specifications at any time without notice. Accordingly, the reader is cautioned to verify that the data sheet is current before placing orders.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

©1989 Silicon Systems, Inc.

Powered by ICminer.com Electronic-Library Service CopyRight 2003