DATA SHEET

74LVC4066
Quad bilateral switches

Product specification

2003 Aug 12

Philips
Semiconductors

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Quad bilateral switches 74LVC4066

FEATURES

- Very low ON resistance:
  - 7.5 Ω (typical) at V_{CC} = 2.7 V
  - 6.5 Ω (typical) at V_{CC} = 3.3 V
  - 6 Ω (typical) at V_{CC} = 5 V.
- ESD protection:
  - HBM EIA/JESD22-A114-A Exceeds 2000 V
  - MM EIA/JESD22-A115-A Exceeds 200 V.
- High noise immunity
- CMOS low power consumption
- Latch up performance exceeds 250 mA
- Complies with JEDEC standard no. 8-1A
- Direct interface TTL-levels.

DESCRIPTION

The 74LVC4066 is a high-speed Si-gate CMOS device.

The 74LVC4066 has four independent analog switches. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3 V	2.5	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5 V	1.9	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3 V	3.4	ns
		C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5 V	2.5	ns
C_I	input capacitance	V_{CC} = 3 V	3.5	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; notes 1 and 2	12.5	pF
C_S	switch capacitance	OFF-state	8.0	pF
		ON-state	14.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   C_S = switch capacitance.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT nE	SWITCH
L	OFF
H	ON

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC4066D	–40 to +125 °C	14	SO14	plastic	SOT108-2
74LVC4066PW	–40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC4066BQ	–40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1Y	independent input/output
2	1Z	independent output/input
3	2Z	independent output/input
4	2Y	independent input/output
5	2E	enable input (active HIGH)
6	3E	enable input (active HIGH)
7	GND	ground (0 V)
8	3Y	independent input/output
9	3Z	independent output/input
10	4Z	independent output/input
11	4Y	independent input/output
12	4E	enable input (active HIGH)
13	1E	enable input (active HIGH)
14	V_{CC}	supply voltage

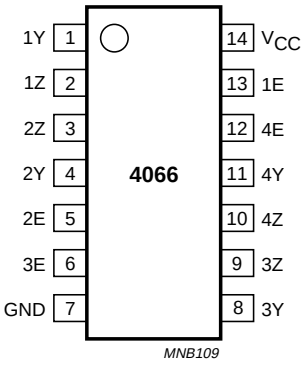
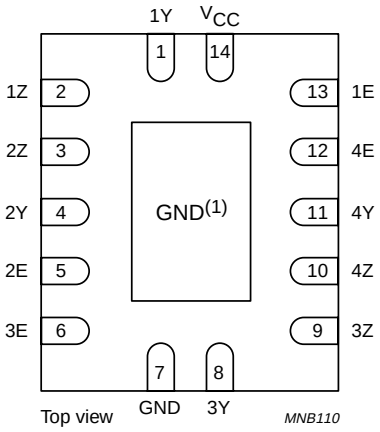


Fig.1 Pin configuration SO14 and TSSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

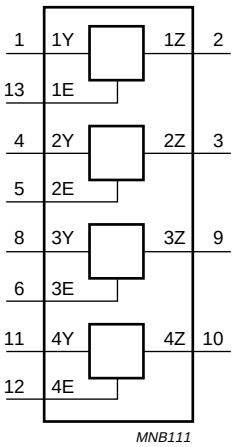


Fig.3 Logic symbol.

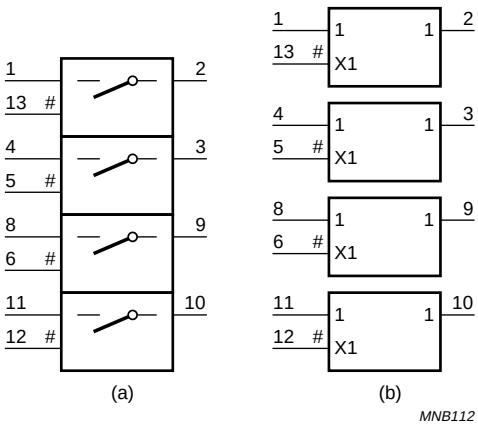


Fig.4 logic symbol (IEEE/IEC).

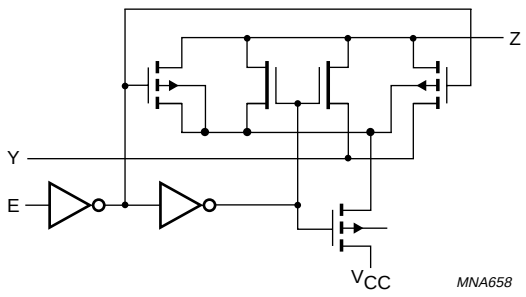


Fig.5 Logic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_S	switch voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); see note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
V_I	input voltage	note 2	–0.5	+6.5	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	–	–50	mA
I_{SK}	switch diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±50	mA
V_S	switch voltage	enable and disable mode	–0.5	+6.5	V
I_S	switch source or sink current	$–0.5 < V_S < V_{CC} + 0.5$ V	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 3	–	500	mW

Notes

1. To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminal Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminal Y. In this case there is no limit for the voltage drop across the switch, but the voltage at Y and Z may not exceed V_{CC} or GND.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. For SO14 packages: above 70 °C derate linearly with 8 mW/K.

   For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.30V_{CC}$	V
I_{LI}	input leakage current (control pin)	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND; see Fig.7	5.5	–	±0.1	±5	μA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND; see Fig.8	5.5	–	±0.1	±5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC}$ – 0.6 V; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.30V_{CC}$	V
I_{LI}	input leakage current (control pin)	V_I = 5.5 V or GND	5.5	–	–	±20	μA
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ − GND; see Fig.7	5.5	–	–	±20	μA
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ − GND; see Fig.8	5.5	–	–	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC}$ − 0.6 V; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	–	5000	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Resistance R_{ON}

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	I_S (mA)	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1; see Fig.6								
$R_{ON(peak)}$	ON-resistance (peak)	V_S = GND to V_{CC}; $V_I = V_{IH}$	4	1.65 to 1.95	–	35	100	Ω
			8	2.3 to 2.7	–	14	30	Ω
			12	2.7	–	11.5	25	Ω
			24	3.0 to 3.6	–	8.5	20	Ω
			32	4.5 to 5.5	–	6.5	15	Ω
$R_{ON(rail)}$	ON-resistance (rail)	V_S = GND; $V_I = V_{IH}$	4	1.65 to 1.95	–	10	30	Ω
			8	2.3 to 2.7	–	8.5	20	Ω
			12	2.7	–	7.5	18	Ω
			24	3.0 to 3.6	–	6.5	15	Ω
			32	4.5 to 5.5	–	6	10	Ω
		$V_S = V_{CC}$; $V_I = V_{IH}$	4	1.65 to 1.95	–	12	30	Ω
			8	2.3 to 2.7	–	8.5	20	Ω
			12	2.7	–	7.5	18	Ω
			24	3.0 to 3.6	–	6.5	15	Ω
			32	4.5 to 5.5	–	6	10	Ω
$R_{ON(flatness)}$	ON-resistance (flatness)	V_S = GND to V_{CC}; $V_I = V_{IH}$; see Figs.10 to 13	4	1.8	–	100	–	Ω
			8	2.5	–	17	–	Ω
			12	2.7	–	10	–	Ω
			24	3.3	–	5	–	Ω
			32	5.0	–	3	–	Ω

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	I_S (mA)	V_{CC} (V)				
T_{amb} = −40 to +125 °C; see Fig.6								
$R_{ON(peak)}$	ON-resistance (peak)	V_S = GND to V_{CC}; $V_I = V_{IH}$	4	1.65 to 1.95	–	–	150	Ω
			8	2.3 to 2.7	–	–	45	Ω
			12	2.7	–	–	38	Ω
			24	3.0 to 3.6	–	–	30	Ω
			32	4.5 to 5.5	–	–	23	Ω
$R_{ON(rail)}$	ON-resistance (rail)	V_S = GND; $V_I = V_{IH}$	4	1.65 to 1.95	–	–	45	Ω
			8	2.3 to 2.7	–	–	30	Ω
			12	2.7	–	–	27	Ω
			24	3.0 to 3.6	–	–	23	Ω
			32	4.5 to 5.5	–	–	15	Ω
		$V_S = V_{CC}$; $V_I = V_{IH}$	4	1.65 to 1.95	–	–	45	Ω
			8	2.3 to 2.7	–	–	30	Ω
			12	2.7	–	–	27	Ω
			24	3.0 to 3.6	–	–	23	Ω
			32	4.5 to 5.5	–	–	15	Ω

Note

1. Typical value $R_{on(flatness)}$ is measured at T_{amb} = −40 to +85 °C, all other typical values are measured at T_{amb} = 25 °C.

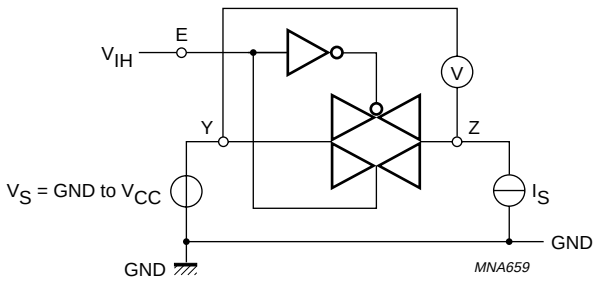


Fig.6 Test circuit for measuring ON-state resistance (R_{ON}).

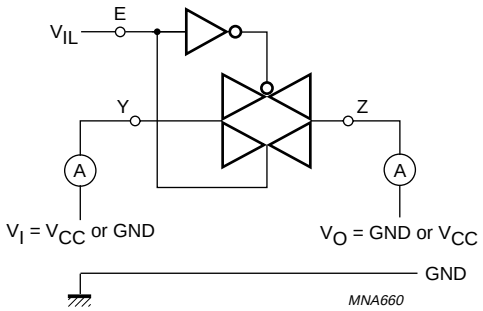


Fig.7 Test circuit for measuring OFF-state current.

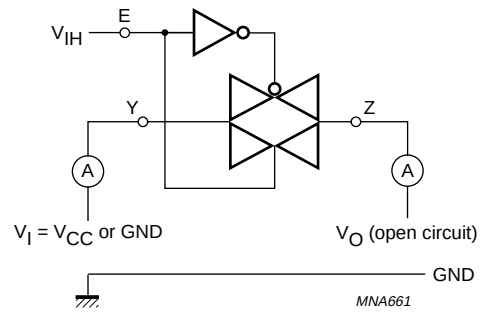


Fig.8 Test circuit for measuring ON-state current.

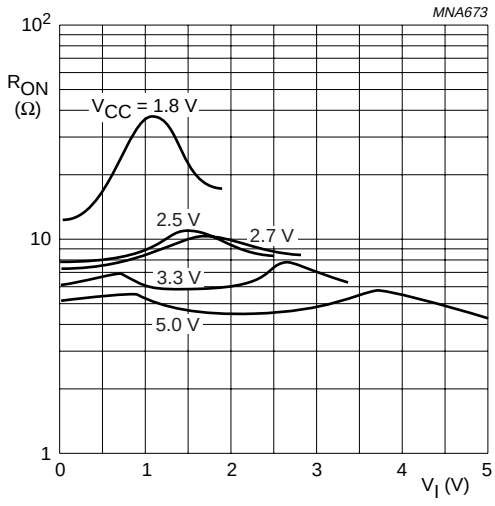


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_S) for V_S = GND to V_{CC}.

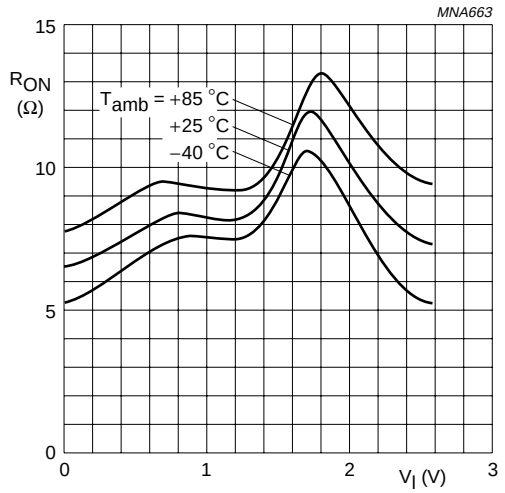


Fig.10 R_{ON} for V_{CC} = 2.5 V.

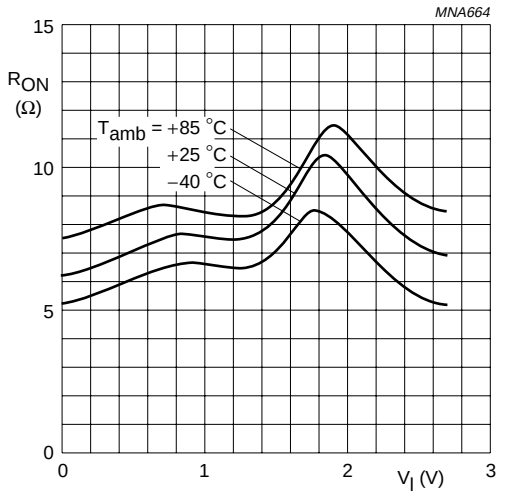


Fig.11 R_{ON} for V_{CC} = 2.7 V.

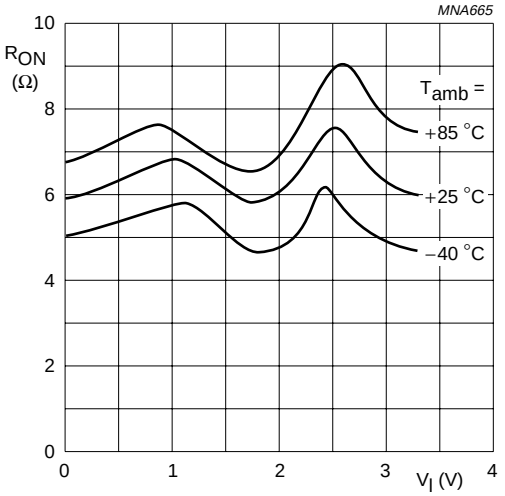


Fig.12 R_{ON} for V_{CC} = 3.3 V.

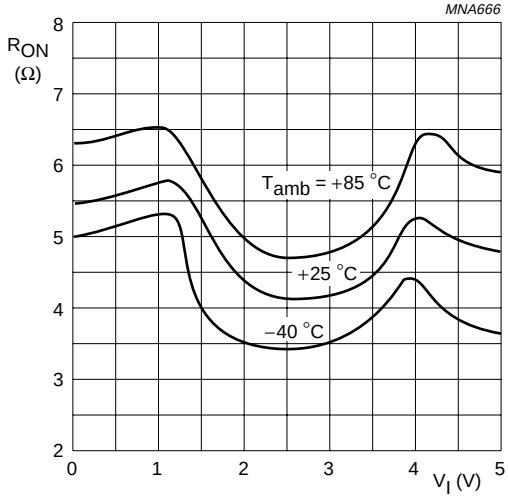


Fig.13 R_{ON} for V_{CC} = 5.0 V.

AC CHARACTERISTICS

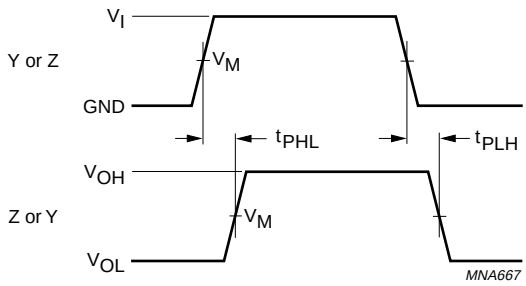
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay nY to nZ or nZ to nY	see Figs 14 and 16; note 2	1.65 to 1.95	–	0.8	2.0	ns
			2.3 to 2.7	–	0.4	1.2	ns
			2.7	–	0.4	1.0	ns
			3.0 to 3.6	–	0.3	0.8	ns
			4.5 to 5.5	–	0.2	0.6	ns
t_{PZH}/t_{PZL}	turn-ON time E to V_{OS}	see Figs 15 and 16	1.65 to 1.95	1.0	5.3	10	ns
			2.3 to 2.7	1.0	3.0	5.6	ns
			2.7	1.0	2.6	5.0	ns
			3.0 to 3.6	1.0	2.5	4.4	ns
			4.5 to 5.5	1.0	1.9	3.9	ns
t_{PHZ}/t_{PLZ}	turn-OFF time E to V_{OS}	see Figs 15 and 16	1.65 to 1.95	1.0	4.2	9.0	ns
			2.3 to 2.7	1.0	2.4	5.5	ns
			2.7	1.0	3.6	6.5	ns
			3.0 to 3.6	1.0	3.4	6.0	ns
			4.5 to 5.5	1.0	2.5	5.0	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nY to nZ or nZ to nY	see Figs 14 and 16; note 2	1.65 to 1.95	–	–	3.0	ns
			2.3 to 2.7	–	–	2.0	ns
			2.7	–	–	1.5	ns
			3.0 to 3.6	–	–	1.5	ns
			4.5 to 5.5	–	–	1.0	ns
t_{PZH}/t_{PZL}	turn-ON time E to V_{OS}	see Figs 15 and 16	1.65 to 1.95	1.0	–	12.5	ns
			2.3 to 2.7	1.0	–	7.0	ns
			2.7	1.0	–	6.5	ns
			3.0 to 3.6	1.0	–	5.5	ns
			4.5 to 5.5	1.0	–	5.0	ns
t_{PHZ}/t_{PLZ}	turn-OFF time E to V_{OS}	see Figs 15 and 16	1.65 to 1.95	1.0	–	11.5	ns
			2.3 to 2.7	1.0	–	7.0	ns
			2.7	1.0	–	8.5	ns
			3.0 to 3.6	1.0	–	7.5	ns
			4.5 to 5.5	1.0	–	6.5	ns

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. t_{PHL}/t_{PLH} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

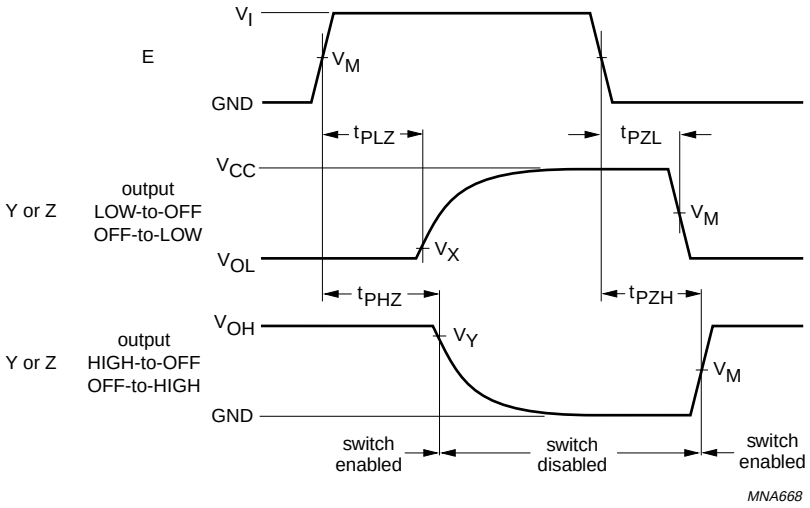
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 and 3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.14 The input (V_S) to output (V_O) propagation delays.

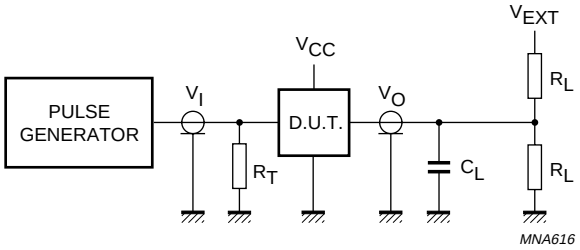


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 and 3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5V_{CC}$	V_{CC}	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.15 Turn-on and turn-off times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 and 3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2V_{CC}$

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.16 Load circuitry for switching times.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values at T_{amb} = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYPICAL	UNIT
d_{sin}	sine-wave distortion	R_L = 10 kΩ; C_L = 50 pF; f_{in} = 1 kHz; see Fig.18	1.65	0.032	%
			2.3	0.008	%
			3	0.006	%
			4.5	0.005	%
		R_L = 10 kΩ; C_L = 50 pF; f_{in} = 10 kHz; see Fig.18	1.65	0.068	%
			2.3	0.009	%
			3	0.008	%
			4.5	0.006	%
f_{ON}	switch ON signal frequency response	R_L = 600 Ω; C_L = 50 pF; see Fig.17; note 1	1.65	170	MHz
			2.3	210	MHz
			3	212	MHz
			4.5	215	MHz
		R_L = 50 Ω; C_L = 5 pF; see Fig.17; note 1	1.65	> 500	MHz
			2.3	> 500	MHz
			3	> 500	MHz
			4.5	> 500	MHz

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYPICAL	UNIT
$\alpha_{OFF(feedthru)}$	switch OFF signal feed-through attenuation	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; see Fig.19; note 2	1.65	–46	dB
			2.3	–46	dB
			3	–46	dB
			4.5	–46	dB
		R_L = 50 Ω; C_L = 5 pF; f_{in} = 1 MHz; see Fig.19; note 2	1.65	–42	dB
			2.3	–42	dB
			3	–42	dB
			4.5	–42	dB
$\alpha_{ct(E-Y/Z)}$	crosstalk between control input to signal output	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; $t_r = t_f$ = 2 ns; see Fig.20	1.65	69	mV
			2.3	87	mV
			3	156	mV
			4.5	302	mV
$\alpha_{ct(S)}$	crosstalk between switches)	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1 MHz; see Fig.21	1.65	–58	dB
			2.3	–58	dB
			3	–58	dB
			4.5	–58	dB
		R_L = 50 Ω; C_L = 5 pF; f_{in} = 1 MHz; see Fig.21	1.65	–58	dB
			2.3	–58	dB
			3	–58	dB
			4.5	–58	dB
C_{PD}	power dissipation capacitance	f_{in} = 10 MHz	2.5	11.0	pF
			3.3	12.5	pF
			5.0	15.6	pF
Q	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f = 1 MHz; R_L = 1 MΩ; see Fig.22; note 3	3.3	0.8	pC
			5.5	1.2	pC

Notes

1. Adjust f_{in} voltage to obtain 0 dBm level at output. Increase f_{in} frequency until dB meter reads –3 dB.
2. Adjust f_{in} voltage to obtain 0 dBm level at input.
3. Guaranteed by design.

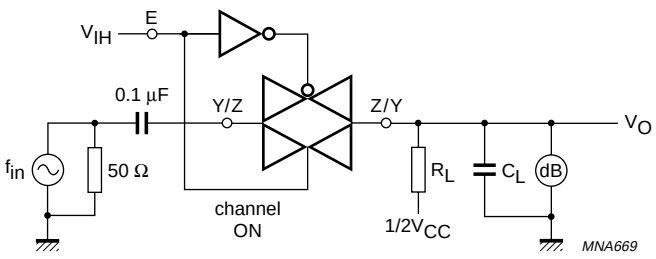
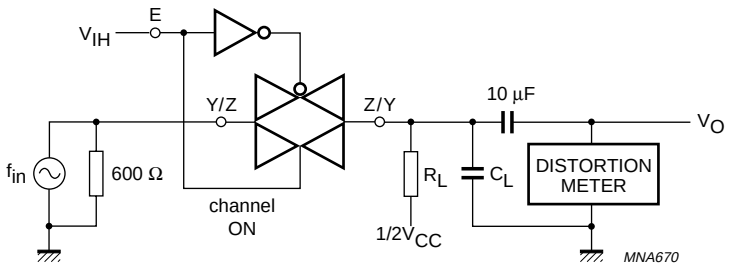


Fig.17 Test circuit for measuring the frequency response when switch is ON.



V_{CC}	V_{IH}
1.65 V	1.4 V (p-p)
2.3 V	2 V (p-p)
3 V	2.5 V (p-p)
4. V	4 V (p-p)

Fig.18 Test circuit for measuring sine-wave distortion.

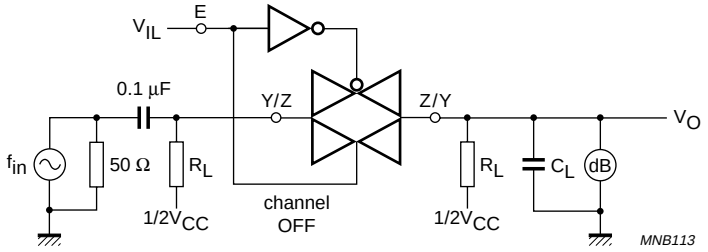


Fig.19 Test circuit for measuring feed-through when switch is OFF.

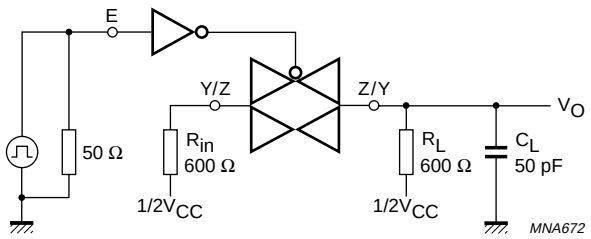


Fig.20 Crosstalk between control input to signal output.

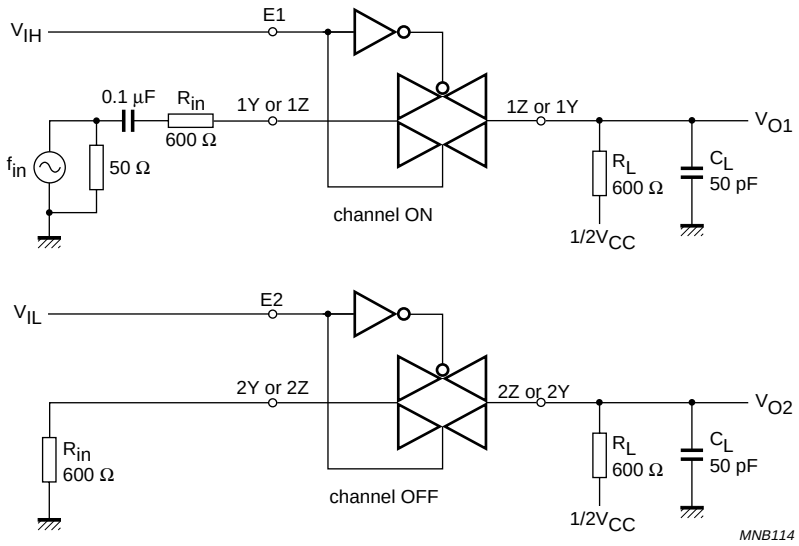
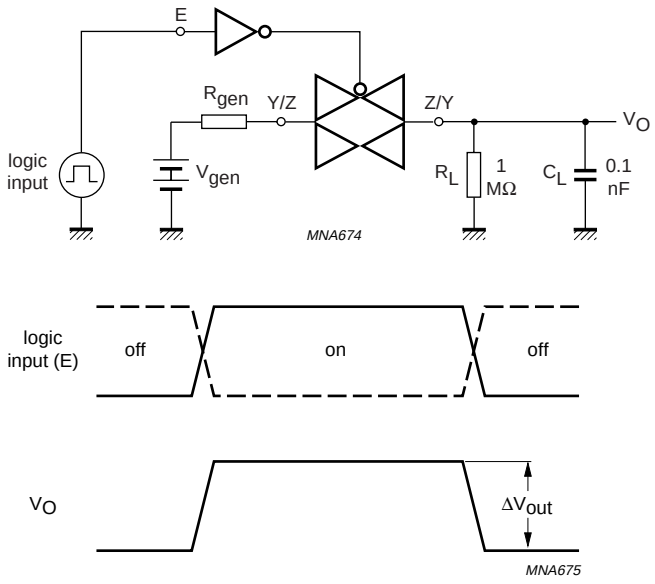


Fig.21 Crosstalk between switches.

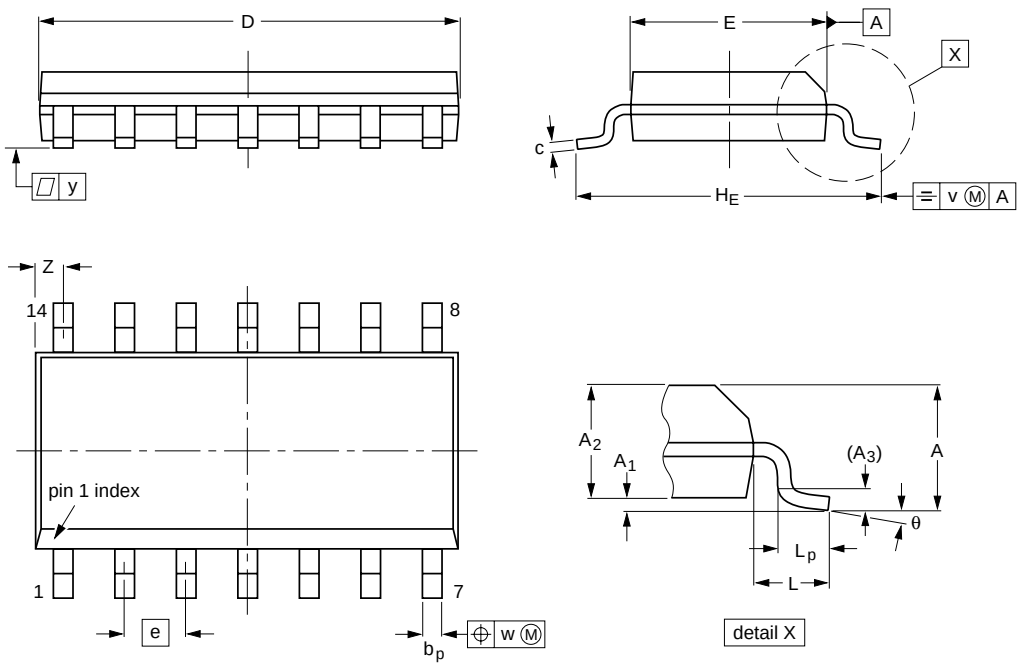


$Q = \Delta V_{out} \times C_L$

Fig.22 Charge injection test.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm **SOT108-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

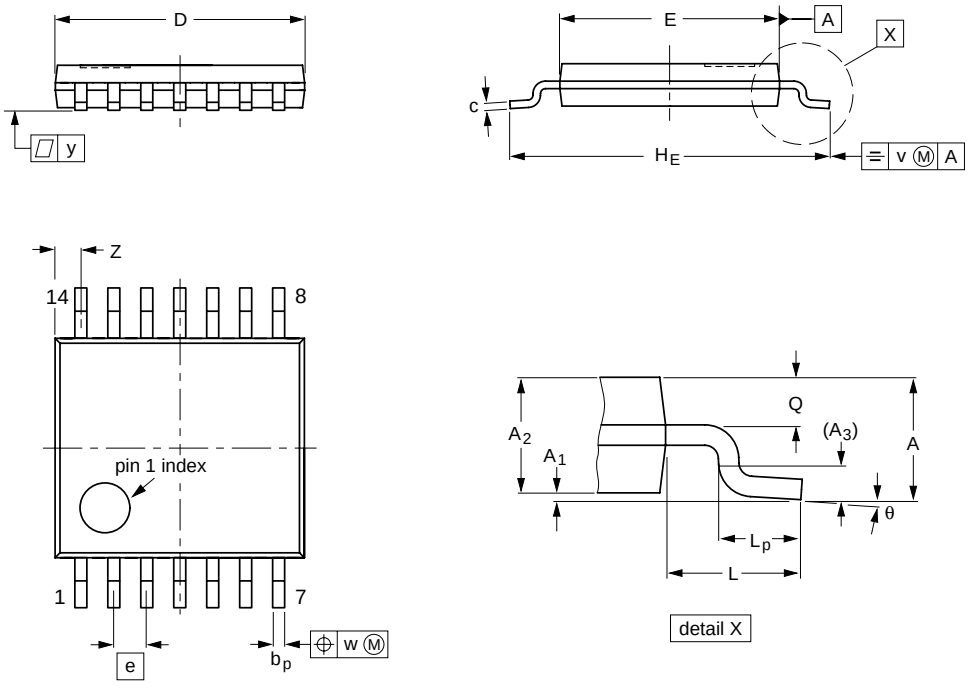
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.55 1.40	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.061 0.055	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.01	0.01	0.004	0.028 0.012	

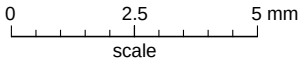
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-2		MS-012				~~01-05-29~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

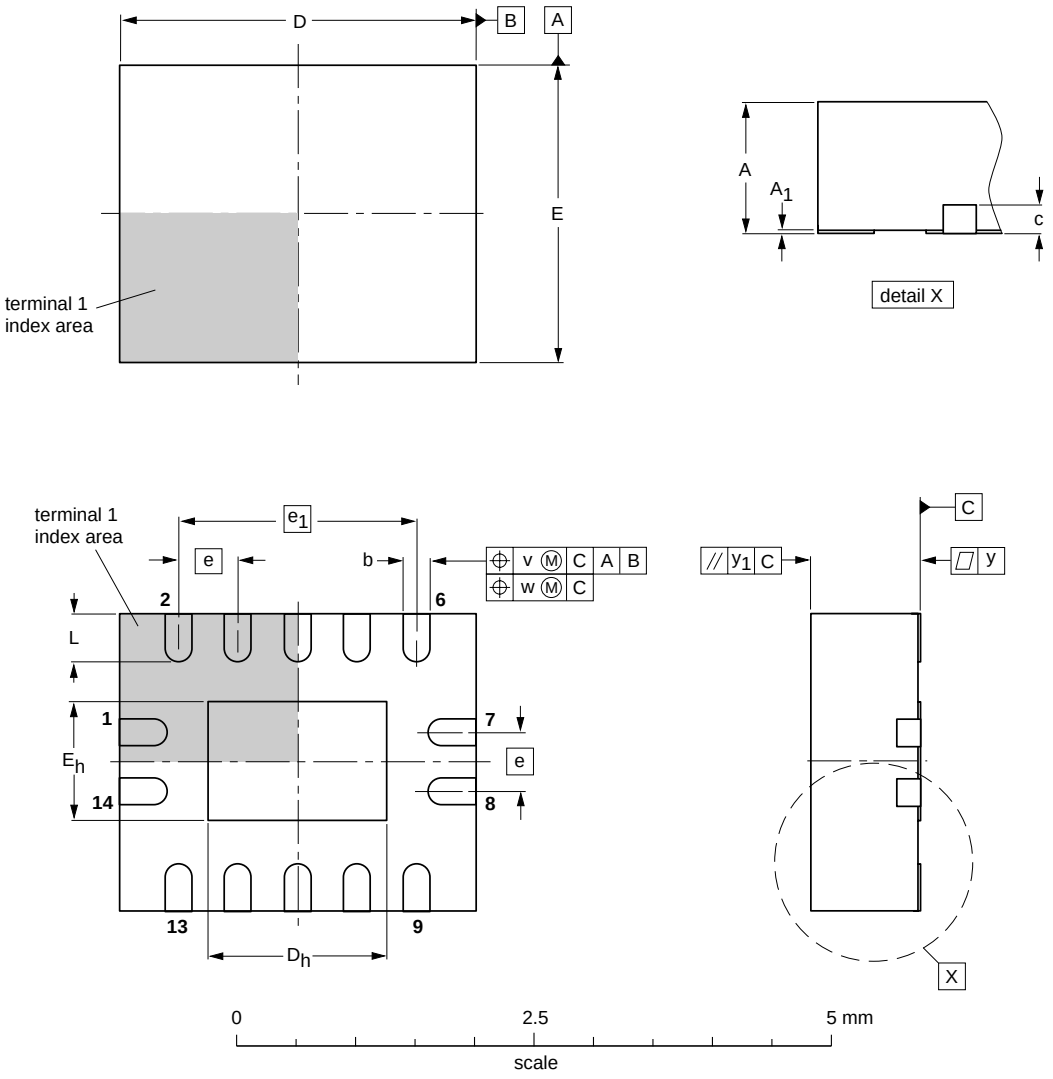
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

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Printed in The Netherlands 613508/01/pp23 Date of release: 2003 Aug 12 Document order number: 9397 750 11652

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