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## 1M x 32 SRAM MODULE

### PUMA 84SV32000 - 70/85/10

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#### Description

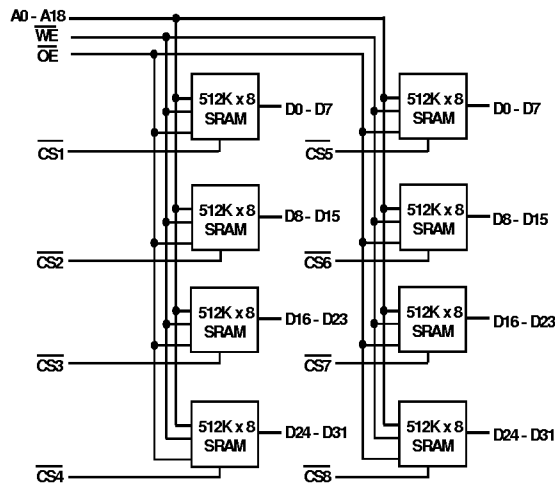
The PUMA 84SV32000 is a 32Mbit CMOS Low Voltage Static RAM organised as 1M x 32 in a JEDEC 84 pin surface mount J-leaded PLCC, available with access times of 70, 85, and 100ns. The output width is user configurable as 8, 16 or 32 bits using eight Chip Selects ( $\overline{CS1} \sim \overline{CS8}$ ).

The PUMA 84SV32000 offers a dramatic space saving advantage over eight standard 512Kx8 devices. The -L version has data retention capability and can be used in battery backup applications.

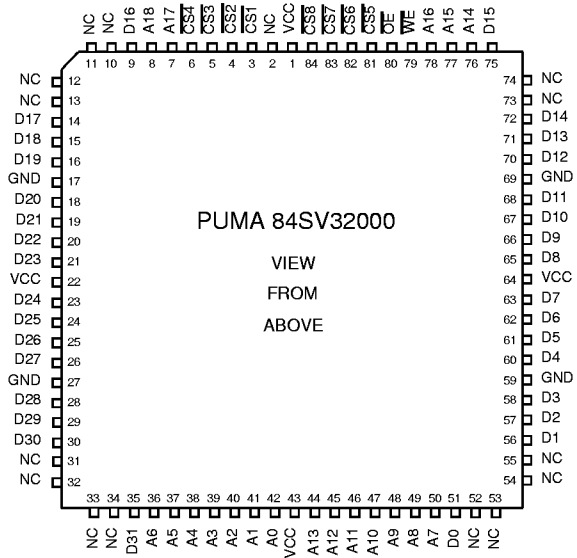
#### Features

- Access times of 70/85/100 ns.
- High Density Package.
- JEDEC 84 'J' leaded plastic Surface Mount Package.
- Single 3.3V±10% Power supply.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power (32-BIT) 864 mW (max)  
 Low Power Standby (-L) 1.4 mW (max)
- Fully Static operation.
- Data Retention Capability (-L version only).
- Multiple ground pins for maximum noise immunity.

#### Block Diagram



#### Pin Definition



#### Pin Functions

Address Inputs	<b>A0 ~ A18</b>
Data Input/Output	<b>D0 ~ D31</b>
Chip Select	<b><math>\overline{CS1} \sim \overline{CS8}</math></b>
Write Enable	<b><math>\overline{WE}</math></b>
Output Enable	<b><math>\overline{OE}</math></b>
No Connect	<b>NC</b>
Power (+5V)	<b>V<sub>cc</sub></b>
Ground	<b>GND</b>

#### Package Details

Plastic 84 J-Leaded JEDEC PLCC

**DC OPERATING CONDITIONS****Absolute Maximum Ratings**<sup>(1)</sup>

Voltage on any pin relative to GND	$V_T$	-0.3V to $V_{CC}+0.5V$
Power Dissipation	$P_T$	3.0 W
Storage Temperature	$T_{STG}$	-55 to +125 °C

Notes (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	min	typ	max	Units
Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
Max Terminal Voltage	$V_{TERM}$	-0.3	-	4.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$ <sup>(1)</sup>	-0.3	-	0.4	V
Operating Temperature	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C ( Suffix I )

Notes: (1) Pulse width: -3.0V for less than 20ns.

**DC Electrical Characteristics** ( $V_{CC}=5V\pm 10\%$ ,  $T_A=-40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$I_{LI1}$	$V_{IN}=0V$ to $V_{CC}$	-8	-	8	$\mu A$
Output Leakage Current	$I_{LO}$	$V_{IO}=0V$ to $V_{CC}$	-8	-	8	$\mu A$
Operating Supply Current <sup>(2)</sup>	32 bit	$I_{CC32}$ Cycle time = min 100% duty $I_{IO}=0mA$				
		$CS=V_{IL}$ $V_{IN}=V_{IH}$ or $V_{IL}$	-	-	240	mA
	16 bit	$I_{CC16}$ As above.	-	-	125	mA
	8 bit	$I_{CC8}$ As above.	-	-	65	mA
Standby Supply Current	(TTL)	$I_{SB}$ $\overline{CS}^{(1)}=V_{IH}$ , $V_{IN}=V_{IL}$ or $V_{IH}$	-	-	6	mA
	-L Version (CMOS)	$I_{SB1}$ $\overline{CS}\geq V_{CC}-0.2V$ , Other inputs = $0\sim V_{CC}$	-	-	500	$\mu A$
Output Voltage Low	$V_{OL}$	$I_{OL}=2.1mA$ , $V_{CC}=\text{Min}$	-	-	0.4	V
Output Voltage High	$V_{OH}$	$I_{OH}=-1.0mA$ , $V_{CC}=\text{Min}$	2.2	-	-	V

Notes: (1)  $\overline{CS}1\sim 4$  or  $\overline{CS}5\sim 8$  inputs operate simultaneously for 32 bit mode.

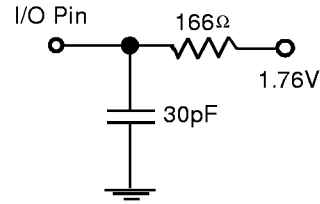
**Capacitance** ( $V_{CC}=5V$ ,  $T_A=25^\circ C$ ,  $F=1MHz$ )

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance Address, $\overline{OE}$ , $\overline{WE}$	$C_{IN1}$	$V_{IN}=0V$	-	-	64	pF
Output Capacitance 8-bit mode (worst case)	$C_{IO}$	$V_{IO}=0V$	-	-	80	pF

Note: These parameters are calculated, not measured.

**AC Test Conditions** **Output Load**

- \*Input pulse levels: 0.4V to 2.2V
- \*Input rise and fall times: 5 ns
- \*Input and Output timing reference levels: 1.5V
- \* $V_{cc} = 5V \pm 10\%$
- \*PUMA module is tested in 32 bit mode.



**Operation Truth Table**

Below is the truth table which applies to each individual SRAM on the module. When operating the module care should be taken to prevent any two SRAM components which are connected to the same data byte from driving the bus simultaneously. This will prevent bus contention occurring on the module. Please refer to the block diagram on the front page of this datasheet.

<i>Mode</i>	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$V_{cc}$ Current	<i>I/O Pin</i>	<i>Reference Cycle</i>
Not Selected	1	X	X	$I_{SB1}, I_{SB2}$	High Z	Power Down
Output Disable	0	1	1	$I_{CC1}$	High Z	
Read	0	0	1	$I_{CC1}$	$D_{OUT}$	Read Cycle
Write	0	X	0	$I_{CC1}$	$D_{IN}$	Write Cycle

1 =  $V_{IH}$ ,      0 =  $V_{IL}$ ,      X = Don't Care

**Low  $V_{cc}$  Data Retention Characteristics - L version only**

<i>Parameter</i>	<i>Symbol</i>	<i>Test Condition</i>	<i>min</i>	<i>typ</i>	<i>max</i>	<i>Unit</i>
$V_{cc}$ for Data Retention	$V_{DR}$	$\overline{CS} = V_{cc} - 0.2V$	2.0	-	-	V
Data Retention Current	$I_{CCDR1}^{(1)}$	$V_{cc} = 3.0V, \overline{CS} > V_{cc} - 0.2V, V_{IN} > 0V$	-	-	0.6	mA
Data Retention Time	$t_{CDR}$	See Retention Waveform	0	-	-	ns
Operation Recovery Time	$t_R$	See Retention Waveform	5	-	-	ms

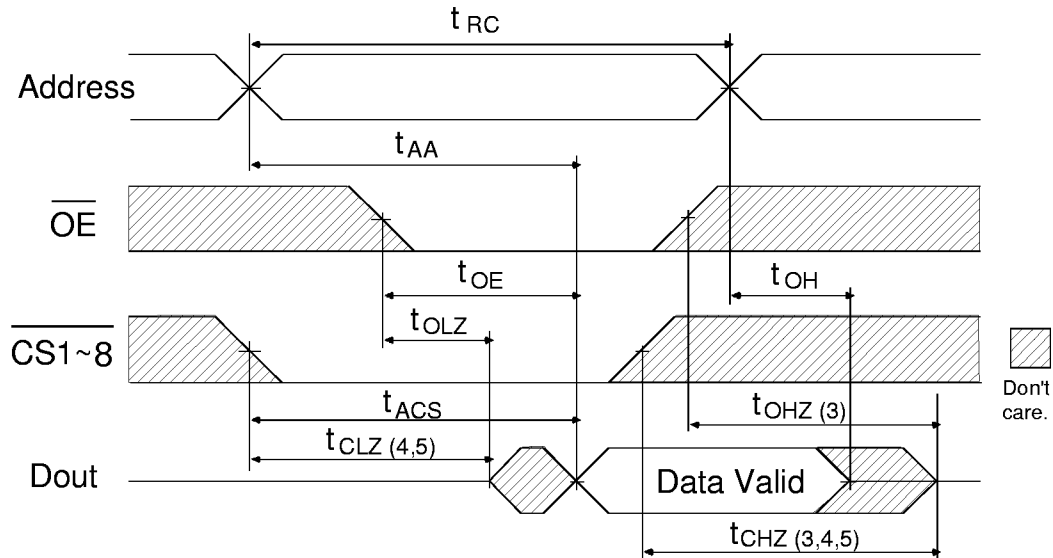
**AC OPERATING CONDITIONS****Read Cycle**

<i>Parameter</i>	<i>Symbol</i>	70		85		10		<i>Units</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Read Cycle Time	$t_{RC}$	70	-	85	-	100	-	ns
Address Access Time	$t_{AA}$	-	70	-	85	-	100	ns
Chip Select Access Time	$t_{ACS}$	-	70	-	85	-	100	ns
Output Enable to Output Valid	$t_{OE}$	-	35	-	45	-	50	ns
Output Hold from Address Change	$t_{OH}$	10	-	10	-	15	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	5	-	5	-	5	-	ns
Output Disable to Output in High Z	$t_{OHZ}$	0	25	0	25	0	30	ns
Chip Disable to Output in High Z	$t_{CHZ}$	0	25	0	25	0	30	ns
Chip Enable to Output in Low Z	$t_{CLZ}$	10	0	10	0	10	0	ns

**Write Cycle**

<i>Parameter</i>	<i>Symbol</i>	70		85		10		<i>Units</i>
		<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	<i>min</i>	<i>max</i>	
Write Cycle Time	$t_{WC}$	70	-	85	-	100	-	ns
Chip Selection to End of Write	$t_{CW}$	60	-	70	-	80	-	ns
Address Valid to End of Write	$t_{AW}$	60	-	70	-	80	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	50	-	60	-	70	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	30	-	35	-	40	-	ns
Output Active from End of Write	$t_{OW}$	3	-	3	-	3	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Write to Output High Z	$t_{WHZ}$	0	25	0	25	0	30	ns

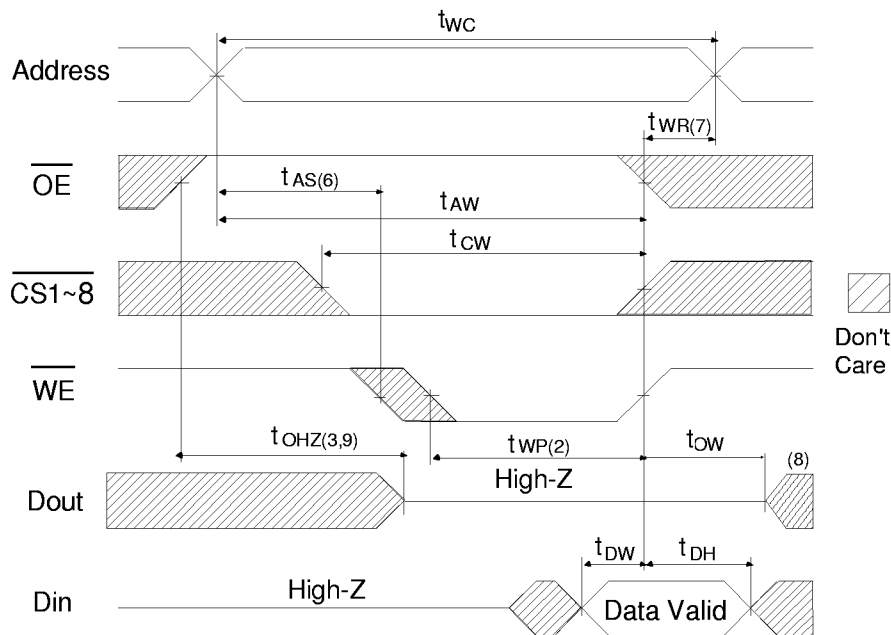
**Read Cycle Timing Waveform<sup>(1,2)</sup>**



**AC Read Characteristics Notes**

- (1)  $\overline{WE}$  is High for Read Cycle.
- (2) All read cycle timing is referenced from the last valid address to the first transition address.
- (3)  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.
- (4) At any given temperature and voltage condition,  $t_{CHZ}$  (max) is less than  $t_{CLZ}$  (min) both for a given module and from module to module.
- (5) These parameters are sampled and not 100% tested.

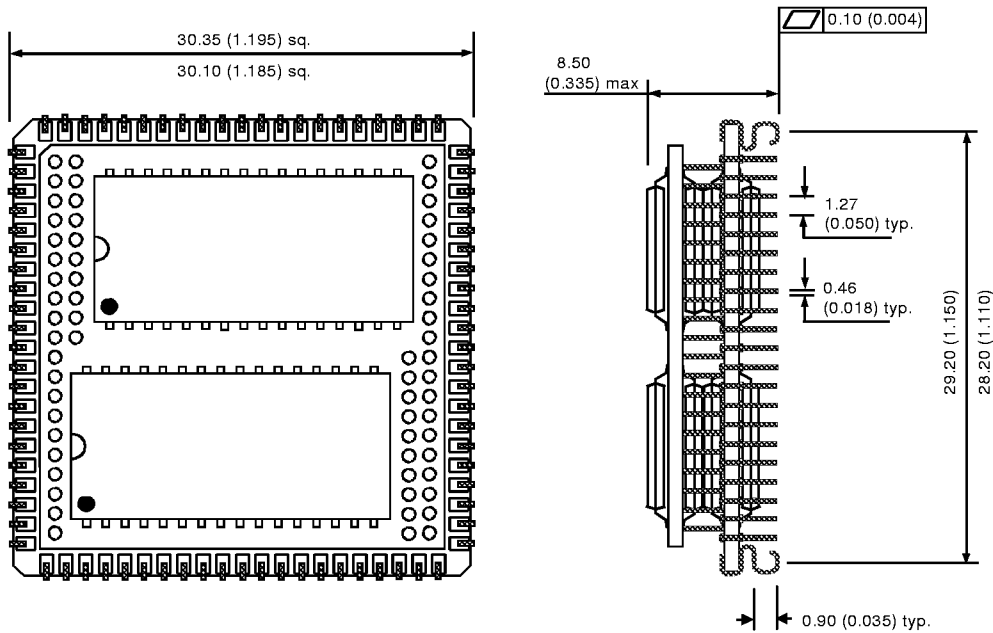
**Write Cycle No.1 Timing Waveform<sup>(1,4)</sup>**





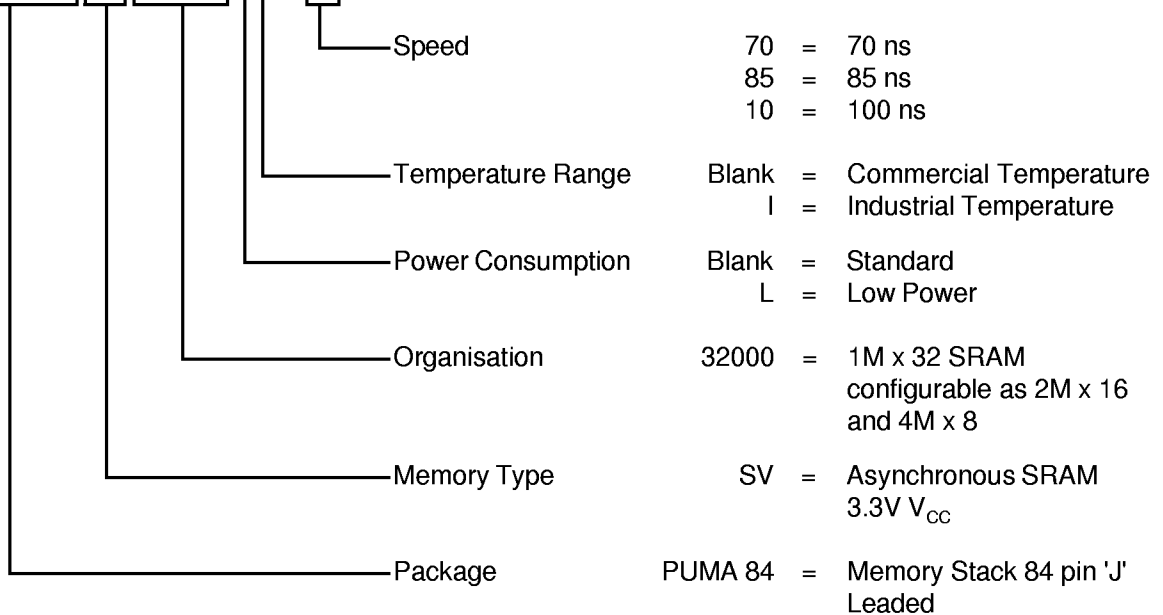
**Package Information**      Dimensions in mm(inches)

**Plastic 84 Pin JEDEC Surface mount PLCC**



**Ordering Information**

**PUMA 84SV32000LI - 70**



**Note :**

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