

**Document Title**

**256Kx36 & 512Kx18-Bit Pipelined NtRAM™**

**Revision History**

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	September. 1997	Preliminary
0.1	1. Changed speed bin from 167MHz to 150MHz 2. Changed DC Parameters; Icc : from 400mA to 450mA ISB : from 60mA to 20mA ISB2 : from 50mA to 85mA	November. 1997	Preliminary
0.2	1. Changed speed bin from 150MHz to 167MHz 2. Changed Power from 3.3V to 2.5V 3. Changed N.C pins to Power and ZZ Pin #14, #16, #64, #66 4. Changed some control pin names. <u>      </u> from CEN to CKE, from BWEx to BWx 5. Modify absolute maximum ratings VDD ; from 4.0V to 3.6V, VIN ; from 4.6V to 3.6V 6. Changed DC parameters ISB ; from 20mA to 80mA, ISB2 ; from 85mA to 10mA VOL ; from 0.4V to 0.2V, VOH ; from 2.4V to 2.0V VIL ; from 0.8V to 0.7V, VIH ; from 2.0V to 1.7V 7. Add the sleep mode timing and characteristics CKE controlled timing and CS controlled timing	March. 11. 1998	Preliminary
0.3	1. Removed speed bin 167MHz 2.Changed AC parameters tHZOE ; from 4.0 to 3.5 , tHZC;from 4.0 to 3.5 for 133MHz tHZOE ; from 5.0 to 3.5 , tHZC;from 5.0 to 3.5 , tCL/H; 4.0 to 3.0 for 100MHz 3.Modify Sleep Mode Waveform. Changed Sleep Mode Electrical Characteristics . tPDS ;from MAX 2cycle to MIN 2cycle tPUS ; from MAX 2cycle to MIN 2cycle	April. 11. 1998	Preliminary
0.4	Modify from <u>ADV</u> to ADV at timing. Add the Trade Mark( NtRAM™)	June. 02. 1998	Preliminary
0.5	1. Changed DC parameters ISB1; from 10mA to 20mA, ISB2 ; from 10mA to 20mA	Aug. 19. 1998	Preliminary

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



**256Kx36 & 512Kx18-Bit Pipelined NtRAM™**

**FEATURES**

- 2.5V ±5% Power Supply.
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A Package.

**GENERAL DESCRIPTION**

The KM736S849 and KM718S949 are 9,437,184 bits Synchronous Static SRAMs.

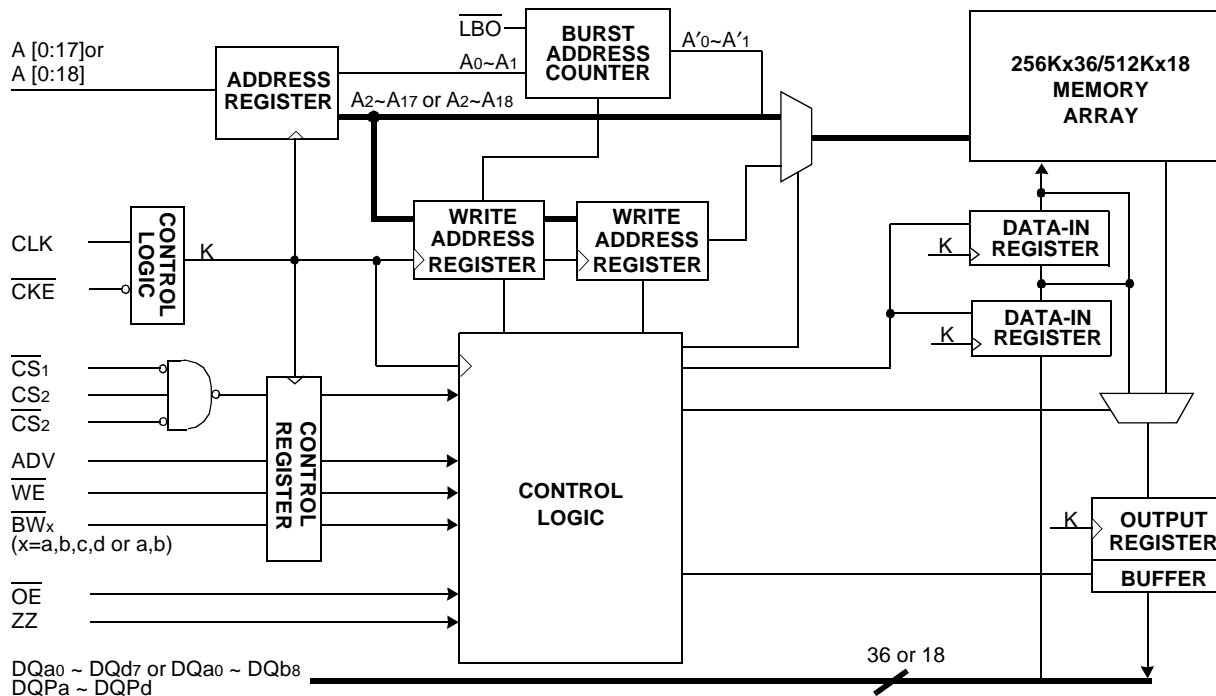
The NtRAM™, or No Turnaround Random Access Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, pipelined SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The KM736S849 and KM718S949 are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP packages. Multiple power and ground pins minimize ground bounce.

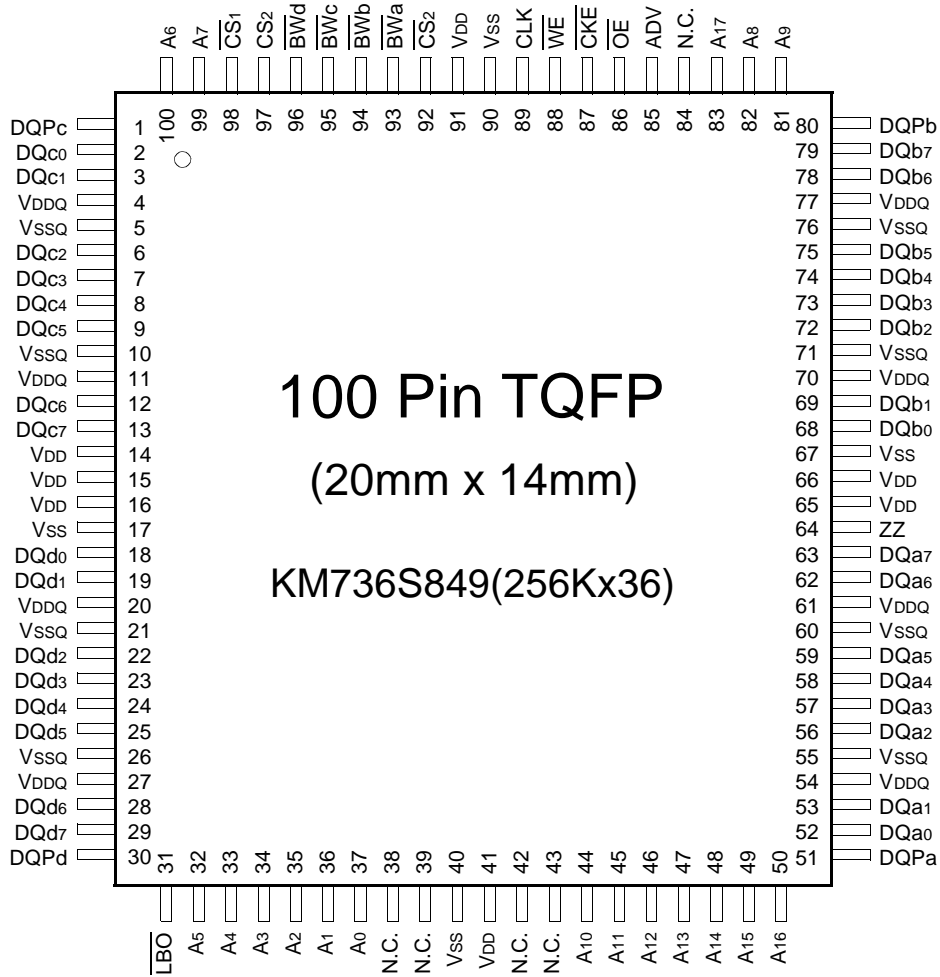
**FAST ACCESS TIMES**

Parameter	Symbol	-67	-75	-10	Unit
Cycle Time	tCYC	6.7	7.5	10	ns
Clock Access Time	tCD	3.8	4.0	5.0	ns
Output Enable Access Time	tOE	3.8	4.0	5.0	ns

**LOGIC BLOCK DIAGRAM**



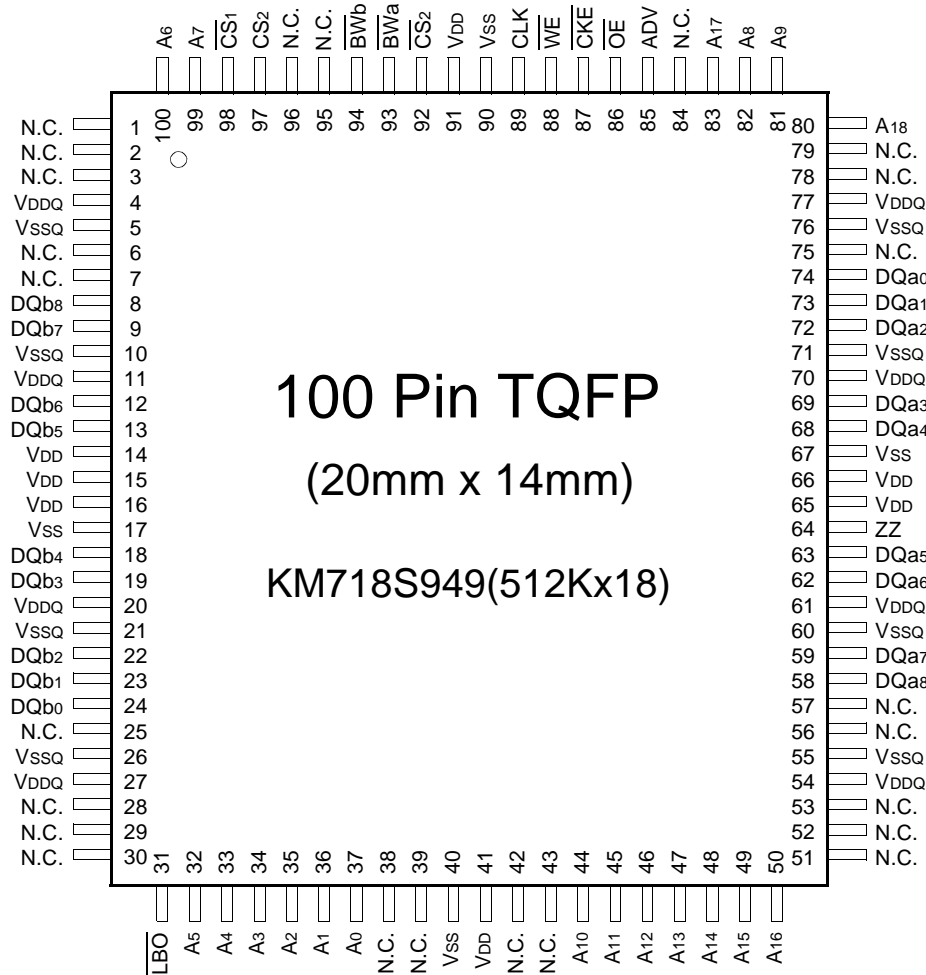
**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 50,81,82,83,99,100	VDD	Power Supply(+2.5V)	14,15,16,41,65,66,91
ADV	Address Advance/Load	85	VSS	Ground	17,40,67,90
WE	Read/Write Control Input	88	N.C.	No Connect	38,39,42,43,84
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CKE	Clock Enable	87	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
BWx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,83,99,100	VDD	Power Supply(+2.5V)	14,15,16,41,65,66,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,25,28,29,30,38,39,42,43,51,52,53,56,57,75,78,79,84,95,96
ADV	Address Advance/Load	85			
WE	Read/Write Control Input	88			
CLK	Clock	89			
CKE	Clock Enable	87	DQa0~a8	Data Inputs/Outputs	8,9,12,13,18,19,22,23,24
CS1	Chip Select	98	DQb0~b8		58,59,62,63,68,69,72,73,74
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx	Byte Write Inputs	93,94	VDDQ	Output Power Supply (+2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

**FUNCTION DESCRIPTION**

The KM736S849 and KM718S949 are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of OE, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(CKE) pin allows the operation of the chip to be suspended as long as necessary. All synchronous inputs are ignored when CKE is high and the internal device registers will hold their previous values.

When CKE is active asserted, ADV is disasserted and all three chip enables(CS1, CS2, CS2) are asserted, NtRAM™ latches external address and initiates a cycle.

Output Enable(OE) can be used to disable the output at any given time.

Read operation is initiated when the following conditions are satisfied at the rising edge of clock, CKE is asserted Low, all three chip enables(CS1, CS2, CS2) are active, the write enable input signals WE is deasserted high, and ADV is asserted Low. The address presented to the address inputs are latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data a propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within provided OE is active Low.

Write operation occurs when WE is sampled Low at the rising edge of clock. BW[d:a] can be used for byte write operation. The Pipelined NtRAM™ uses a late-late write cycle to utilize 100% of the bandwidth.

At the first rising edge of clock, WE and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected.

And this pin is High, Interleaved burst sequence is selected.

During normal operation, ZZ must be pulled LOW. When ZZ is pulled HIGH, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to LOW, the SRAM normally operates after 2 cycles of wake up time.

**BURST SEQUENCE TABLE**

(Interleaved Burst, LBO=High)

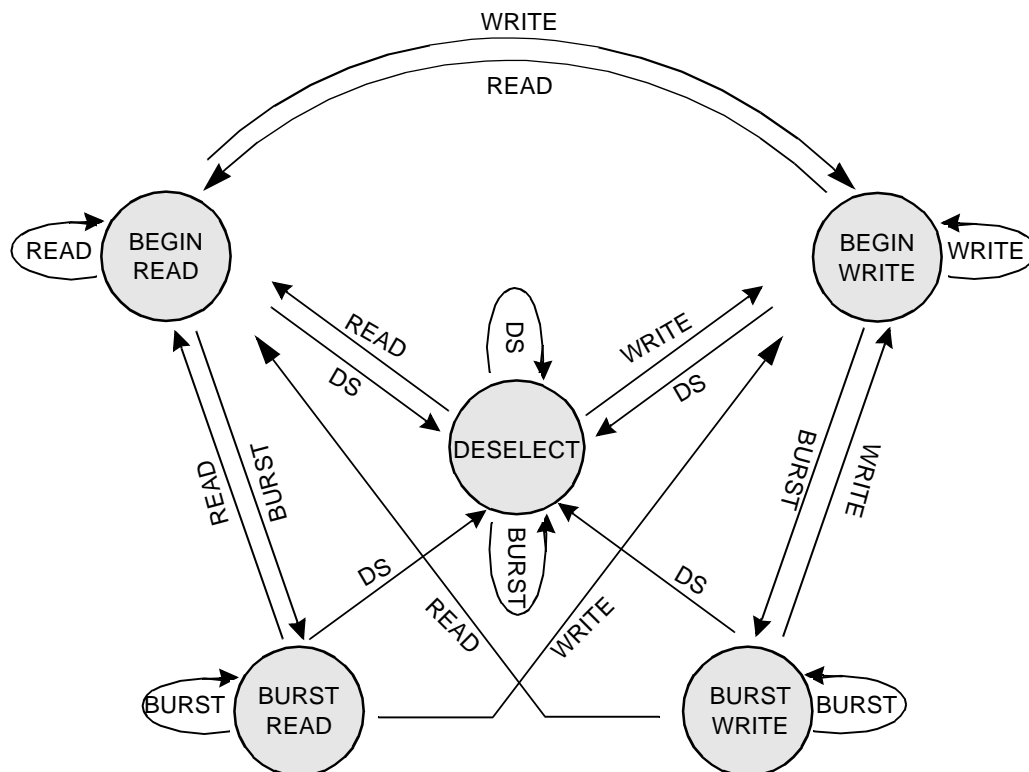
LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, LBO=Low)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

**NOTE** : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

NOTE

1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because  $\overline{\text{CKE}}$  HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK)

**TRUTH TABLES**

**SYNCHRONOUS TRUTH TABLE**

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	ADV	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CKE}$	CLK	Address Accessed	Operation
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- NOTE :** 1. X means "Don't Care".      2. The rising edge of clock is symbolized by (↑).  
 3. A continue deselect cycle can only be entered if a deselect cycle is executed first.  
 4.  $\overline{WRITE} = L$  means Write operation in WRITE TRUTH TABLE.  
 $\overline{WRITE} = H$  means Read operation in WRITE TRUTH TABLE.  
 5. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{OE}$ ).

**WRITE TRUTH TABLE(x36)**

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	$\overline{BW}_c$	$\overline{BW}_d$	Operation
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	WRITE ABORT/NOP

**WRITE TRUTH TABLE(x18)**

$\overline{WE}$	$\overline{BW}_a$	$\overline{BW}_b$	Operation
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTEs
L	H	H	WRITE ABORT/NOP

- NOTE :** 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**ASYNCHRONOUS TRUTH TABLE**

(See Notes 1 and 2):

Operation	ZZ	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**NOTE**

1. X means "Don't Care".
2. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Rating	Unit
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.3 to 3.6	V
Voltage on Any Other Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to 3.6	V
Power Dissipation	P <sub>D</sub>	1.4	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>OPR</sub>	0 to 70	°C
Storage Temperature Range Under Bias	T <sub>BIAS</sub>	-10 to 85	°C

\*NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS**(0°C ≤ T<sub>A</sub> ≤ 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>DD</sub>	2.375	2.5	2.625	V
	V <sub>DDQ</sub>	2.375	2.5	2.625	V
Ground	V <sub>SS</sub>	0	0	0	V

\*NOTE : V<sub>DD</sub> and V<sub>DDQ</sub> must be supplied with identical voltage levels.

**CAPACITANCE\***(T<sub>A</sub>=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	8	pF

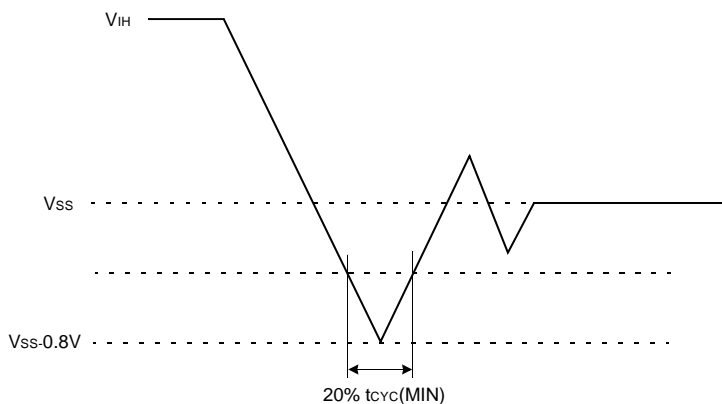
\*NOTE : Sampled not 100% tested.



**DC ELECTRICAL CHARACTERISTICS**(V<sub>DD</sub>=2.5V ±5%, T<sub>A</sub>=0°C to +70°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	I <sub>IL</sub>	V <sub>DD</sub> =Max ; V <sub>IN</sub> =V <sub>SS</sub> to V <sub>DD</sub>	-2	+2	μA
Output Leakage Current	I <sub>OL</sub>	Output Disabled,	-2	+2	μA
Operating Current	I <sub>CC</sub>	V <sub>DD</sub> =Max I <sub>OUT</sub> =0mA Cycle Time ≥ t <sub>CYC</sub> Min	-67	420	mA
			-75	370	
			-10	300	
Standby Current	I <sub>SB</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≤V <sub>IL</sub> , f=Max, All Inputs≤0.2V or ≥ V <sub>DD</sub> -0.2V	-67	70	mA
			-75	60	
			-10	50	
	I <sub>SB1</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V <sub>DD</sub> -0.2V or 0.2V)	-	20	mA
I <sub>SB2</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≥V <sub>DD</sub> -0.2V, f=Max, All Inputs≤V <sub>IL</sub> or ≥V <sub>IH</sub>	-	20	mA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =1.0mA	-	0.2	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.0	-	V
Input Low Voltage	V <sub>IL</sub>		-0.3*	0.7	V
Input High Voltage	V <sub>IH</sub>		1.7	V <sub>DD</sub> +0.3**	V

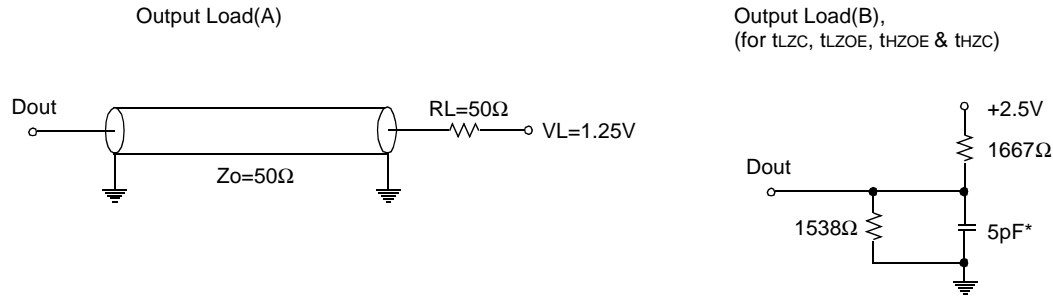
\*\* In Case of I/O Pins, the Max. V<sub>IH</sub>=V<sub>DDQ</sub>+0.3V



**TEST CONDITIONS**

(T<sub>A</sub>=0 to 70°C, V<sub>DD</sub>=2.5V ±5%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80%)	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Fig. 1



\* Including Scope and Jig Capacitance

Fig. 1

**AC TIMING CHARACTERISTICS**  
(VDD=2.5V ±5%, TA=0 to 70°C)

Parameter	Symbol	-67		-75		-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	tCYC	6.7	-	7.5	-	10.0	-	ns
Clock Access Time	tCD	-	3.8	-	4.0	-	5.0	ns
Output Enable to Data Valid	tOE	-	3.8	-	4.0	-	5.0	ns
Clock High to Output Low-Z	tLZC	1.5	-	1.5	-	1.5	-	ns
Output Hold from Clock High	tOH	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.0	-	3.5	-	3.5	ns
Clock High to Output High-Z	tHZC	-	3.0	-	3.5	-	3.5	ns
Clock High Pulse Width	tCH	2.5	-	3.0	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.5	-	3.0	-	3.0	-	ns
Address Setup to Clock High	tAS	1.5	-	1.5	-	1.5	-	ns
CKE Setup to Clock High	tCES	1.5	-	1.5	-	1.5	-	ns
Data Setup to Clock High	tDS	1.5	-	1.5	-	1.5	-	ns
Write Setup to Clock High ( $\overline{WE}$ , $\overline{BWX}$ )	tWS	1.5	-	1.5	-	1.5	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	1.5	-	1.5	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	1.5	-	1.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
CKE Hold from Clock High	tCEH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ( $\overline{WE}$ , $\overline{BWE}$ )	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

- NOTE :**
- All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  - Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
  - A write cycle is defined by WE low having been registered into the device at ADV Low, A Read cycle is defined by WE High with ADV Low, Both cases must meet setup and hold times.
  - To avoid bus contention, At a given voltage and temperature tCLZ is more than tHZC.  
The specs as shown do not imply bus contention because tCLZ is a Min. parameter that is worst case at totally different test conditions (0°C,2.625V) than tCHZ, which is a Max. parameter(worst case at 70°C,2.375V)  
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
  - ADV must not be asserted for at least 2 Clocks after leaving ZZ state.

**SLEEP MODE**

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

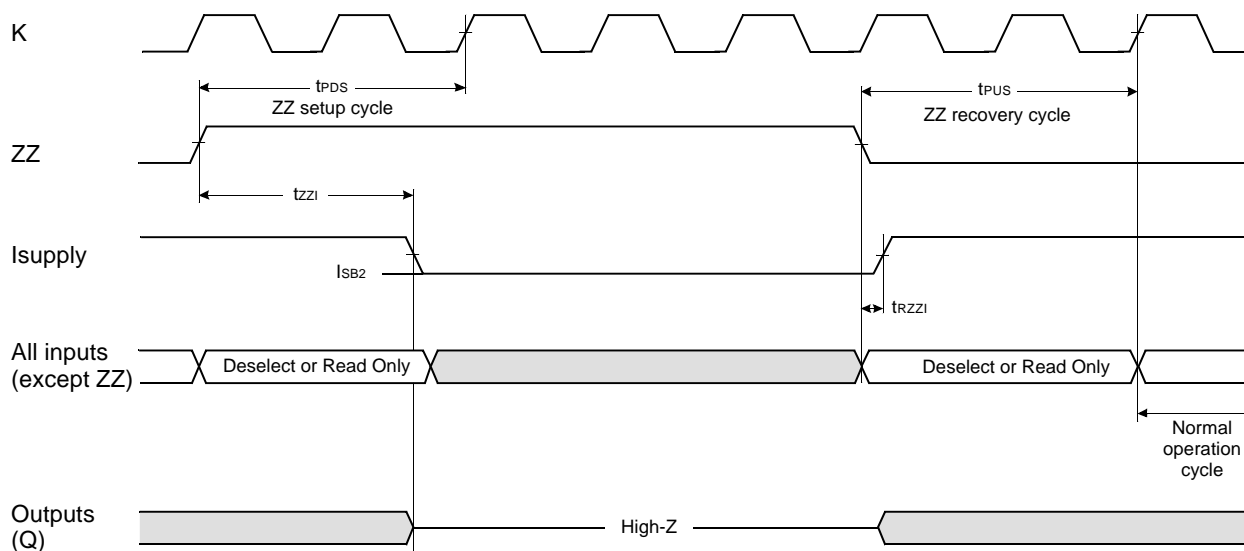
When the ZZ pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZI}$  is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during  $t_{PUS}$ , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

**SLEEP MODE ELECTRICAL CHARACTERISTICS**

( $V_{DD}, V_{DDQ} = 2.5V \pm 5\%$ )

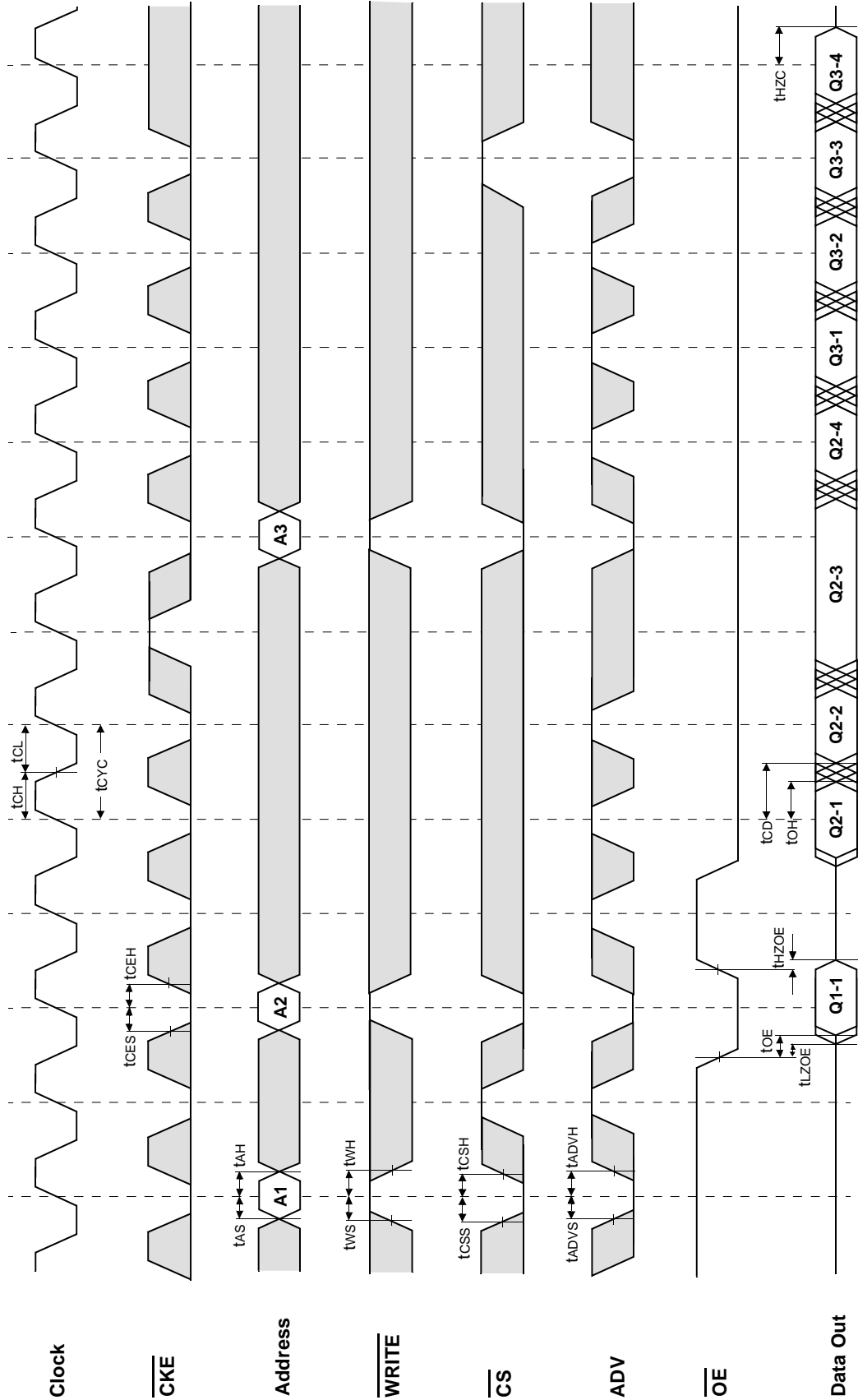
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	$I_{SB2}$		10	mA
ZZ active to input ignored		$t_{PDS}$	2		cycle
ZZ inactive to input sampled		$t_{PUS}$	2		cycle
ZZ active to SLEEP current		$t_{ZZI}$		2	cycle
ZZ inactive to exit SLEEP current		$t_{RZZI}$	0		

**SLEEP MODE WAVEFORM**



□ DON'T CARE

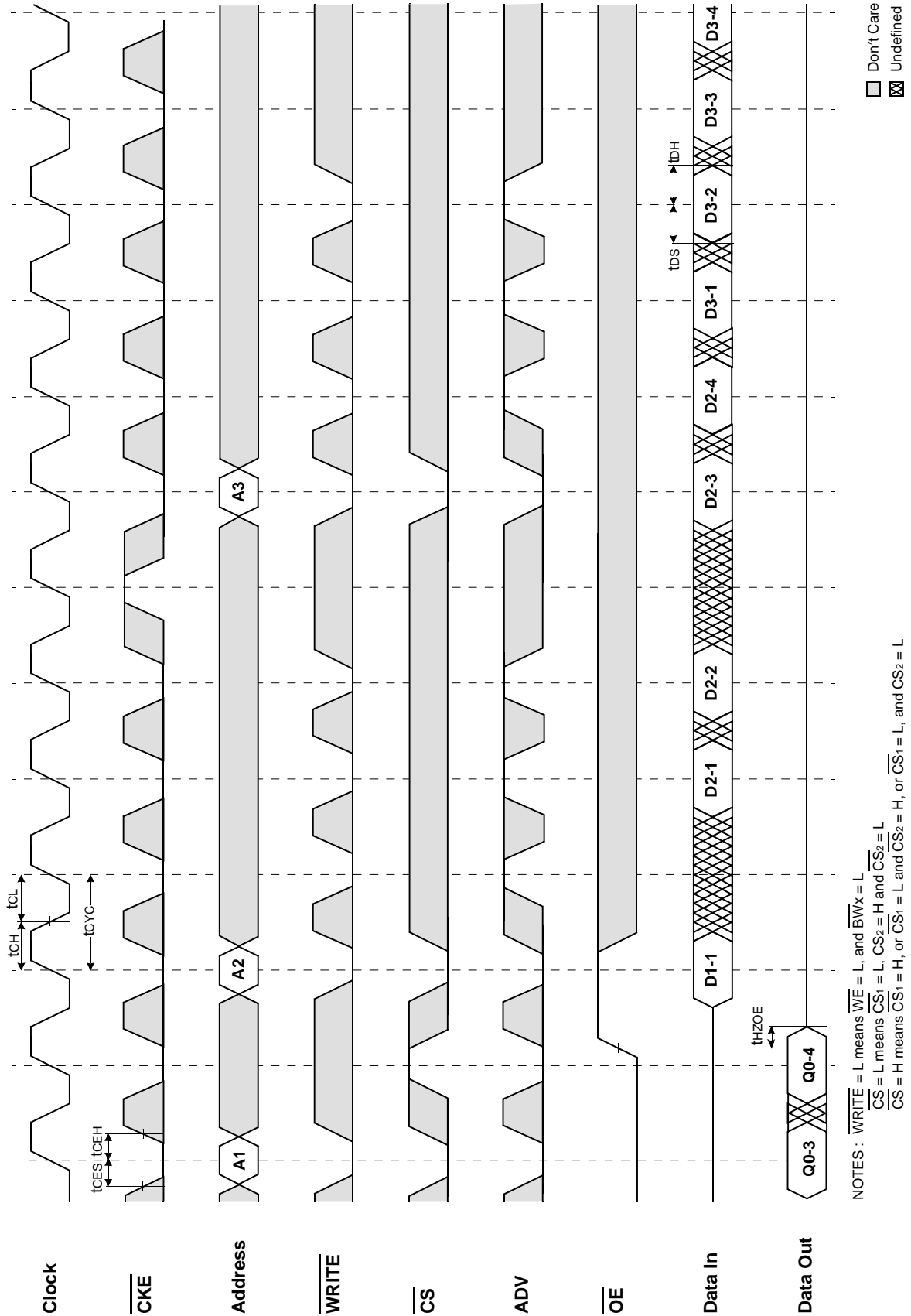
**TIMING WAVEFORM OF READ CYCLE**



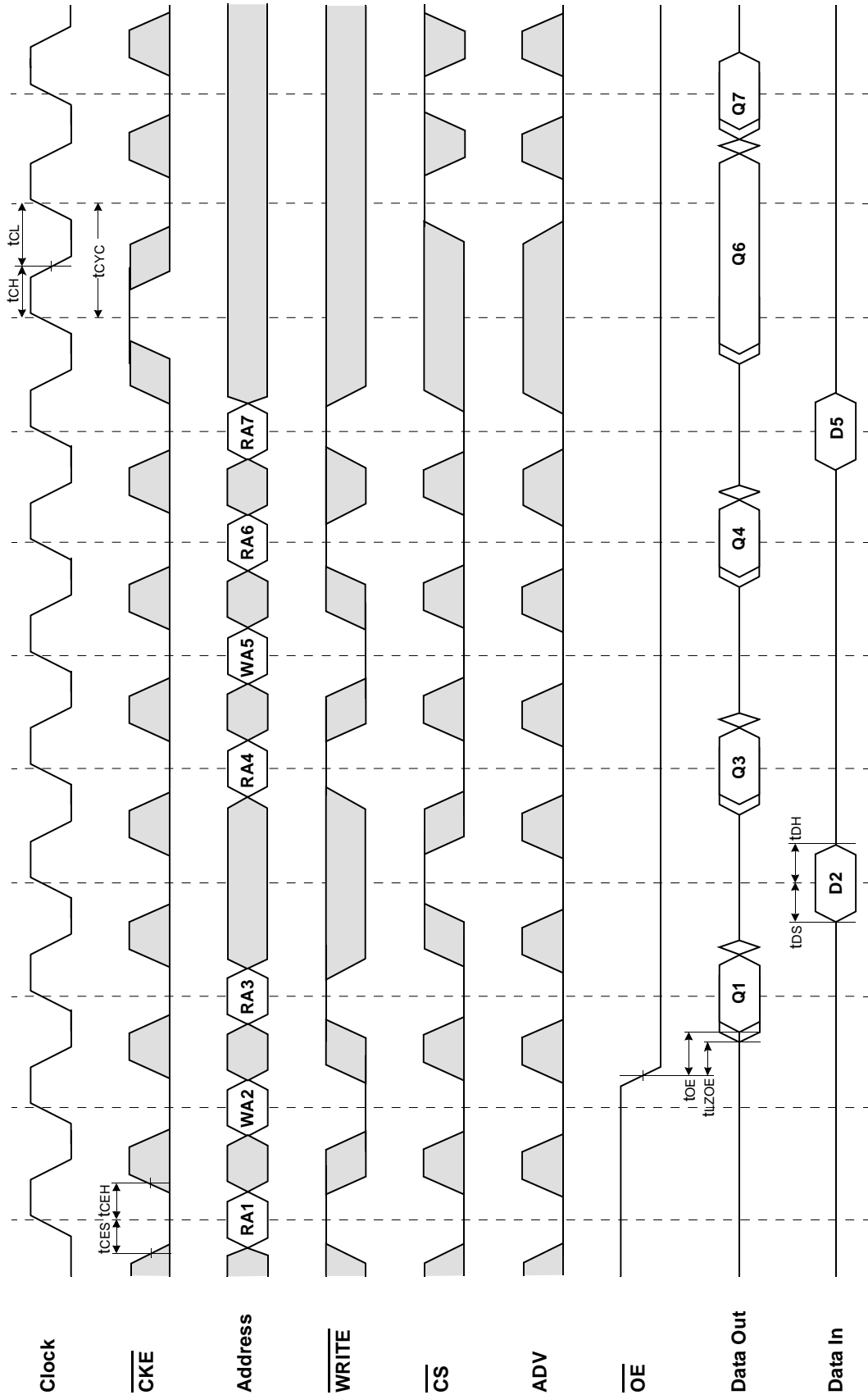
□ Don't Care  
▣ Undefined

NOTES:  $\overline{WRITE} = L$  means  $\overline{WE} = L$ , and  $\overline{BWx} = L$   
 $\overline{CS} = L$  means  $\overline{CS1} = L$ ,  $\overline{CS2} = H$  and  $\overline{CS2} = L$   
 $\overline{CS} = H$  means  $\overline{CS1} = H$ , or  $\overline{CS1} = L$  and  $\overline{CS2} = H$ , or  $\overline{CS1} = L$ , and  $\overline{CS2} = L$

**TIMING WAVEFORM OF WRTE CYCLE**



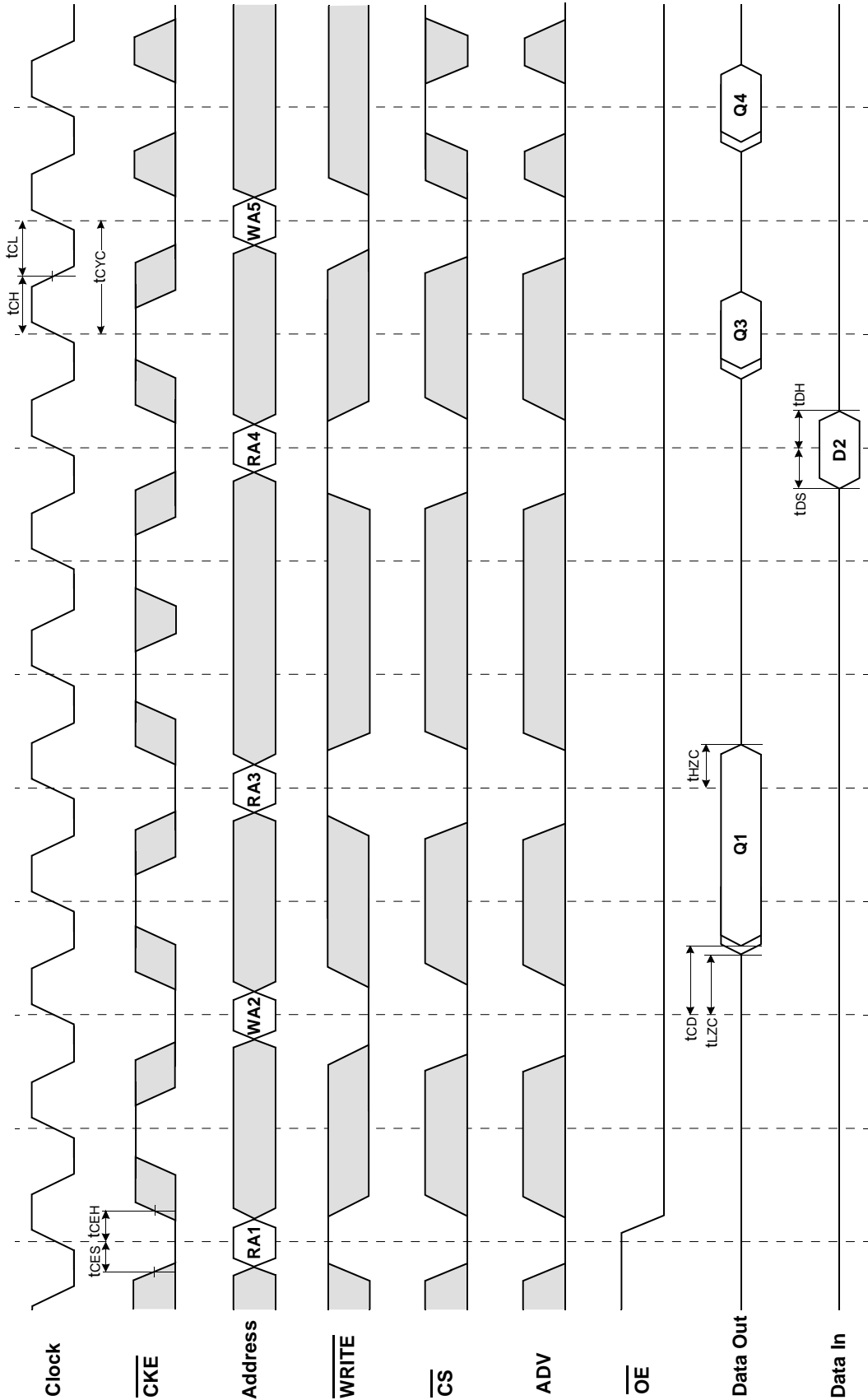
**TIMING WAVEFORM OF SINGLE READWRITE**



□ Don't Care  
⊗ Undefined

NOTES:  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BW}}_x = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\overline{\text{CS}}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\overline{\text{CS}}_2 = \text{L}$

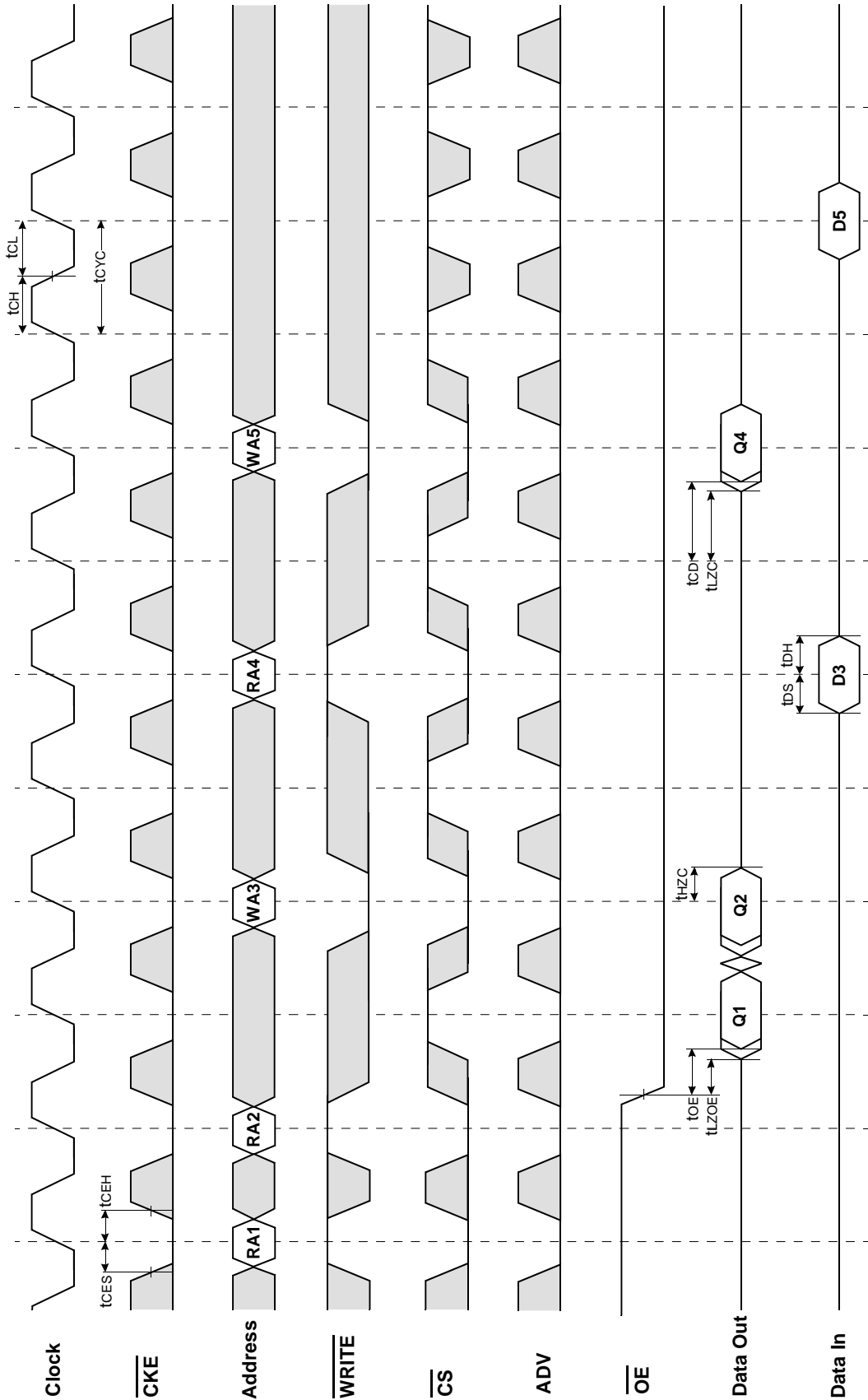
**TIMING WAVEFORM OF  $\overline{\text{CKE}}$  OPERATION**



□ Don't Care  
☒ Undefined

NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BWx}} = \text{L}$   
 $\text{CS} = \text{L}$  means  $\text{CS}_1 = \text{L}$ ,  $\text{CS}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\text{CS} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\text{CS}_2 = \text{L}$

**TIMING WAVEFORM OF CS OPERATION**



□ Don't Care  
☒ Undefined

NOTES: WRITE = L means WE = L, and BWx = L  
CS = L means CS<sub>1</sub> = L, CS<sub>2</sub> = H and CS<sub>2</sub> = L  
CS = H means CS<sub>1</sub> = H, or CS<sub>1</sub> = L and CS<sub>2</sub> = H, or CS<sub>1</sub> = L, and CS<sub>2</sub> = L



**PACKAGE DIMENSIONS**

