HM62832/HM62832H
8-Bit CMOS Static RAM

T-46-23-14

32768-WORD × 8-BIT HIGH SPEED CMOS STATIC RAM

■ FEATURES

- High speed: Fast Access time 25/35/45 ns (max.)

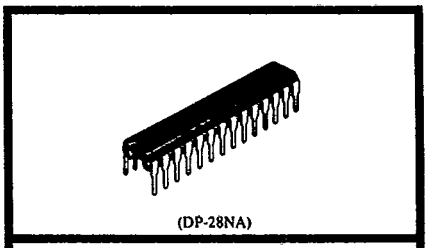
HM62832—Low power
Standby: 10 μW (typical) (L-version)
Active: 300 mW (typical)

HM62832H—Low power
Standby: 300 mW (typical)
Active: 30 μW (typical) (L-version)

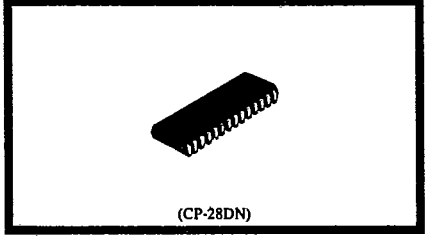
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three stage output
- Directly TTL compatible—All inputs and outputs

■ ORDERING INFORMATION

Part No.	Access	Package
HM62832P-35	35 ns	300 mil 28-pin Plastic DIP
HM62832P-45	45 ns	
HM62832LP-35	35 ns	
HM62832LP-45	45 ns	
HM62832JP-35	35 ns	300 mil 28-pin Plastic SOJ
HM62832JP-45	45 ns	
HM62832LJP-35	35 ns	
HM62832LJP-45	45 ns	
HM62832HP-25	25 ns	300 mil 28-pin Plastic DIP (DP-28NA)
HM62832HP-35	35 ns	
HM62832HP-45	45 ns	
HM62832HJP-25	25 ns	300 mil 28-pin Plastic SOJ (CP-28DN)
HM62832HJP-35	35 ns	
HM62832HJP-45	45 ns	



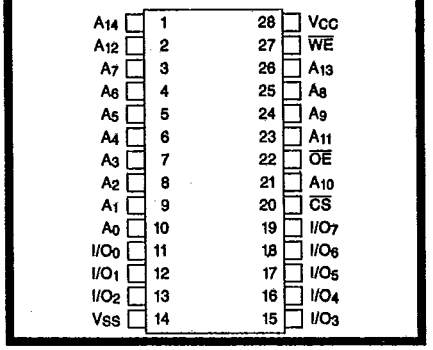
(DP-28NA)



(CP-28DN)

PIN ARRANGEMENT

Top View

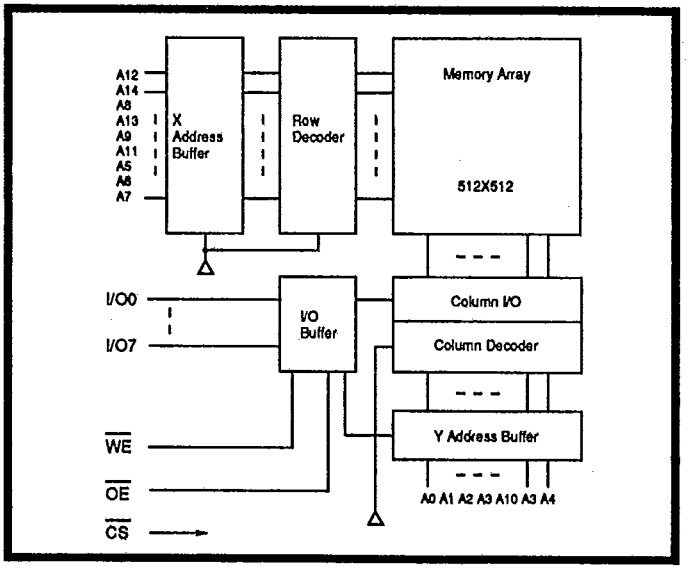


■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{14}	Address
I/O_0–I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM

T-46-23-14



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5*1 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. -2.5 V for pulse width ≤ 10 ns

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	• Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1) to (3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L		I_{CC}	D_{in}	Write Cycle(2)

NOTE: 1. X : H or L

■ DC CHARACTERISTICS for HM62832 (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) T-46-23-14

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	10	μA	V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Average Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby V_{CC} Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
	I_{SB1}	—	2	100	μA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0 V ≤ V_{in} ≤ 0.2 V, or V_{in}, ≥ V_{cc} - 0.2 V	L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = -4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ DC CHARACTERISTICS for HM62832H (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby Power Supply Current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0 V ≤ V_{in} ≤ 0.2 V, or V_{in}, ≥ V_{cc} - 0.2 V	
		—	0.006	0.1	mA		L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = -4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

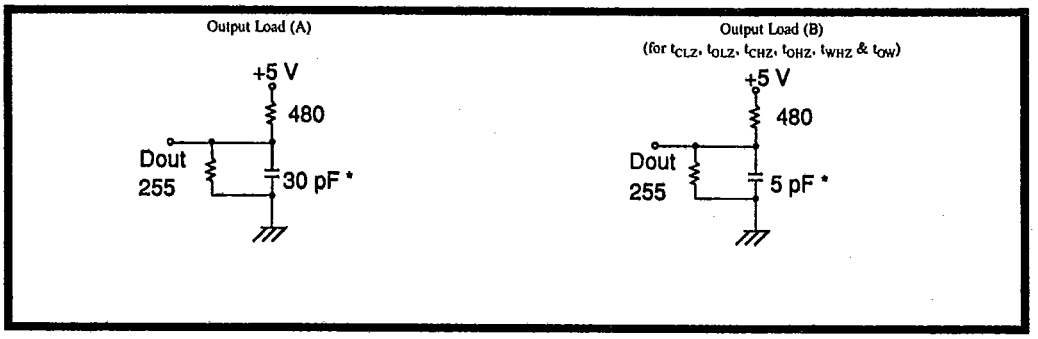
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

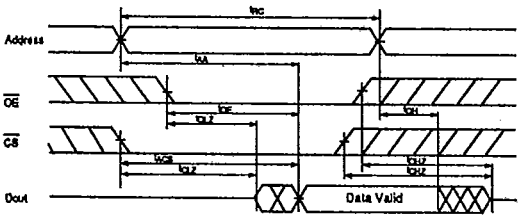


NOTE: *Including scope & jig.

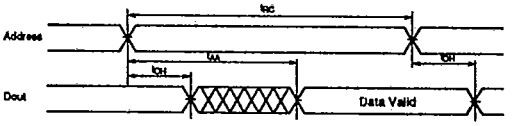
■ Read Cycle

Parameter	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	—	20	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{CLZ}	5	—	5	—	5	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}	0	12	0	15	0	15	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	15	ns

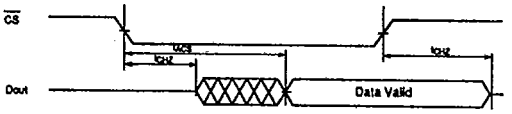
Read Cycle Timing (1) *1



Read Cycle Timing (2) *1, *2, *4



Read Cycle Timing (3) *1, *3, *4



NOTES: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

■ Write Cycle

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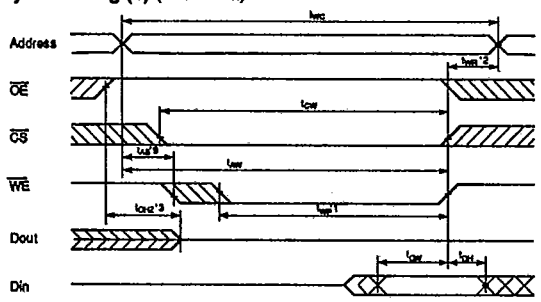
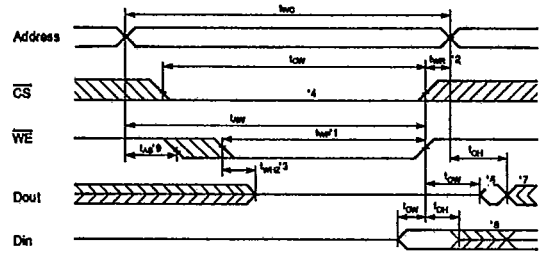
Item	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	15	—	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Write to Output in High-Z	t_{WHZ}	0	15	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	20	ns
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ Low Fixed)



NOTES:
*1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL}).
*6. D_{out} is in the same phase of written data of this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.
*9. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

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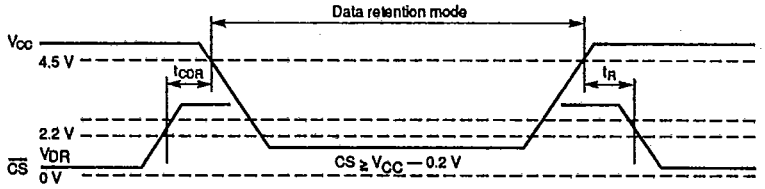
■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

This characteristics is guaranteed only for L-version

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or $0 V \leq V_{in} \leq 0.2$ V
Data Retention Current	I_{CCDR}	—	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	t_{RC}*1	—	—	ns	

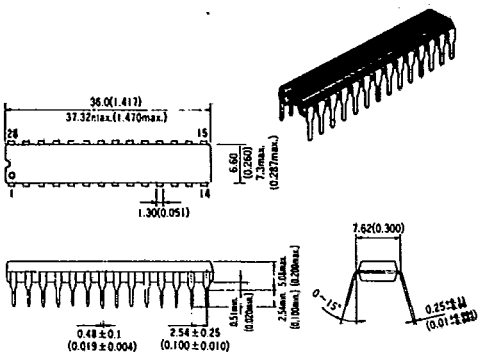
NOTES: *1. t_{RC} = read cycle time.
*2. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform

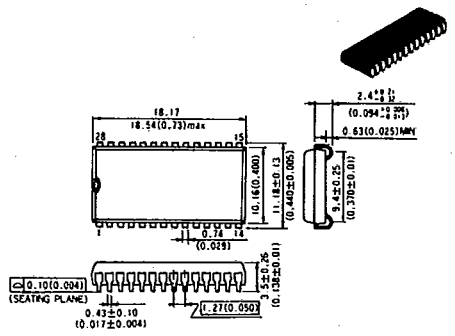


■ PACKAGE DIMENSIONS Unit: mm (inch)

HM62832HP Series
(DP-28NA)
HM62832P/HP



HM62832HJP Series
(CP-28DN)
HM62832JP/HJP



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