NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD3725D-01

5000-BIT × 3 CCD COLOR LINEAR IMAGE SENSOR

The μPD3725D-01 is a high sensitivity 5000-bit × 3 CCD (Charge Coupled Device) color image sensor which changes optical images to electrical signal and has the function of color separation. ★

The μPD3725D-01 has 3 rows of 5000-bit photocell array and 6 rows of 2500-bit charge transferred register, so it is suitable for high resolution color image scanner and degital color copier.

FEATURES

- Valid photocell : 5000-bit × 3
- Photocell's pitch : 14 μm
- Line distance : 112 μm (8 lines) R(red) bit-G(green) bit, Gbit-B(blue)bit
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7lx•Hour)
- Resolution : 16 dot/mm across the shorter side of a B4-size (257 × 364 mm) sheet
- Drive clock level : CMOS output under 5 V operation
- Data rate : 16 MHz MAX.
- High speed scan : 320 μs/line
- Power supply : +12 V

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD3725D-01	24-pin ceramic DIP (CERDIP) (600 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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The mark ★ shows revised points.

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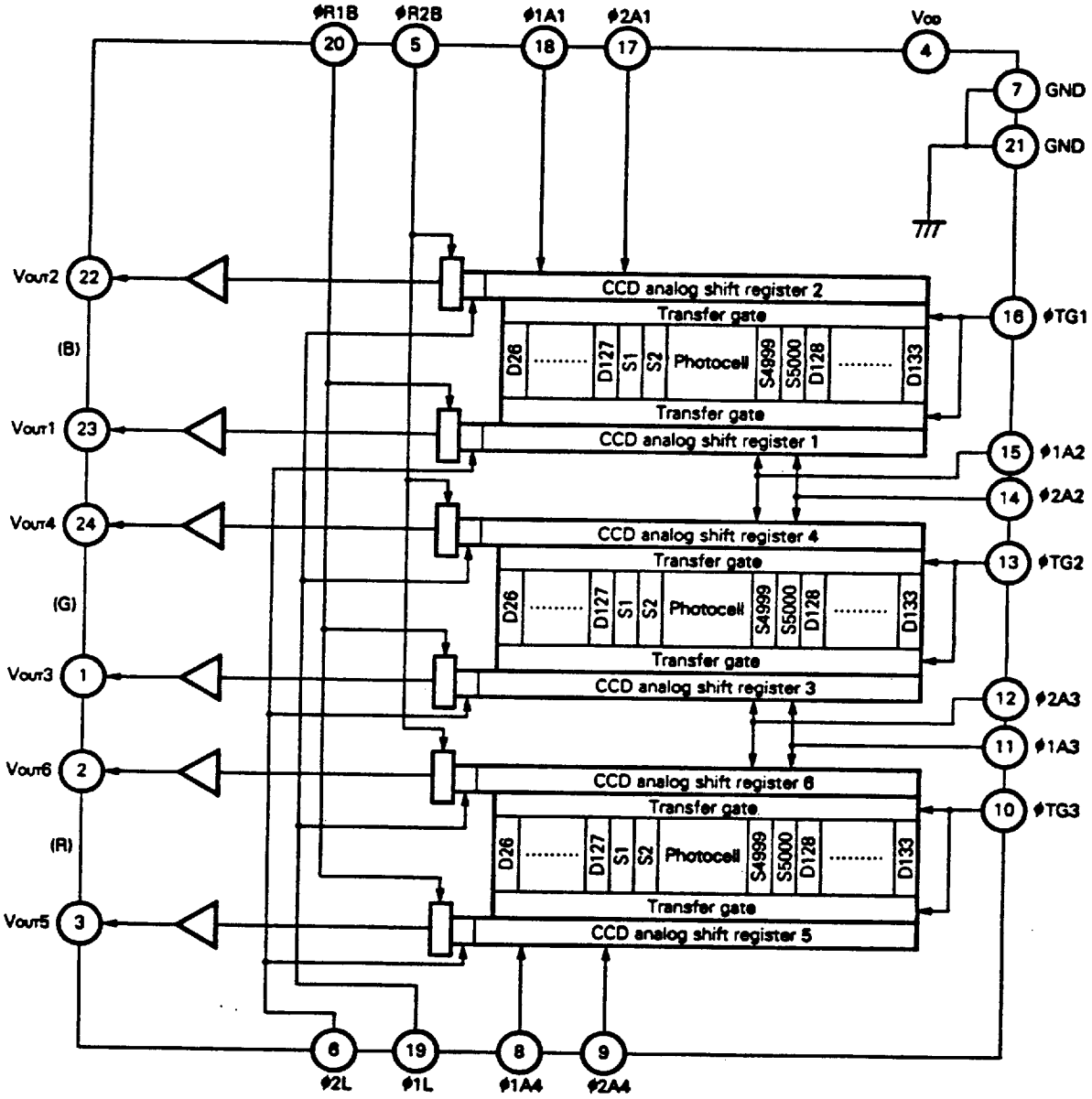
BLOCK DIAGRAM



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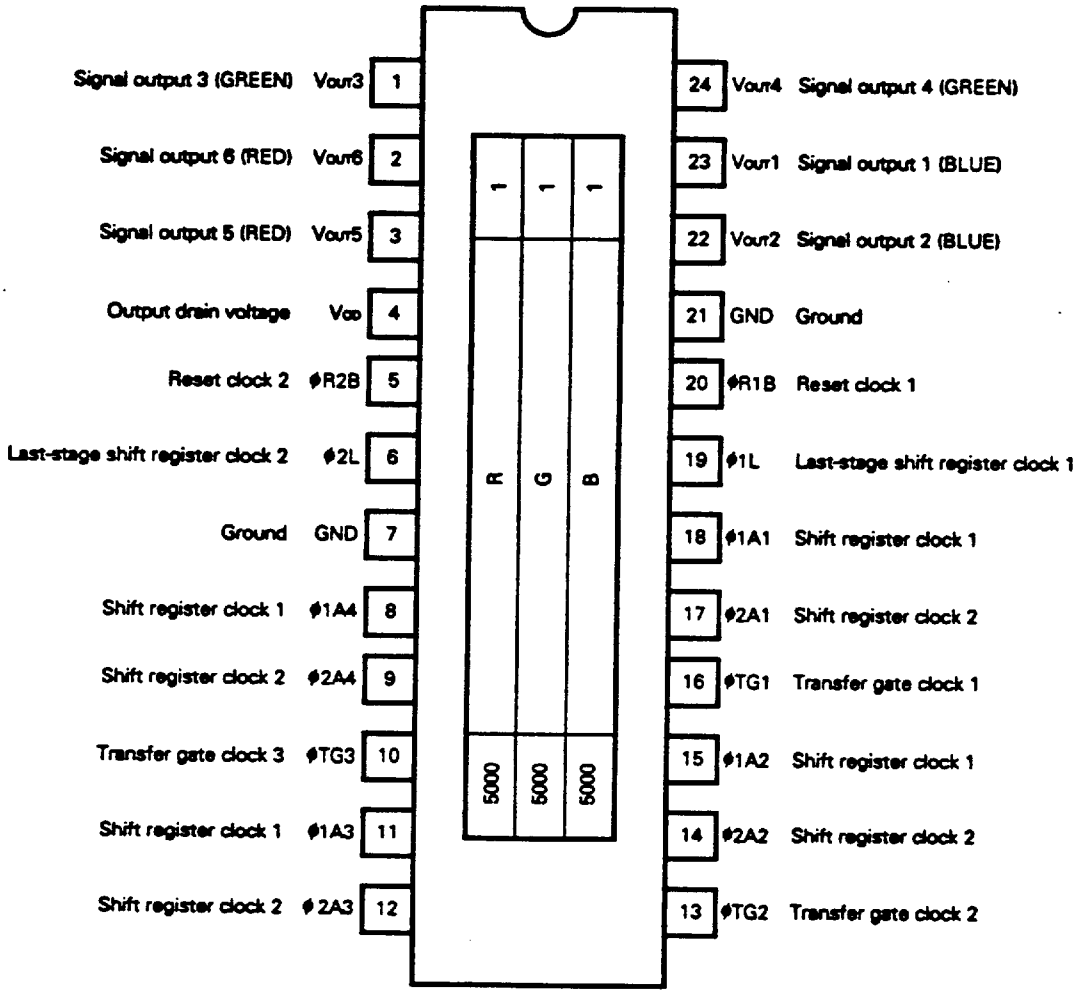
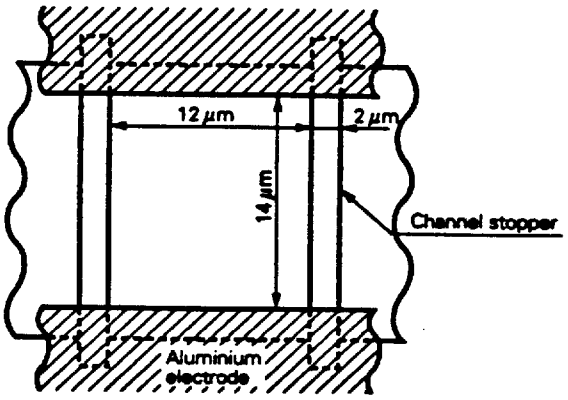
PIN CONFIGURATIONS (Top View)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi R1S}$, $V_{\phi R2S}$	−0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T_a = +25 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply	V_{OD}	11.4	12.0	12.6	V
Shift register clock signal high level	$V_{\phi 1H}$, $V_{\phi 2H}$	4.5	5	5.5	V
Shift register clock signal low level	$V_{\phi 1L}$, $V_{\phi 2L}$	−0.3	0	0.5	V
Reset signal high level	$V_{\phi R1SH}$, $V_{\phi R2SH}$	4.5	5	5.5	V
Reset signal low level	$V_{\phi R1SL}$, $V_{\phi R2SL}$	−0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	5	5.5	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3	0	0.5	V
Data rate	$2 \times f_{\phi R1S}$, $2 \times f_{\phi R2S}$	–	2	16	MHz

Remark φ1: φ1A1 to φ1A4, φ1L
φ2: φ2A1 to φ2A4, φ2L

ELECTRICAL CHARACTERISTICS ★

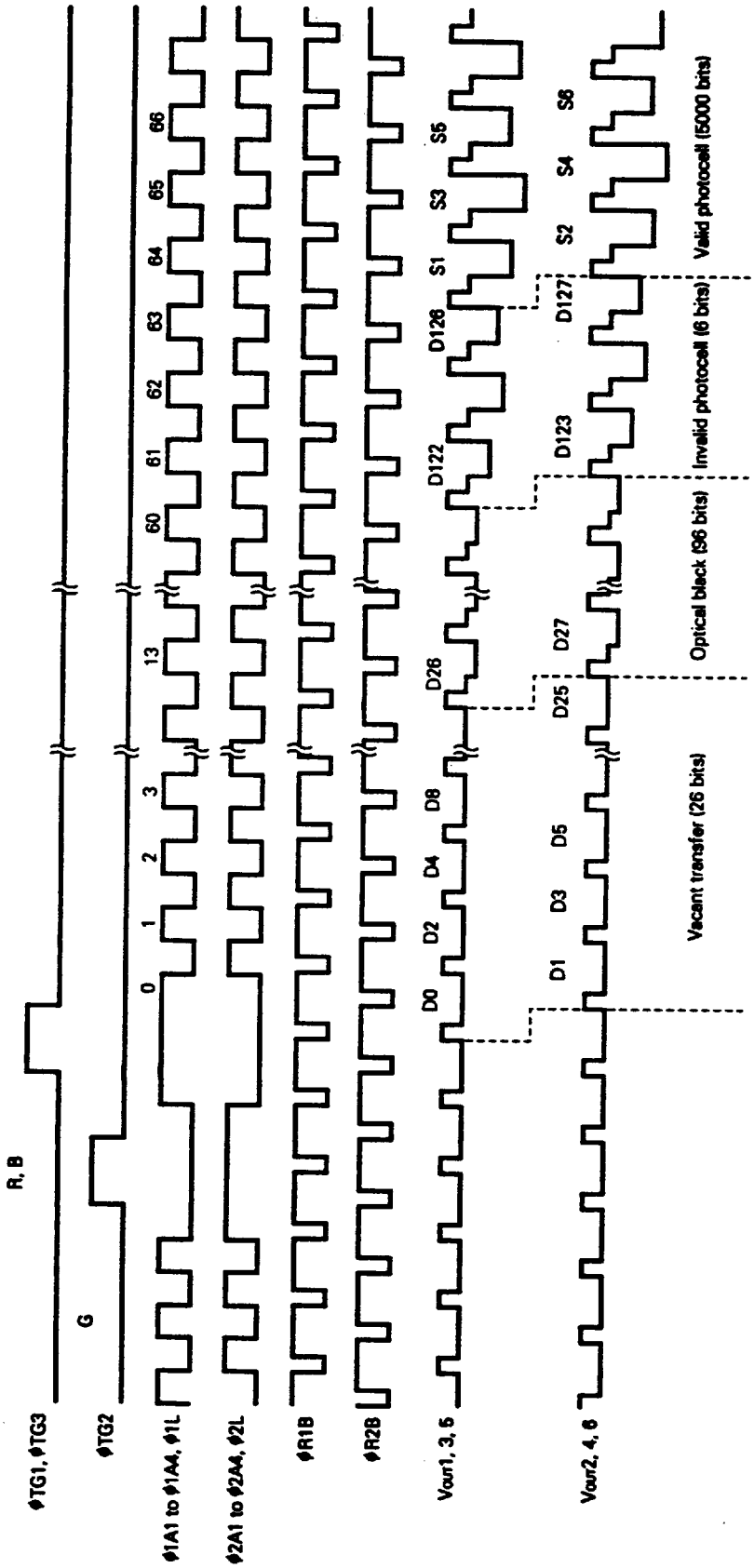
T_a = +25 °C, V_{DD} = 12 V, $f_{\phi R1S}$, $f_{\phi R2S}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms
light source; 3200 K halogen lamp +C500 (infrared cut filter), input signal clock = 5 V_{P-P}

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{SAT}		1.0	1.3	–	V
Saturation exposure	SER			0.3		lx•s
	SEG			0.3		lx•s
	SEB			0.6		lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		±6	±15	%
Average dark signal	ADS			0.1	5	mV
	DSNU			0.5	5	mV
Power consumption	P_W			300	500	mW
Output impedance	Z_O			0.5	1	kΩ
Response	R_R		2.71	3.87	5.03	V/lx•s
	R_G		2.66	3.80	4.91	V/lx•s
	R_B		1.45	2.07	2.70	V/lx•s
Image lag	IL	V_{OUT} = 500 mV		2	5	%
Offset level	V_{OS}		4	6	8	V
Output fall delay time	t_d		33	40	47	ns
Transfer efficiency	TTE		92	98		%
Register imbalance	RI	V_{OUT} = 500 mV	–4.0	0.0	4.0	%
Red response peak				630		nm
Green response peak				540		nm
Blue response peak				460		nm
Dynamic range	DR	V_{SAT}/DSNU		2600		times
Reset feed through noise	RFSN			300	500	mV

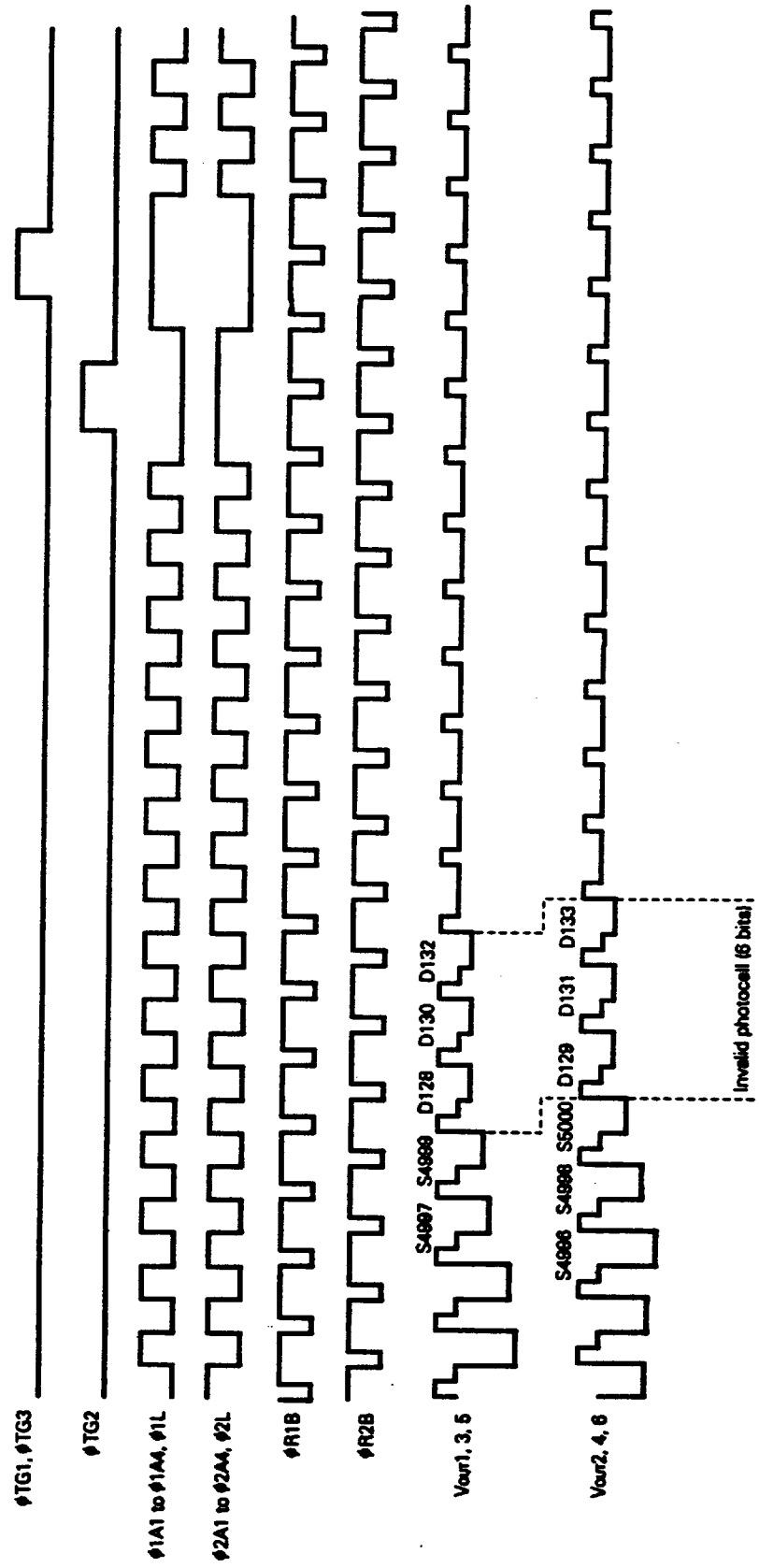
★ INPUT PIN CAPACITANCE

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Transfer gate pin capacitance	$C_{\phi TG}$	φTG1	16		300		pF
		φTG2	13				
		φTG3	10				
Reset clock pin capacitance	$C_{\phi R}$	φR1B	20		50		pF
		φR2B	5				
Last stage shift register clock pin capacitance	$C_{\phi L}$	φ1L	19		100		pF
		φ2L	6				
Shift register clock pin capacitance A	$C_{\phi A}$	φ1A1	18		250		pF
		φ1A4	8				
		φ2A1	17				
		φ2A4	9				
Shift register clock pin capacitance B	$C_{\phi B}$	φ1A2	15		500		pF
		φ1A3	11				
		φ2A2	14				
		φ2A3	12				

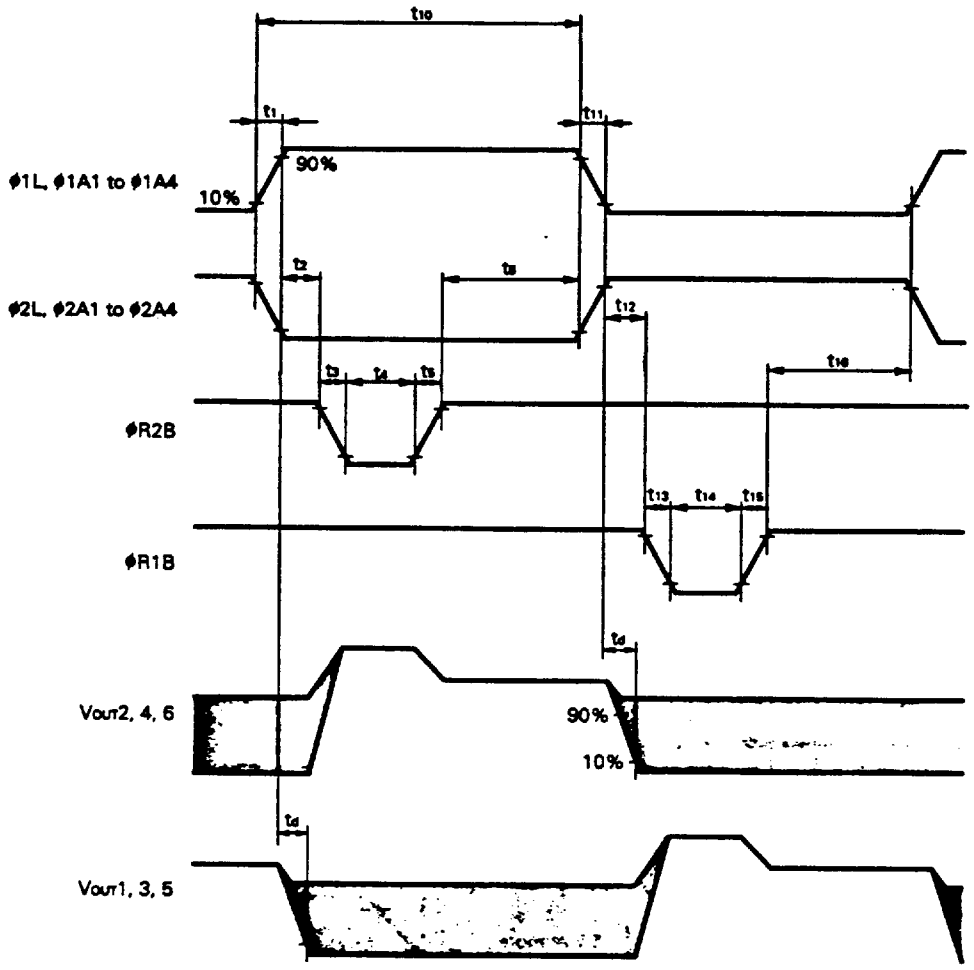
TIMING CHART 1



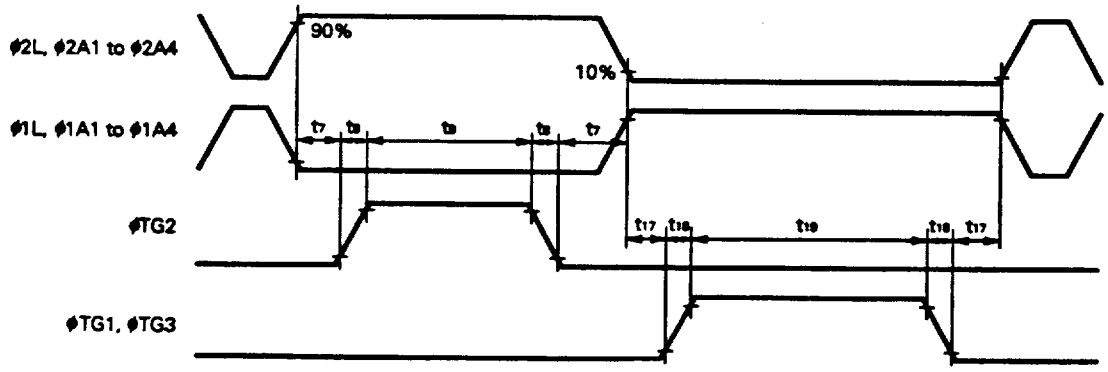
TIMING CHART 2



TIMING CHART 3 (Usual speed drive $f_{\phi R1B}$, $f_{\phi R2B}$ = 1 to 5 MHz)



TIMING CHART 4



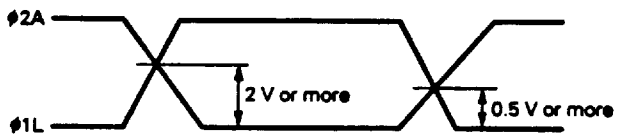
Recommended Timing (Usual speed drive $f_{\phi m1}$, $f_{\phi m2}$ = 1 to 5 MHz)

(Unit: ns)

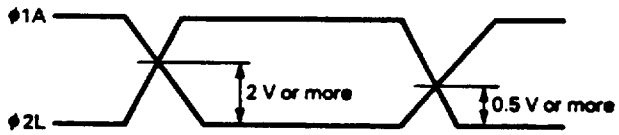
Symbol	MIN.	TYP.	MAX.
t_1, t_{11}	0	10	–
t_2, t_{12}	0	50	–
t_3, t_8, t_{13}, t_{18}	0	5	–
t_4, t_{14}	20	50	–
t_5, t_{15}	20	50	–
t_7, t_{17}	20	50	–
t_8, t_{16}	0	50	–
t_9, t_{19}	1000	2000	–

φ1A, φ2A cross points

φ1L, φ2A cross points



φ1A, φ2L cross points



Remark 1. Adjust input resistance of each pin for cross points (φ1A, φ2A), (φ1L, φ2A) and (φ1A, φ2L)

2. φ1A: φ1A1, φ1A2, φ1A3

φ2A: φ2A1, φ2A2, φ2A3

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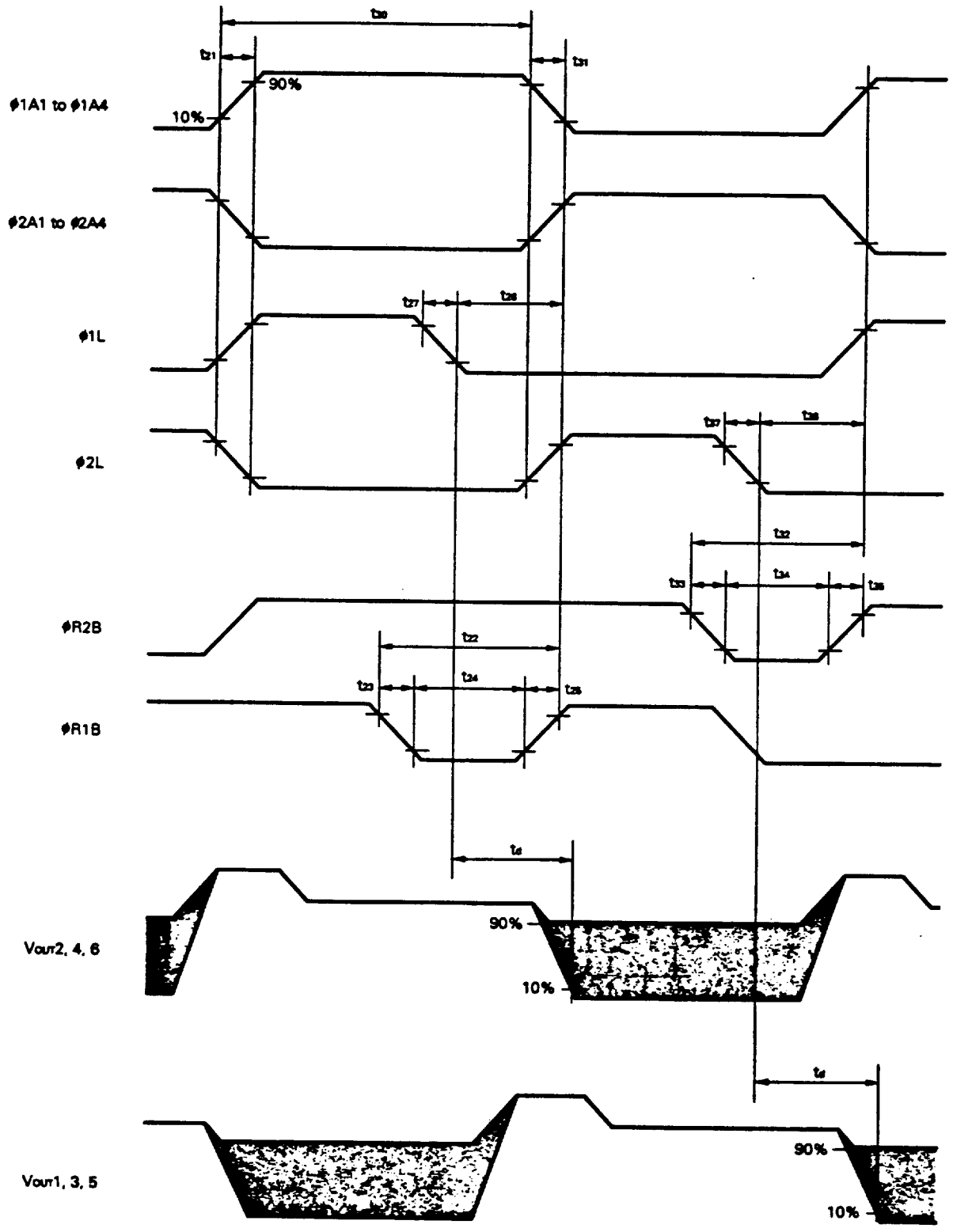
TIMING CHARTS (High speed drive $f_{\phi R1B}$, $f_{\phi R2B}$ = 5 to 8 MHz) ★



★ **Recommended Timing** (High speed drive $f_{\phi R1B}$, $f_{\phi R2B}$ = 5 to 8 MHz)

(Unit: ns)

Symbol	MIN.	TYP.	MAX.
t_{21}, t_{31}	0	10	—
t_{22}, t_{32}	0	30	—
t_{23}, t_{33}, t_{35}, t_{36}	0	5	—
t_{24}, t_{34}	20	$t_{28}/2$	—
t_{25}, t_{26}	10	20	—
t_{27}, t_{37}	0	10	—
t_{28}	60	100	—

Caution When driving μPD3725D-01 according to timing shown in TIMING CHART 1 at high speed, period of signal output is shorten, therefore data may not be sampled normally.
To sample data normally, drive μPD3725D-01 according to timing shown in TIMING CHART 5.
To extend the period of signal output, falling edge of last gate shift register clock ϕ1L, ϕ2L should be earlier than that of shift register clock ϕ1A, ϕ2A.
When making the falling edge of ϕ1L, ϕ2 early, output signal is effected by noise from reset clock ϕR1B, ϕR2B. To avoid the effection of this noise, the falling edge of ϕR1B, ϕR2B should be set earlier.
Driving at high speed, drive capability is necessary to be powered up. So design the peripheral circuit referring to peripheral circuit example 2.

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DEFINITIONS OF CHARACTERISTIC ITEMS

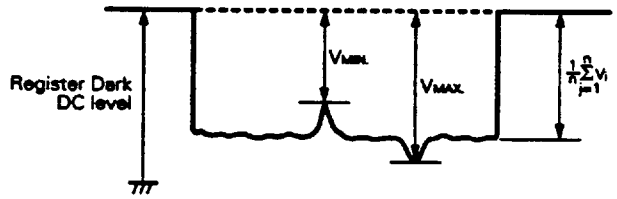
1. **Saturation voltage: V_{SAT}**
   Output signal voltage at which the response linearity is lost.

2. **Saturation exposure: SE**
   Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.

3. **Photo response non-uniformity: PRNU**
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

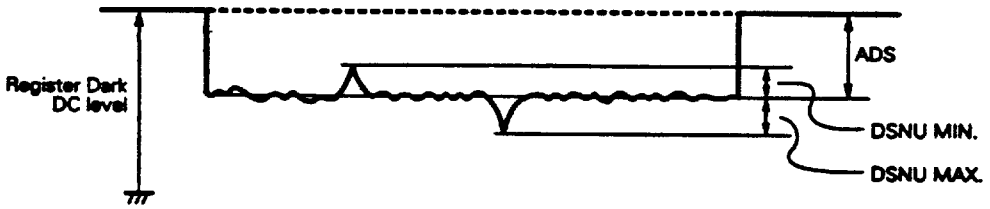
n: Number of valid bits
V_j: Output voltage of each bit



4. **Average dark signal: ADS**
   Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. **Dark signal non-uniformity: DSNU**
   The difference between peak or bottom output voltage in light shielding and ADS.



6. **Output impedance: Zo**
   Output pin impedance viewed from outside.

7. **Response: R**
   Output voltage divided by exposure (lx·s).
   Note that the response varies with the light source.

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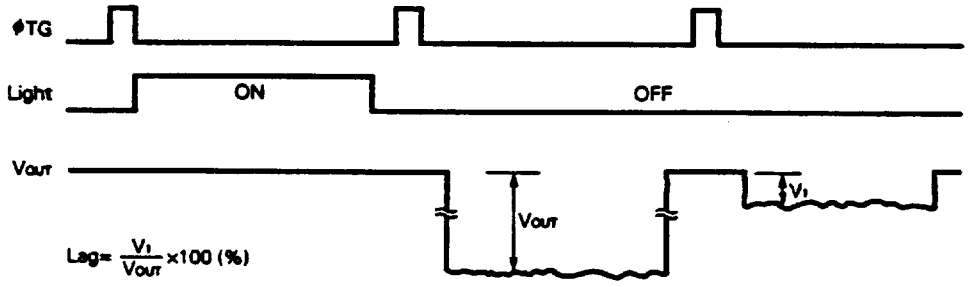
8. **Image Lag: IL**

The rate between the last output voltage and the next one after read out the data of a line.

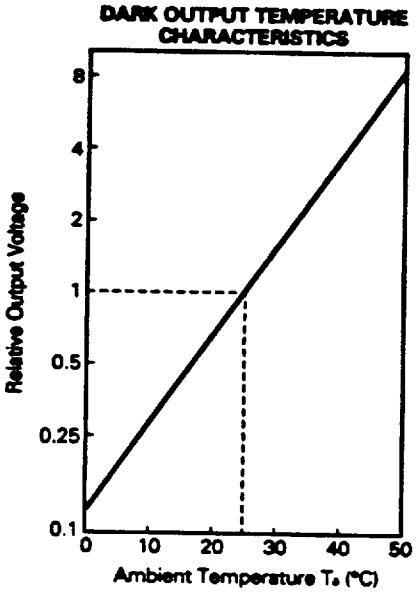


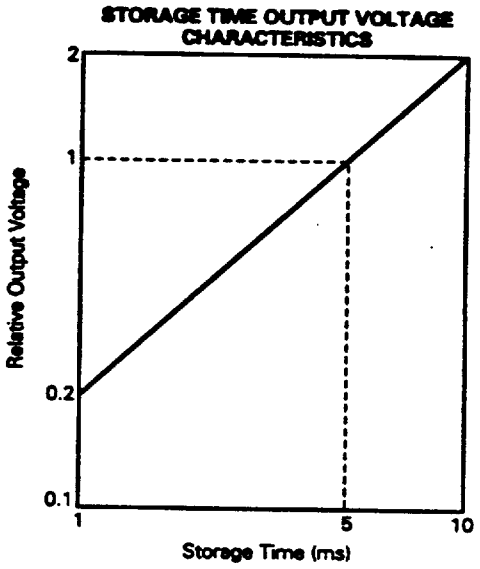
9. **Register Imbalance: RI**

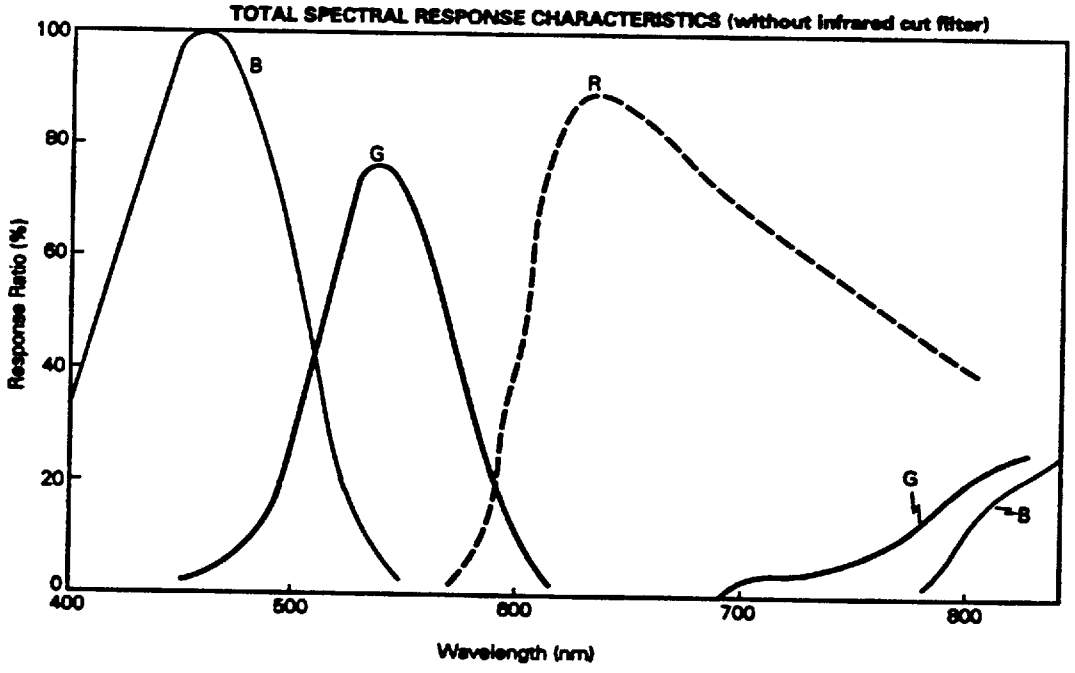
The rate of the average voltage which is the difference between the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

$$RI = \frac{\frac{1}{n}\sum_{j=1}^{n}|Vj - Vj+1|}{\frac{1}{n}\sum_{j=1}^{n}Vj} \times 100\ (\%)$$

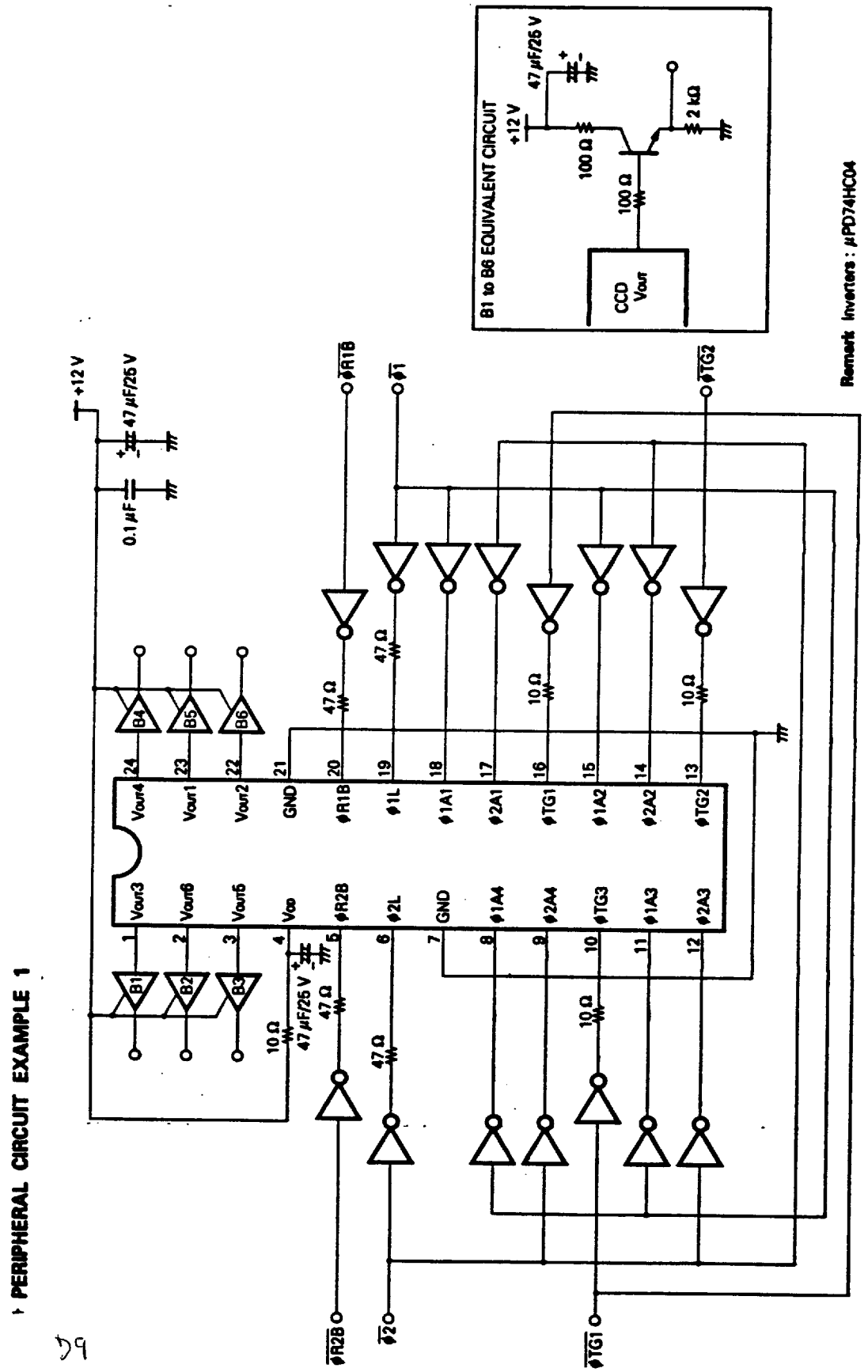
STANDARD CHARACTERISTIC CURVES (T_a = +25 °C)





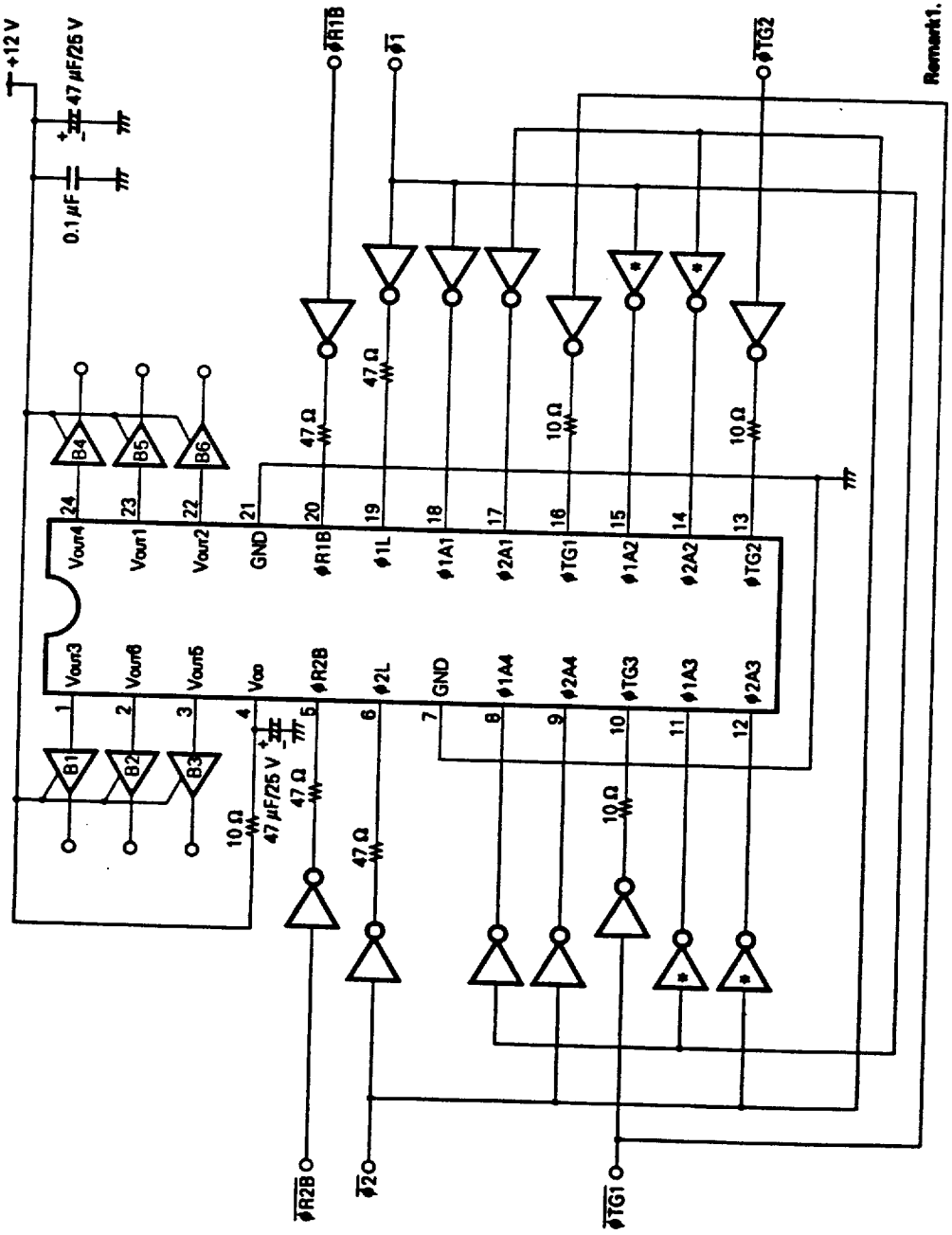


PERIPHERAL CIRCUIT EXAMPLE 1



The application circuits and their parameters are for reference only and are not intended for use in actual design-in's.

★ PERIPHERAL CIRCUIT EXAMPLE 2 (For high speed drive)



Remark1. Inverters : 74AC04
2. For * inverter, use high speed inverter which has double capability of 74AC04

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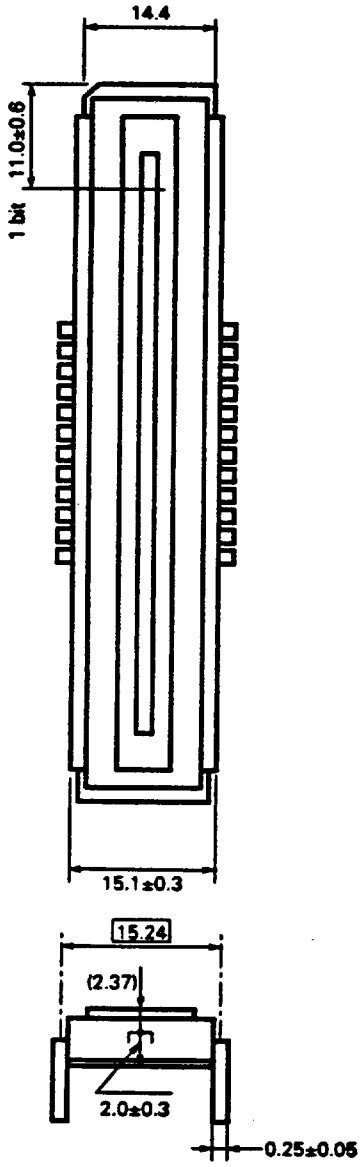
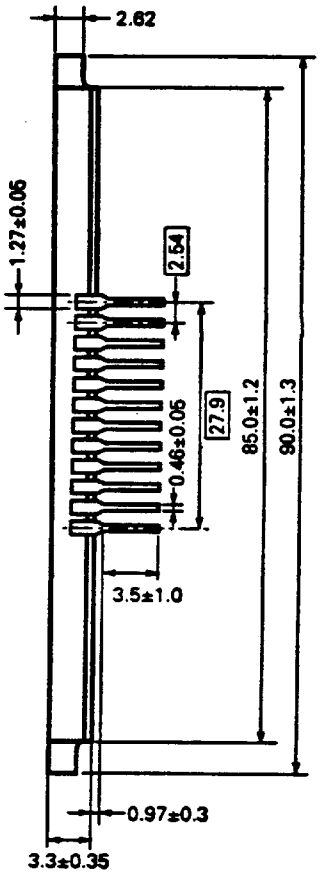
★ **PACKAGE DIMENSIONS (Unit: mm)**





RECOMMENDED SOLDERING CONDITIONS ★

The following conditions (see table below) must be met when soldering this product.
For more details, refer to out document "SEMICONDUCTOR DEVICE TECHNOLOGY MANUAL" (IEI-1207).
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 1 Type of Through Hole Device

μPD3725D-01:24-pin ceramic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only lead part)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 260 °C or below, Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.