



Am6687

Ultra-Fast Voltage Comparators

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

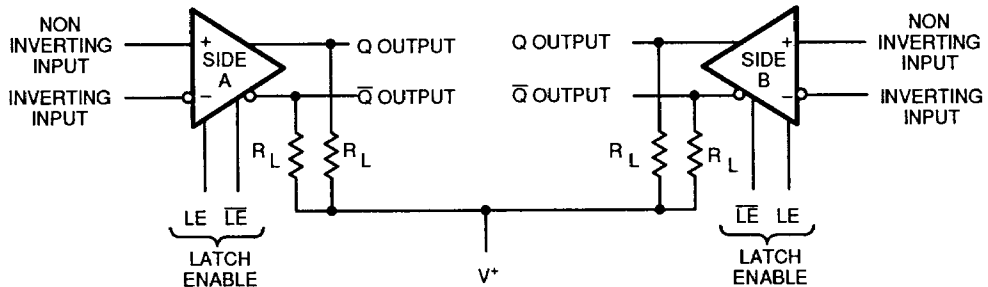
- 2.7 ns typical propagation delay
- Complementary ECL outputs
- 50-Ω driving capability
- Built-in latch

GENERAL DESCRIPTION

The Am6687 is an ultra-fast dual voltage comparator constructed on a single silicon chip with the advanced IMOX* process. It is pin-for-pin compatible with the Am687, and has improved speed performance. The circuit features very short propagation delays as well as excellent matching characteristics. Each comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output drive current is capable of driving terminated 50-ohm transmission lines. The low-input offsets and short delays make these comparators especially suitable for high-speed precision analog-to-digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample-and-hold mode. The Latch Enable inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is HIGH and \overline{LE} is LOW, the comparator functions normally. When LE is driven LOW and \overline{LE} is driven HIGH, the comparator outputs are locked in their existing logical states. If the latch function is not used, the LE must be connected to ground.

BLOCK DIAGRAM



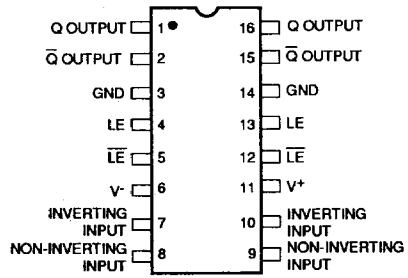
The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200 Ω connected to -2.0 V, or 200–2000 Ω connected to -5.2 V.

05679-001B

CONNECTION DIAGRAM

Top View

DIP



05679-002

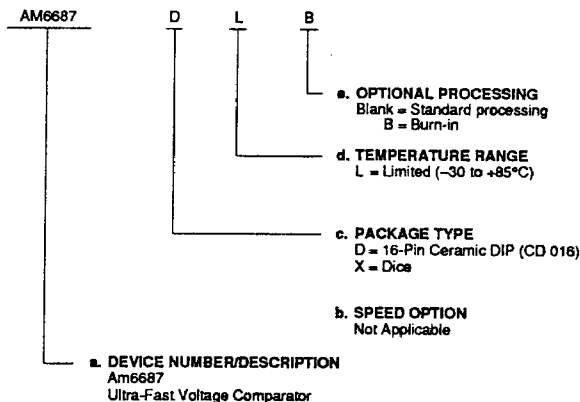
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations

Valid Combinations	
AM687	DL, DLB, XL, XM

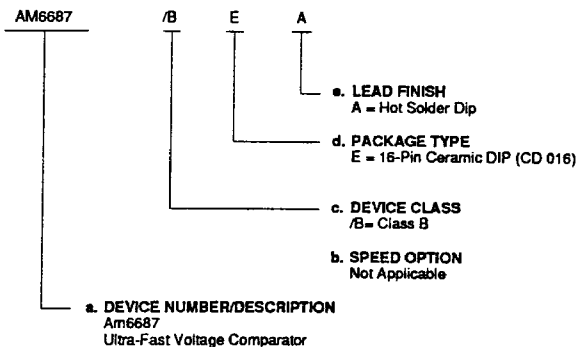
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations

Valid Combinations	
AM687	/BEA

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, 3.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Positive Supply Voltage	+7 V
Negative Supply Voltage	-7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30 mA
Power Dissipation (Note 1)	500 mW
Lead Temperature (soldering, 60 s)	300°C
Minimum Operating Voltage (V+ to V-)	9.7 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Limited (L) Devices
Ambient Temperature (T_A) -30 to +85°C

Military (M) Devices
Ambient Temperature (T_A) -55 to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 4, 5, 6 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input Offset Voltage	$RS \leq 100 \Omega$, $T_A = 25^\circ C$	-2	0.3	+2	-2	0.3	+2	mV
		$RS \leq 100 \Omega$	-2.5		+2.5	-3		+3	
$\Delta V_{os}/\Delta T$	Average Tempco of V_{os} (Note 3)	$RS \leq 100 \Omega$	-15	+3	+15	-15	+3	+15	$\mu V/^\circ C$
I_{os}	Input Offset Current	$25^\circ C \leq T_A \leq T_A (Max.)$	-1.5	0.2	+1.5	-1.5	0.2	+1.5	μA
		$T_A = T_A (Min.)$	-2.5	0.3	+2.5	-3.0	0.3	+3.0	
I_b	Input Bias Current	$25^\circ C \leq T_A \leq T_A (Max.)$		4	15		4	15	μA
		$T_A = T_A (Min.)$		7	25		8	30	
V_{in}	Input Voltage Range		-3.3		+2.7	-3.3		+2.7	V
CMRR	Common Mode Rejection Ratio	$RS \leq 100 \Omega$, $-3.3 V \leq V_{cm} \leq 2.7 V$	80			80			dB
SVRR	Supply Voltage Rejection Ratio	$RS \leq 100 \Omega$, $V_s = \pm 5\%$	60			60			dB
V_{oh}	Output HIGH Voltage	$T_A = 25^\circ C$	-0.96	-0.885	-0.81	-0.96	-0.885	-0.81	V
		$T_A = T_A (Min.)$	-1.06	-0.975	-0.89	-1.1	-1.010	-0.92	
		$T_A = T_A (Max.)$	-0.89	-0.795	-0.70	-0.85	-0.735	-0.62	
V_{ol}	Output LOW Voltage	$T_A = 25^\circ C$	-1.85	-1.750	-1.65	-1.85	-1.750	-1.65	V
		$T_A = T_A (Min.)$	-1.89	-1.783	-1.675	-1.91	-1.800	-1.69	
		$T_A = T_A (Max.)$	-1.825	-1.725	-1.625	-1.81	-1.693	-1.575	

Table continued on next page

DC CHARACTERISTICS (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I ₊	Positive Supply Current			20	32		20	32	mA
I ₋	Negative Supply Current			18	30		18	30	mA
P _{DISS}	Power Dissipation			250	373		250	373	mW

Notes: See notes following Switching Characteristics.

DEFINITION OF TERMS

V_{OS} Input Offset Voltage

That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

ΔV_{OS}/ΔT Average Temperature Coefficient of Input Offset Voltage

The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} Input Offset Current

The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_b Input Bias Current

The average of the two input currents.

R_{IN} Input Resistance

The resistance looking into either input terminal with the other grounded.

C_{IN} Input Capacitance

The capacitance looking into either input terminal with the other grounded.

V_{CM} Input Voltage Range

The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR Common Mode Rejection Ratio

The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR Supply Voltage Rejection Ratio

The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} Output HIGH Voltage

The logic-HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} Output LOW Voltage

The logic-LOW output voltage with an external pull-down resistor returned to a negative supply.

I₊ Positive Supply Current

The current required from the positive supply to operate the comparator.

I₋ Negative Supply Current

The current required from the negative supply to operate the comparator.

P_{DISS} Power Dissipation

The power dissipated by the comparator with both outputs terminated in 50 Ω to -2.0 V.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroup 9 is tested unless otherwise noted) ($V_{IN} = 100 \text{ mV}$, $V_{OVERDRIVE} = 10 \text{ mV}$)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD+} , t_{PD-}	Propagation Delay	$T_A = 25^\circ\text{C}$ (Note 3)	2.0	2.7	4.0	2.0	2.7	4.0	ns
$t_{PD+(E)}$, $t_{PD-(E)}$	Latch Enable to Output (HIGH or LOW)	$T_A = 25^\circ\text{C}$ (Note 4)		2.3			2.3		ns
t_s	Min. Latch Setup Time	$T_A = 25^\circ\text{C}$ (Note 4)		1.0			1.0		ns
t_h	Min. Latch Hold Time	$T_A = 25^\circ\text{C}$ (Note 4)		-0.5			-0.5		ns

- Notes:
1. Derate at $9 \text{ mW}/^\circ\text{C}$ for operation at ambient temperature above $+115^\circ\text{C}$.
 2. Unless otherwise specified $V_+ = 5.0 \text{ V}$, $V_- = -5.2 \text{ V}$, $V_T = 2.0 \text{ V}$, and $R_L = 50 \Omega$, all switching characteristics are for a 100-mV input step with 10 mV overdrive. The specification given for V_{OS} , I_{OS} , I_B , CMRR, SVRR, t_{PD+} , and t_{PD-} apply for $\pm 5\%$ supply voltages. The Am6687 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 linear feet per minute or greater.
 3. Not 100% tested. Group A sample only.
 4. Not tested in production. These tests are supported by device characterization data.

DEFINITION OF TERMS

(refer to Switching Waveforms)

t_{PD+} Input to Output HIGH Delay

The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW-to-HIGH transition.

t_{PD-} Input to Output LOW Delay

The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH-to-LOW transition.

$t_{PD+(E)}$ Latch Enable to Output HIGH Delay

The propagation delay measured from the 50% point of the Latch Enable signal LOW-to-HIGH transition to the 50% point of an output LOW-to-HIGH transition.

$t_{PD-(E)}$ Latch Enable to Output LOW Delay

The propagation delay measured from the 50% point of the Latch Enable signal LOW-to-HIGH transition to the 50% point of an output HIGH-to-LOW transition.

t_s Minimum Setup Time

The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h Minimum Hold Time

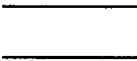



The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

Other Symbols

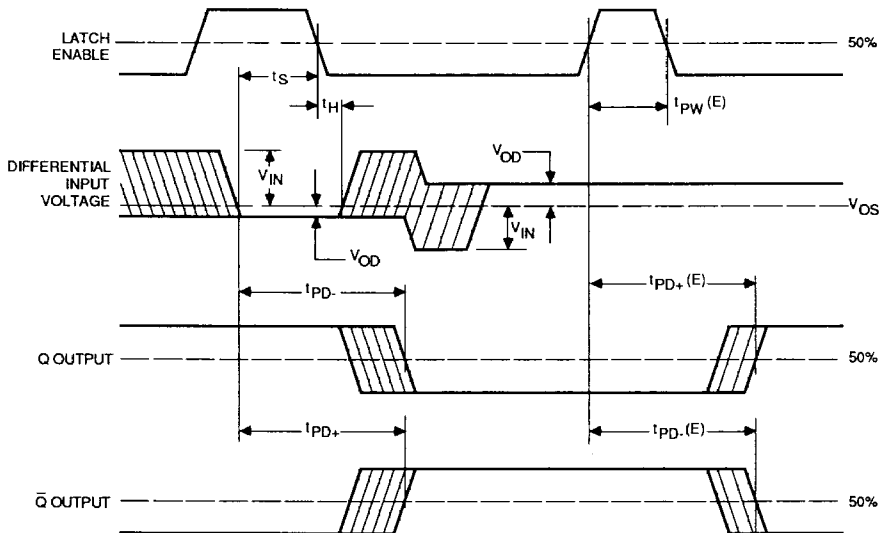
- T_A = Ambient temperature
- R_S = Input source resistance
- V_S = Supply voltages
- V_+ = Positive supply voltage
- V_- = Negative supply voltage
- V_T = Output load terminating voltage
- R_L = Output load resistance
- V_{IN} = Input pulse amplitude
- V_{OD} = Input overdrive
- f = Frequency

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

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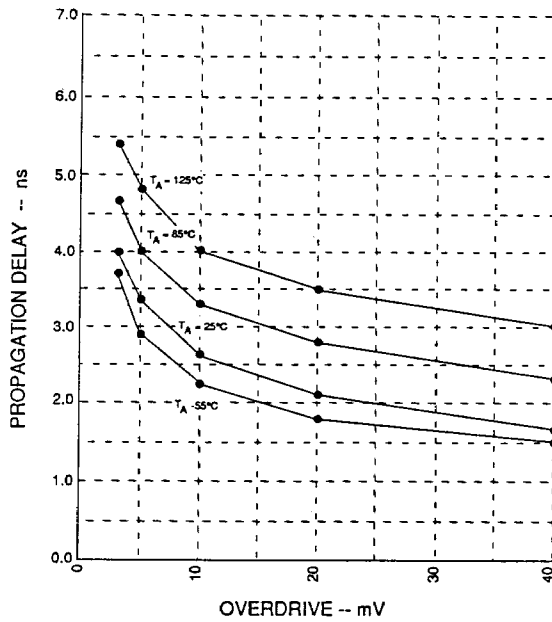
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The setup and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal

changes occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may or may not be detected.

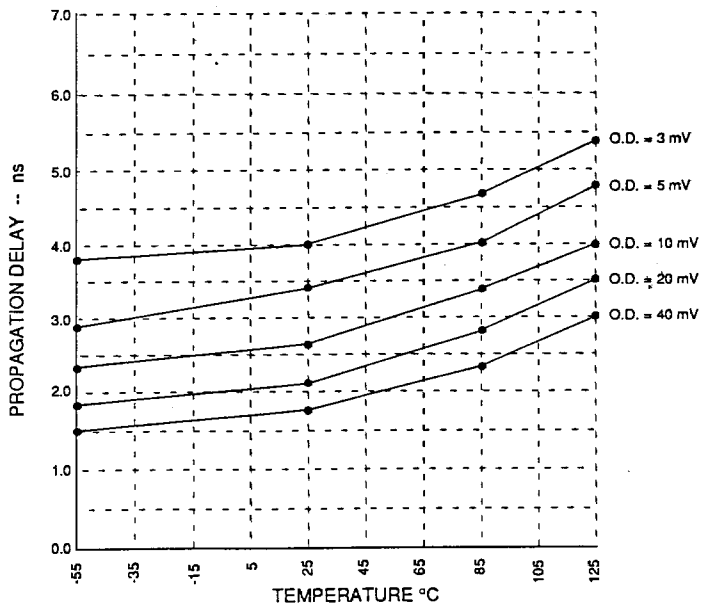
TYPICAL PERFORMANCE CURVES

Propagation Delay vs Overdrive



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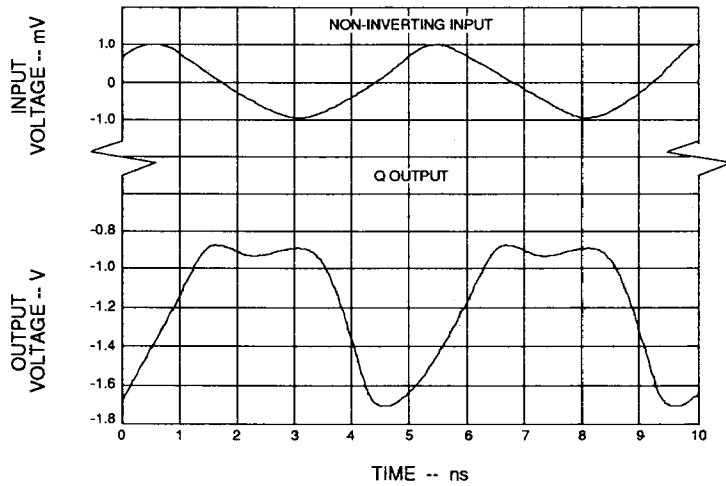
Propagation Delays vs Temperature also Overdrive



05975-006

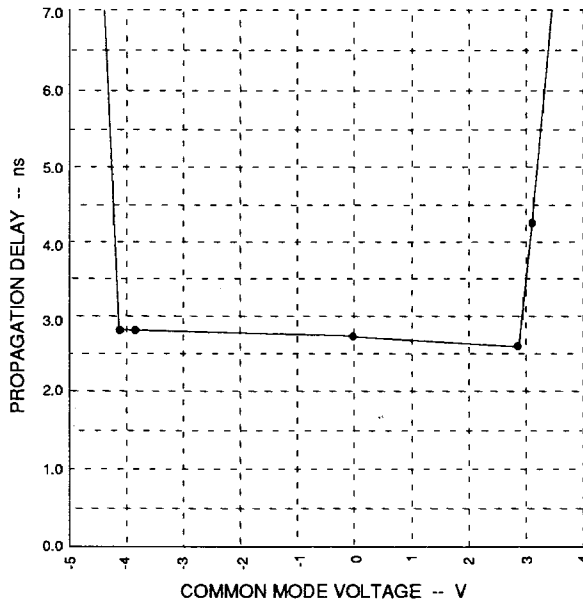
TYPICAL PERFORMANCE CURVES (Cont'd.)

Response to 200-MHz Sine Wave



05975-008

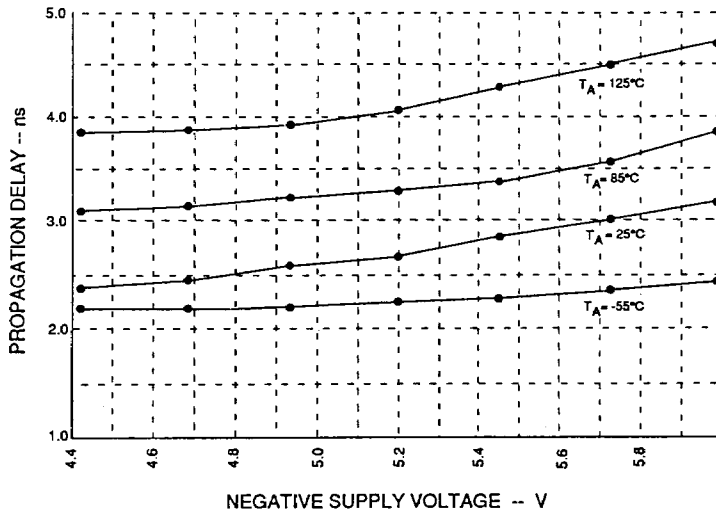
Propagation Delay vs VCM



05975-009

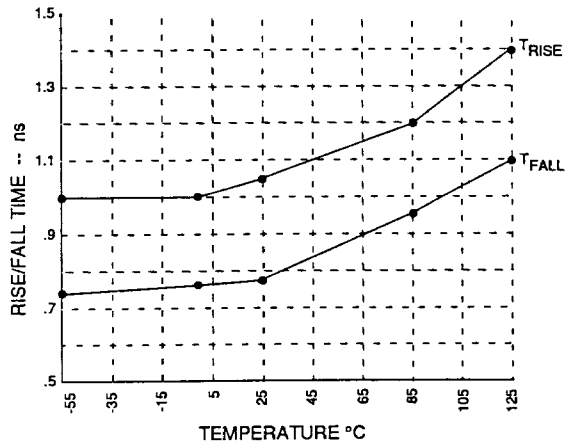
TYPICAL PERFORMANCE CURVES (Cont'd.)

Propagation Delay vs V-



05975-010

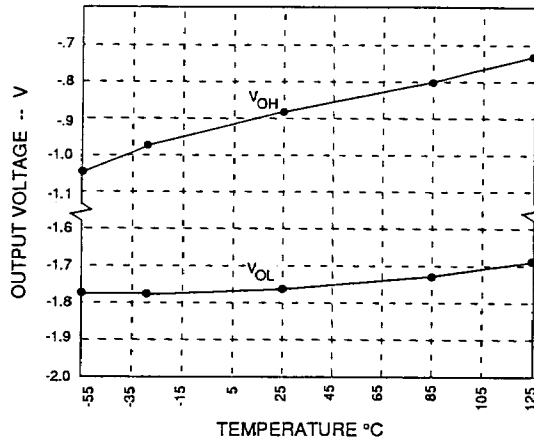
Output Rise and Fall vs Temperature



05975-011

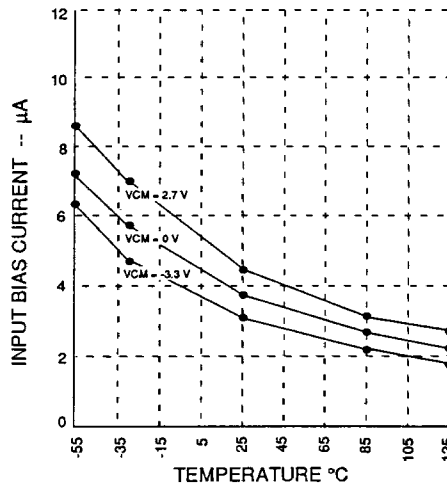
TYPICAL PERFORMANCE CURVES (Cont'd.)

Output Voltage vs Temperature



05975-012

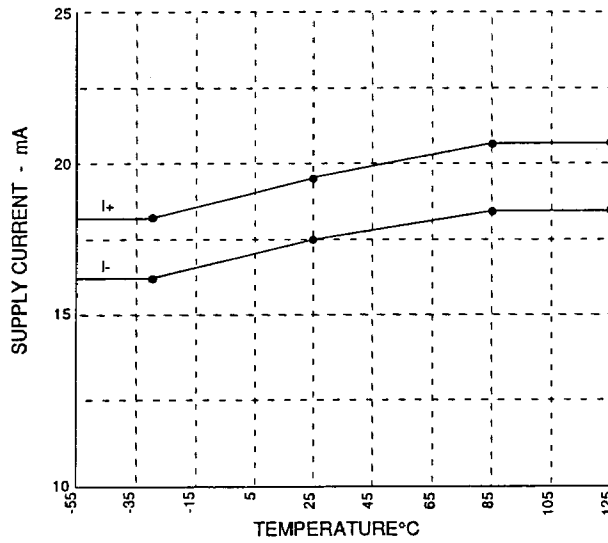
Input Bias Current vs Temperature



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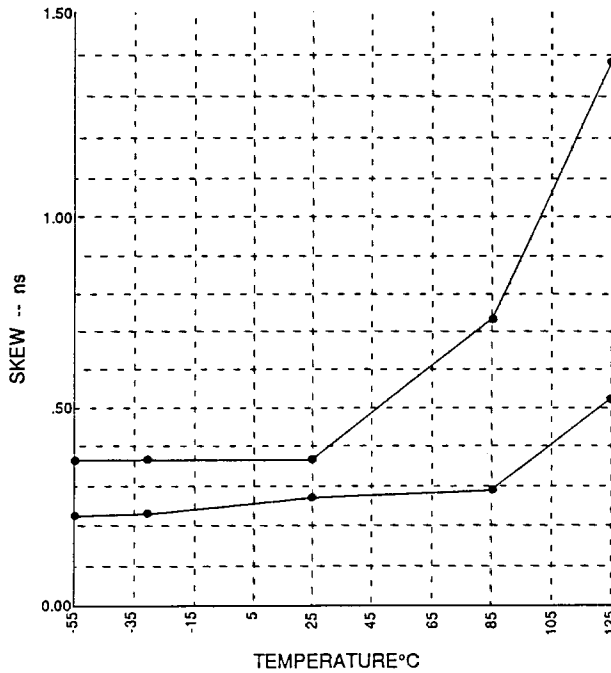
TYPICAL PERFORMANCE CURVES (Cont'd.)

Supply Currents vs Temperature



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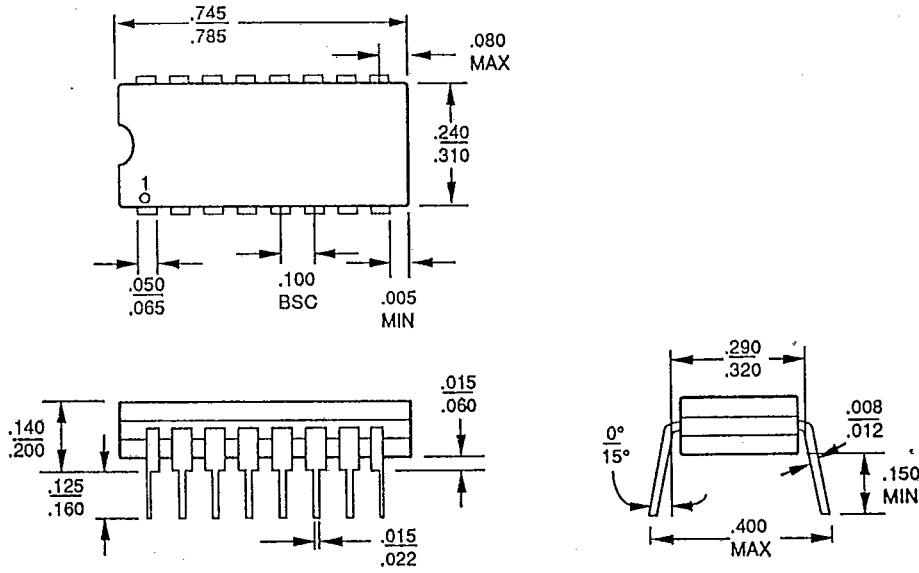
Skew vs Temperature



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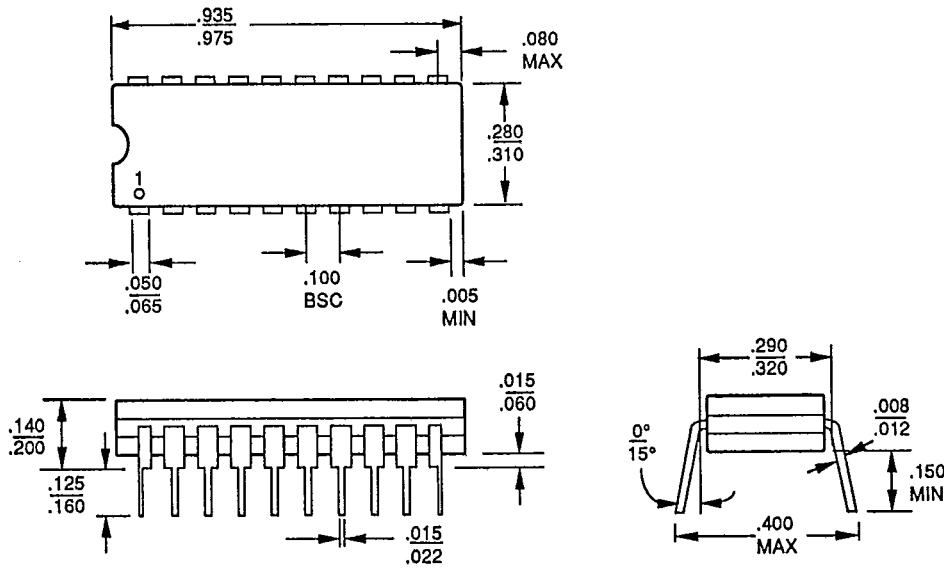
PHYSICAL DIMENSIONS
CD 016

T-90-20



07319B

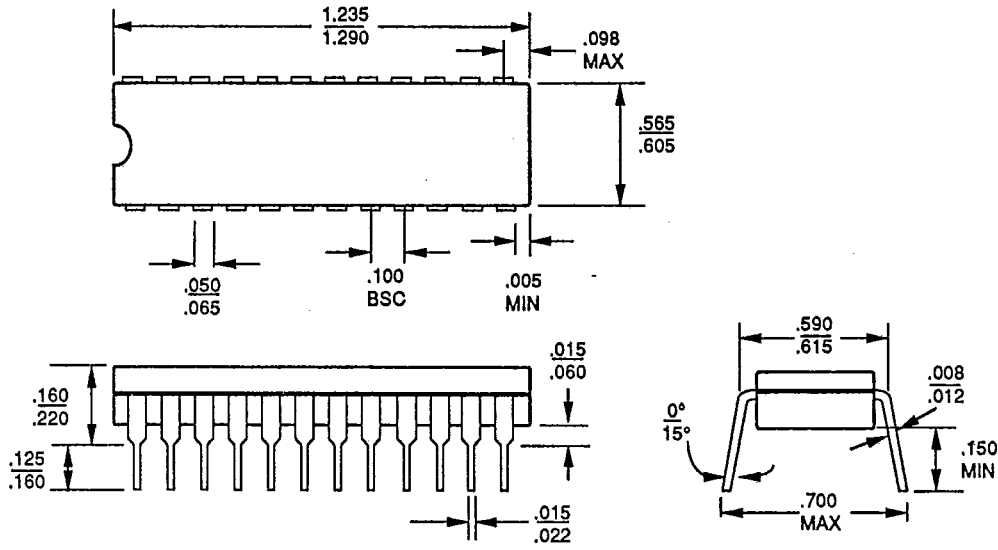
CD 020



03941-004C

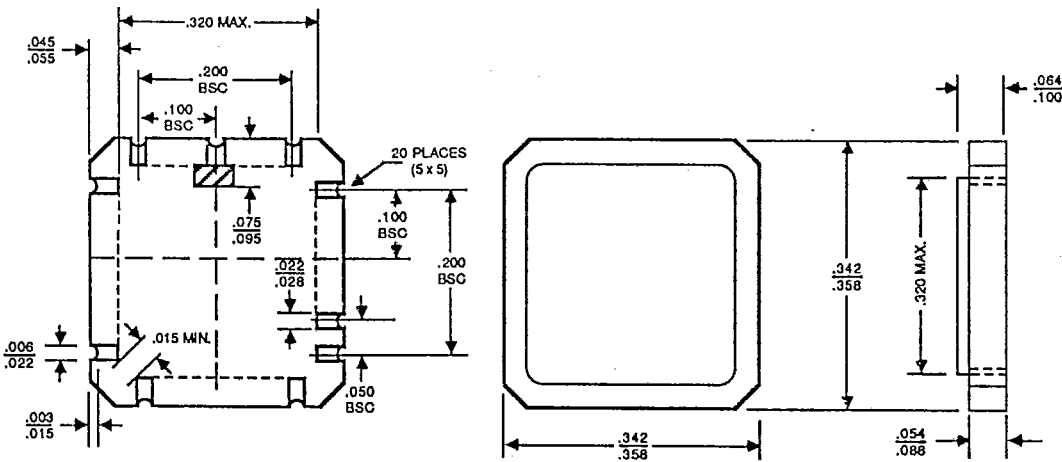
PHYSICAL DIMENSIONS (continued)
CD 024

T-90-20



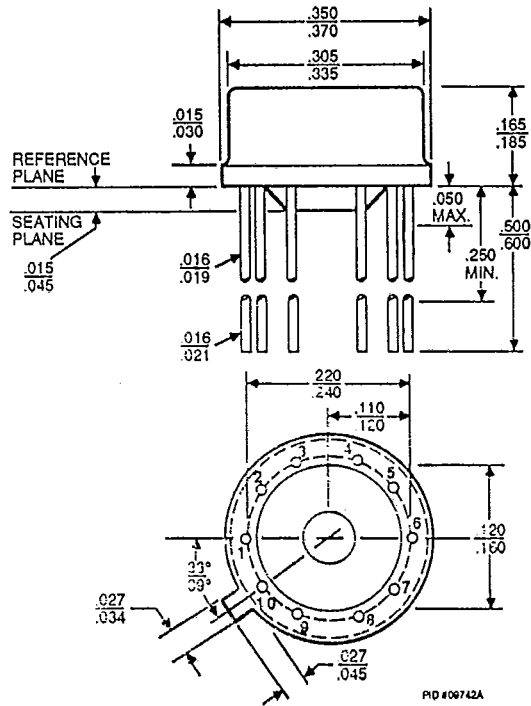
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CL 020

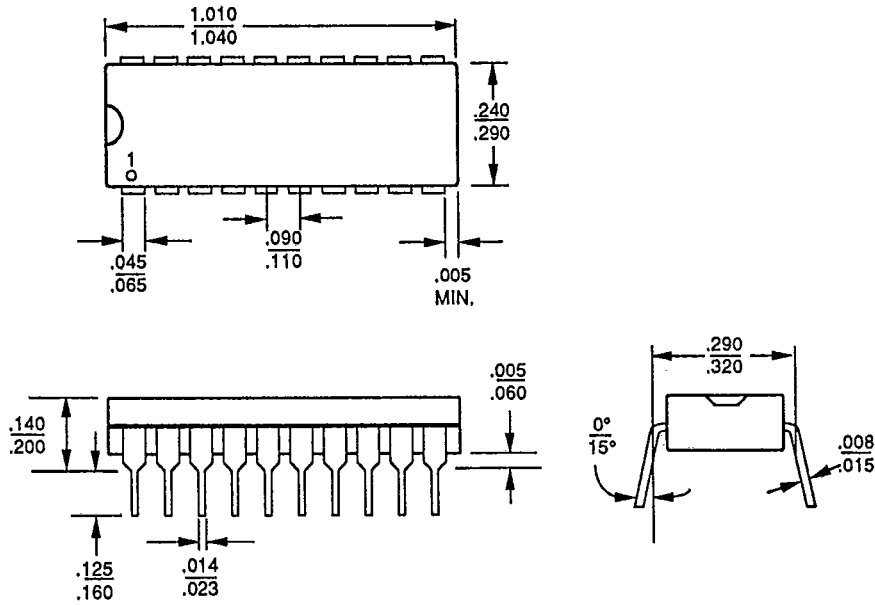


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PHYSICAL DIMENSIONS (continued)
MC 010



PD 020



03941-005C