3V high speed, high output drive GAL-type PLD — LVT16V8-6, -7

FEATURES

- Fastest 3V PLD – 6.0ns t_{PD}
- Supports 3-volt/5-volt mixed systems
- Low ground bounce <1.1V worst case
- Bus-hold devices eliminate the need for external pull-up resistors on unused inputs
- Metastable immune device
- High output drive capability: 32mA/–16mA
- Available in 20-pin Plastic Small Outline, PLCC and DIP packages
- Architectural flexibility
  - Emulates all 20 pin PAL devices
  - Up to 16 inputs and 8 outputs
  - Independently programmable I/O macrocells
  - Independently programmable output polarity
  - Product term output enable for combinatorial functions
  - Preload and Power Up Reset of all registers
- Design support provided by third party CAE vendors
- Programming support on industry standard programmers

DESCRIPTION

The LVT16V8 is a versatile, high performance, 3-volt GAL-type device with a pin-to-pin propagation delay of 6.0ns. The LVT16V8 operates in mixed 3-volt/5-volt power supply systems. The device is manufactured in Philips QUBiC BiCMOS process. In addition to the speed advantages, the BiCMOS process provides the higher noise immunity needed in 3-volt systems. The LVT16V8 is identical in function and fuse map to most industry standard 16V8s. The flexibility of the output macrocell allows the device to be used as a replacement for any of the common PLDs listed in Table 1.

The LVT16V8 outputs do not exhibit a metastable state due to setup/hold time violations at the flip-flop inputs. The 3-volt LVT16V8 inputs and outputs interface to 5-volt as well as 3-volt devices.

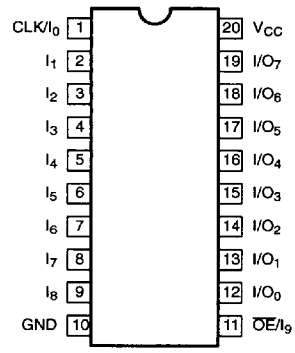
The LVT16V8 uses an AND/OR array for direct implementation of sum of products equations. Third-party CAE suppliers which support the LVT16V8 include Data I/O's Abel, Exemplar Logic's Core, Logical Devices CUPL, Isdata's LOG/IC, OrCAD-PLD, and Minc's PLDesigner.

After programming and verification, designs using the LVT16V8 can be secured by programming a security fuse link. Once programmed, the security fuse prevents readback of the internal programmed pattern.

The LVT16V8 is programmed using industry standard programmers, including Data I/O's Unisite, 2900, and 3900, and various programmers from BP Microsystems.

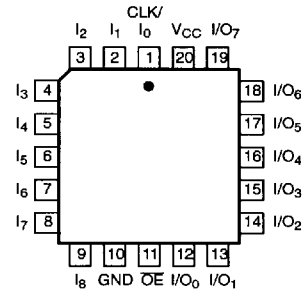
PIN CONFIGURATIONS

DB, D and N Packages



N = Plastic DIP (300mil-wide)
D = Plastic SOL (300mil-wide)
DB = Plastic Shrink Small Outline Package

A Package



A = Plastic Leaded Chip Carrier

SP00391B

PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		DRAWING NUMBER
20-Pin Plastic Dual-In-Line Package 300mil-wide	LVT16V8-6N LVT16V8-7N	6.0ns device 7.5ns device	SOT146-1
20-Pin Plastic Leaded Chip Carrier	LVT16V8-6A LVT16V8-7A	6.0ns device 7.5ns device	SOT380-1
20-Pin Plastic Small Outline Package	LVT16V8-6D LVT16V8-7D	6.0ns device 7.5ns device	SOT163-1
20-Pin Plastic Shrink Small Outline Package	LVT16V8-6DB LVT16V8-7DB	6.0ns device 7.5ns device	SOT339-1

FUNCTIONAL DESCRIPTION

The LVT16V8 uses an industry standard AND/OR logic array structure to implement sum of products equations. Figure 1 is a functional diagram of the LVT16V8. The LVT16V8's eight dedicated inputs and two multi-function input pins are connected to a 72 product term AND array. Of the 72 product terms, 64 are used for logic and 8 are used for direction control. The programmable AND array drives a fixed OR array. The eight OR terms drive eight output macrocells which are individually configurable by the user. A logic diagram of the LVT16V8 is given in Figure 2. The LVT16V8 also contains a 64-bit signature field that can be used to store information like manufacturing part number, revision level, etc. This field is accessible to the user even when the security fuse is programmed.

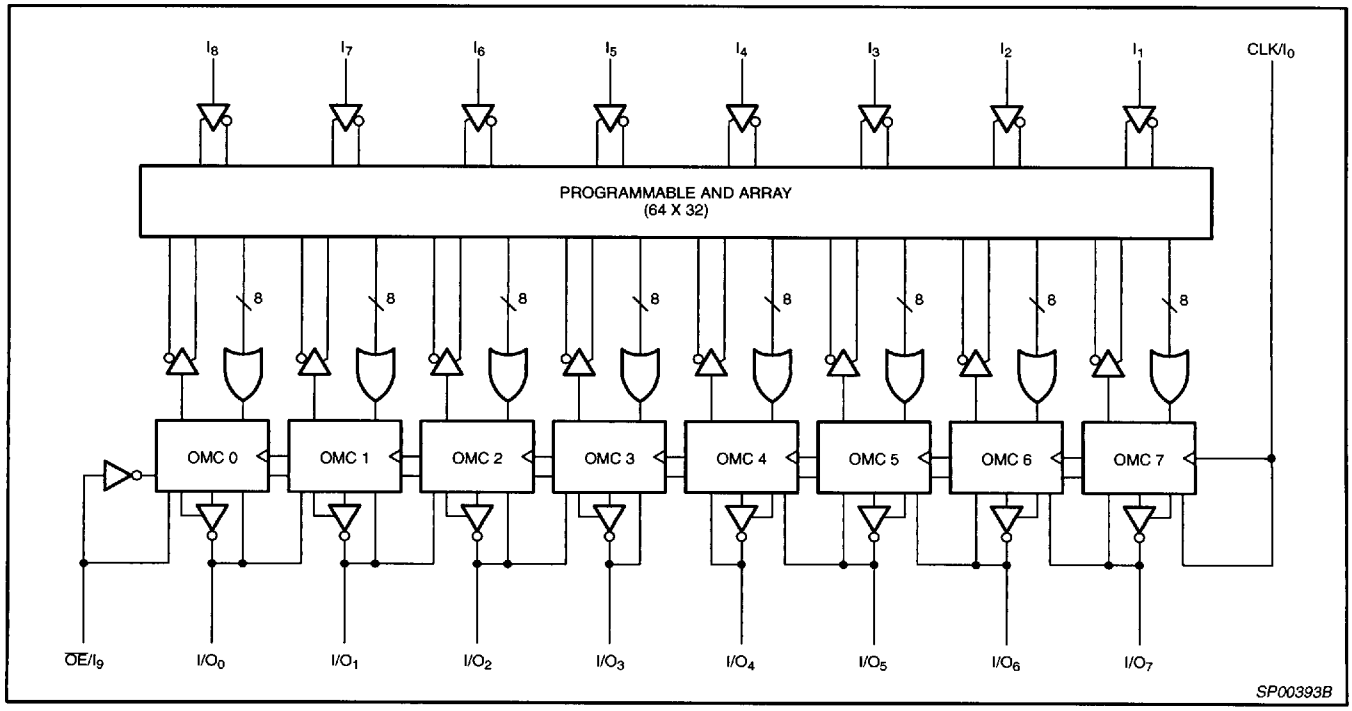


Figure 1. Functional Diagram

LOGIC DIAGRAM

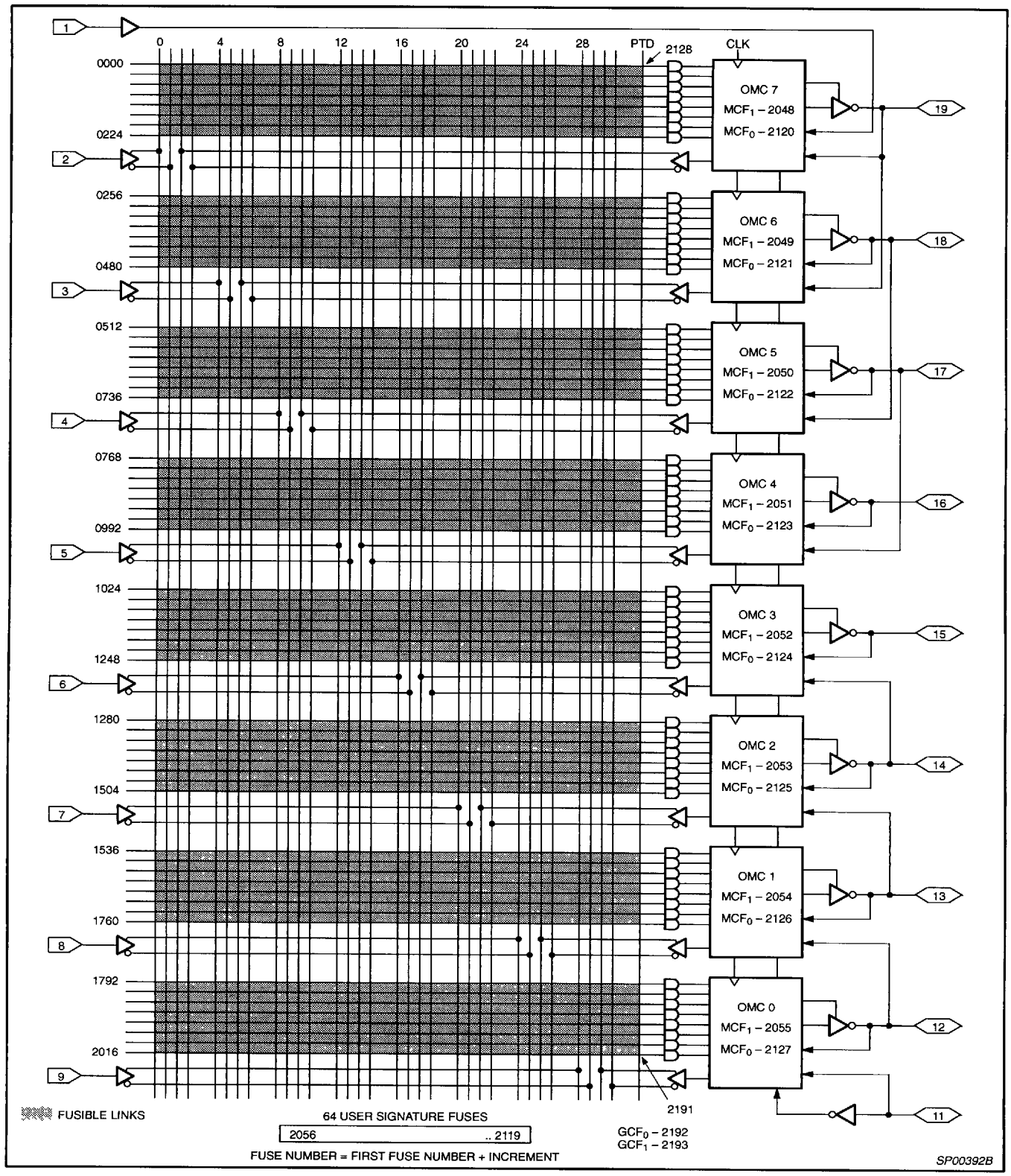


Figure 2. Logic Diagram

OUTPUT MACROCELL

The LVT16V8 output macrocell is configurable to support emulation of a variety of different types of PLDs. There are 18 configuration bits in each OMC which control whether the output is registered or combinatorial, output polarity, output enable, and feedback operation.

Global Output Macrocell Configurations

Globally, the OMCs are programmed as one of the following primary configurations: registered, complex, or simple. Two global configuration bits, GCF0 and GCF1, control the configuration mode for the eight macrocells. In addition to the global configuration bits, each individual OMC has two configuration bits, MCF0 and MCF1, which configure the output polarity and the input/output configuration for each OMC. Table 2 lists the configuration modes.

In the registered mode, all OMCs are configured as either dedicated registered outputs or as combinatorial I/O functions. The clock and OE signals are common to all registered OMCs. There are a total of eight product terms available for each registered OMC. OMCs configured as combinatorial I/O have asynchronous product term direction control. There are a total of seven product terms available for each combinatorial OMC. Dedicated input or outputs can be implemented as subsets of this configuration.

In the complex mode, OMCs are configured as either dedicated outputs or combinatorial I/O functions with programmable output polarity. Six of the eight OMCs can be configured as combinatorial I/O. The OMCs associated with pins 12 and 19 do not have input capability, and can only be configured as dedicated outputs. Designs requiring eight combinatorial outputs can be implemented in registered mode.

In the simple mode, OMCs have a maximum of eight logic product terms. The output polarity is individually programmable. Because the feedback paths of all OMCs are routed via adjacent pins, pins 15 and 16 cannot be configured as inputs or I/O, and operate only as dedicated inputs.

Local Configuration Functions

The polarity of each OMC can be active High or active Low, either to match a signal's polarity requirements or to reduce the number of product terms required to realize a logic function. Polarity selection is controlled by MCF1 in the OMC, and affects both registered and combinatorial outputs.

Each output buffer's 3-State control signal is driven either by a dedicated input or a product term signal. Using a product term allows the control to be a function of any product of the input or output feedback signals. The bidirectional I/O pins may be configured as dedicated inputs if the output buffer is disabled.

Table 1. PLD Architectures Emulated by LVT16V8

PLD Architectures Emulated by LVT16V8	LVT16V8 Global OMC Mode
16R8 16R6 16R4 16RP8 16RP6 16RP4	Registered
16L8 16H8 16P8	Complex
10L8 12L6 14L4 16L2 10H6 12H6 14H4 16H2 10P8 12P6 14P4 16P2	Simple

Table 2. Output Macrocell Configurations

	GCF_0	GCF_1	MCF_0	MCF_1	NOTES
Registered Mode					
Registered Output: Active Low	0	1	0	0	Pin 1 controls the common clock for all registered outputs. Pin 11 controls the common $\overline{OE}$ for all registered outputs. Pins 1 and 11 are permanently configured as CLK and $\overline{OE}$, respectively.
Registered Output: Active High	0	1	0	1	Pin 1 controls the common clock for all registered outputs. Pin 11 controls the common $\overline{OE}$ for all registered outputs. Pins 1 and 11 are permanently configured as CLK and $\overline{OE}$, respectively.
Combinatorial I/O: Active Low	0	1	1	0	Pins 1 and 11 are permanently configured as CLK and $\overline{OE}$, respectively.
Combinatorial I/O: Active High	0	1	1	1	Pins 1 and 11 are permanently configured as CLK and $\overline{OE}$, respectively.
Complex Mode					
Combinatorial I/O: Active Low	1	1	1	0	Pins 13 through 18 only.
Combinatorial I/O: Active High	1	1	1	1	Pins 13 through 18 only.
Combinatorial Output: Active Low	1	1	1	0	Pins 12 and 19 only.
Combinatorial Output: Active High	1	1	1	1	Pins 12 and 19 only.
Simple Mode					
Combinatorial I/O: Active Low	1	0	0	0	All I/O pins except pins 15 and 16.
Combinatorial I/O: Active High	1	0	0	1	All I/O pins except pins 15 and 16.
Combinatorial Output: Active Low	1	0	0	0	Pins 15 and 16 only.
Combinatorial Output: Active High	1	0	0	1	Pins 15 and 16 only.
Dedicated Input: Active Low	1	0	1	0	All I/O pins except pins 15 and 16.
Dedicated Input: Active High	1	0	1	1	All I/O pins except pins 15 and 16.

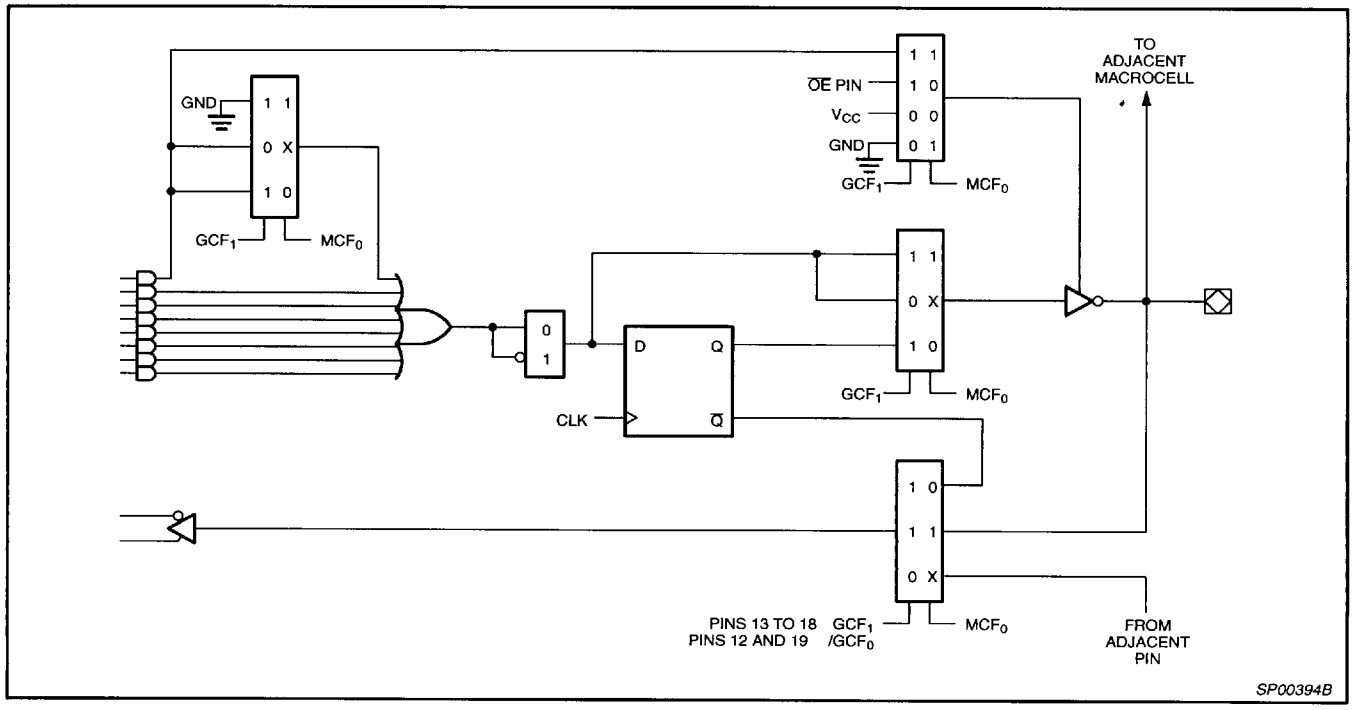


Figure 3. The Output Macro Cell Logic Diagram

Table 3. Metastability Characteristics

	0°C		25°C		75°C	
	τ	T_O	τ	T_O	τ	T_O
3.6V	84.60ps	3.17×10^5	85.80ps	163×10^6	122.00ps	2.66×10^2
3.3V	88.90ps	1.78×10^6	104.00ps	3.62×10^4	114.00ps	7.69×10^4
3.0V	121.00ps	1.90×10^3	129.00ps	1.01×10^3	145.00ps	2.56×10^2

METASTABILITY CHARACTERISTICS

The LVT16V8's outputs do not exhibit output anomalies even if the setup and/or hold time to the flip-flops are violated. The LVT16V8 is metastable immune due to two characteristics. The first is a patented Philips circuit that prevents the outputs from glitching, oscillating, or remaining in the linear region. The second is the flip-flop's inherent ability to resolve the metastable condition.

If a metastable event occurs within the flip-flop, there is an increased clock to Q delay. This delay is a function of the metastability characteristics of the device, defined by the parameters τ and T_O. Since the LVT16V8's outputs do not exhibit anomalies, the only metastable failure that can propagate in the system is when the next flip-flop in the system samples the LVT16V8's output during an input transition. By allowing sufficient time for the clock to Q delay, propagation of metastable failures are avoided.

As an example, suppose the LVT16V8 is used to synchronize 10MHz asynchronous data in a system with a 50MHz clock frequency. The output is sampled 8.5ns after the clock edge to ensure that any clock to Q delays resulting from internal metastability are complete and the outputs are transitioned. The mean time to failure (MTBF) is calculated by:

$$MTBF = \frac{e^{t'/\tau}}{T_O F_C F_I}$$

where

- t' = sample time from clock edge (s)
- F_C = clock frequency (Hz)
- F_I = average input event frequency (Hz)
- τ = metastability time constant (s)
- T_O = normalization constant for the propagation delay of the device (s)

Here, F_I is twice the data frequency, or 20MHz, because the input consists of both High and Low transitions. F_C is 50MHz, F_I is 20MHz, τ is 83ps, t' is 8.5ns, and T_O is 2.2×10^{17} seconds. This gives a MTBF of 43.1 years.

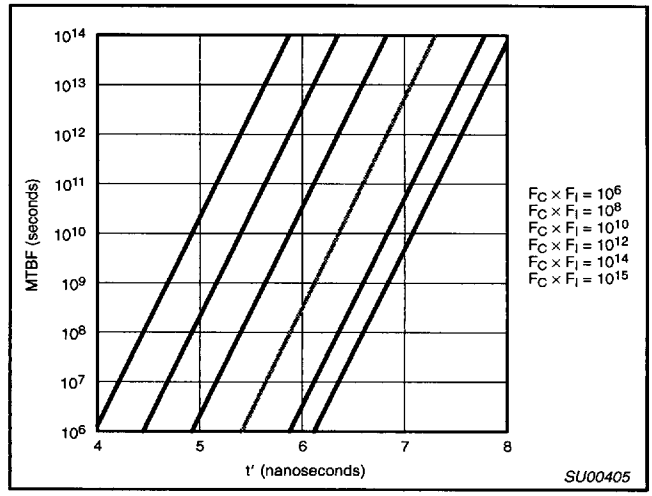


Figure 4. Mean Time Between Failures (MTBF) vs. t'
V_{CC} = 3.3 volts; T_{amb} = 25°C

POWER-UP RESET OPERATION

The LVT16V8's internal registers are reset when power is applied to the device. When the device is in register mode, all outputs are high, independent of the programmed polarity. In the simple and complex modes, the output state is a function of the programmed polarity.

Register Preload

The LVT16V8 registers can be pre-loaded via the I/O pins so that state machines can be tested without stepping through all known states. This allows for testing for correct operation in invalid states by loading flip-flops directly and observing that the logic recovers correctly. This functionality if available even when the security bit is programmed. The register preload is available on device programmers that are approved for programming the LVT16V8.

INPUT/OUTPUT BUFFER CHARACTERISTICS

The BiCMOS process provides increased noise immunity over CMOS processes. The ground bounce for the LVT16V8 is typically under 0.8 volts, and under 1.1 volts with V_{CC} = 3.6 volts. The test for ground bounce is done with seven outputs switching from High to Low, and the eighth output Low.

V_{CC} bounce occurs on a non-switching active High output, while other outputs transition High. V_{CC} bounce is more critical in 3.3 volt systems than 5 volt systems because of the lower noise margin between V_{CC} and V_{OH}. The LVT16V8's V_{CC} bounce is typically less than 1.0 volt.

Bus hold devices maintain the input High or Low until a minimum level of overdrive current is supplied to change the state. Bus hold devices are used when an input is unused and unconnected. The bus hold circuit can sink the minimum low sustaining current at the maximum V_{IL}, and can source the minimum high sustaining current at V_{IH} minimum. An external driver must source at least I_{BHLO} to switch a node from Low to High, and I_{BHHO} to switch a node from High to Low.

The LVT16V8 outputs directly drive TTL inputs. A pullup resistor is required when the LVT16V8 drives 5-volt CMOS threshold devices. The LVT16V8 device inputs directly interface to 5-volt devices.

DESIGN TOOLS

There are a wide variety of third party tools that run on PC and workstation platforms that target the LVT16V8. Third party development systems are available from Data I/O, Minc, Exemplar Logic, ISDATA, Logical Devices, Viewlogic, OrCAD, and others.

Third party software tools support the three different global OMC modes as different device types. These device types are listed in Table 4. Most design tools automatically select the device type, generally based on the register and output enable (OE) usage. If a design contains registers, the software selects the register mode. If a design contains combinatorial outputs with output enable controlled by a product term, the software selects the complex mode. The software selects the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in Table 4 can be used to override the automatic device selection by the software. For further details, refer to the software manuals.

Table 4. Third Party Design Tools

THIRD PARTY SOFTWARE TOOL	MODE			AUTO MODE SELECT
	REGISTERED	COMPLEX	SIMPLE	
Data I/O ABEL	P16V8R	P16V8C	P16V8AS	P16V8
Logical Devices CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
Isdata LOG/IC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	Registered[1]	Complex[1]	Simple[1]	GAL16V8A
Minc PLDesigner	P16V8R[1]	P16V8C[1]	P16V8C[1]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[2]	G16V8

NOTES:
1. Used with **Configuration** keyword.
2. Supported on Version 1.20 or later.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.5	4.6	V
V_{IN}	Input voltage[2]	–0.5	7.0	V
V_{OUT}	Output voltage[3]	–0.5	5.5	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current		100	mA
T_{stg}	Storage temperature range	–65	150	°C
T_J	Junction temperature		150	°C
T_{amb}	Ambient temperature		75	°C
T_R	Allowable thermal rise ambient to junction		75	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except in programming mode.
3. Outputs can be pulled up to 7V via external pull-up resistor.

OPERATING RANGE

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	3.0	3.6	V
T_{amb}	Operating free-air temperature	0	75	°C

DC ELECTRICAL CHARACTERISTICS

Commercial: 3.0V ≤ V_{CC} ≤ 3.6V; 0°C ≤ T_{amb} ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = MIN		0.8	V
V_{IH}	High-level input voltage	V_{CC} = MAX	2.0		V
V_I	Clamp voltage	V_{CC} = MIN, I_{IN} = –18mA		–1.2	V
V_{OH}	High-level output voltage	I_{OH} = –100 µA	V_{CC}–0.2		V
		I_{OH} = –16mA	2.0		V
		I_{OH} = –6 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 100µA		0.2	V
		I_{OL} = 32 mA		0.5	V
		I_{OL} = 16 mA		0.4	V
Input current					
I_{IL}	Low-level input leakage current (except Pin 1)	V_{CC} = MAX, V_{IN} = 0.0V		–10	µA
I_{IH}	High-level input leakage current (except Pin 1)	V_{CC} = MAX, V_{IN} = V_{CC}		10	µA
I_I	Input leakage current (Pin 1)	V_{CC} = MAX, V_{IN} = 5.5V		100	µA
I_{BHL}	Bus hold low sustaining current	V_{CC} = 3V, V_{IN} = 0.8V	75		µA
I_{BHH}	Bus hold high sustaining current	V_{CC} = 3V, V_{IN} = 2V	–75		µA
I_{BHLO}	Bus hold low overdrive current[2]	V_{CC} = 3.6V	500		µA
I_{BHHO}	Bus hold high overdrive current[2]	V_{CC} = 3.6V	–500		µA
Output current					
I_{OFF}	Output off current	V_{CC} = 0V, V_{IN} or V_{OUT} = 0 to 4.5V		±10	µA
I_{EX}	Current into an output in high state when V_O > V_{CC}	V_O = 5.5V, V_{CC} = 3.0V		±100	µA
I_{OZH}	Output leakage current	V_{OUT} = 5.5V		10	µA
I_{OZL}	Output leakage current	V_{OUT} =0V		–10	µA
I_{SC}	Short circuit current[1]	V_{OUT} = 0.5V	–30	–220	mA
I_{CC}	Supply current	V_{CC} = 3.6V, Outputs disabled, V_{IN} = V_{CC} or GND; I_{OUT} = Open		90	mA

NOTES:

1. One output is tested at a time. Duration of the short-circuit test does exceed one second.
2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where input current may be affected.

AC ELECTRICAL CHARACTERISTICS[3]

Commercial: $3.0V \le V_{CC} \le 3.6V$; $0°C \le T_{amb} \le 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LVT16V8-6			LVT16V8-7			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output	C_L = 50pF			6.0			7.5	ns
t_S	Setup time from input or feedback to Clock		4.0			6.0			ns
t_H	Hold time		0			0			ns
t_{CO}	Clock to output				5.0			5.0	ns
t_{CF}	Clock to feedback[1]				3.0			3.5	ns
t_{WL}	Width of Clock LOW		3.0			4.0			ns
t_{WH}	Width of Clock HIGH		3.0			4.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[2]		111			91			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[2]		135			118			MHz
t_{EA1}	Input, I/O, Feedback to Output Valid				7.0			9.0	ns
t_{ER1}	Input, I/O, Feedback to Output 3-State	C_L = 5pF			7.0			9.0	ns
t_{EA2}	$\overline{OE}$ to Output Valid	C_L = 50pF			5.0			6.0	ns
t_{ER2}	$\overline{OE}$ to Output 3-State	C_L = 5pF			5.0			6.0	ns
t_{PR}	Power-up reset delay				1			1	µs

Capacitance[2]

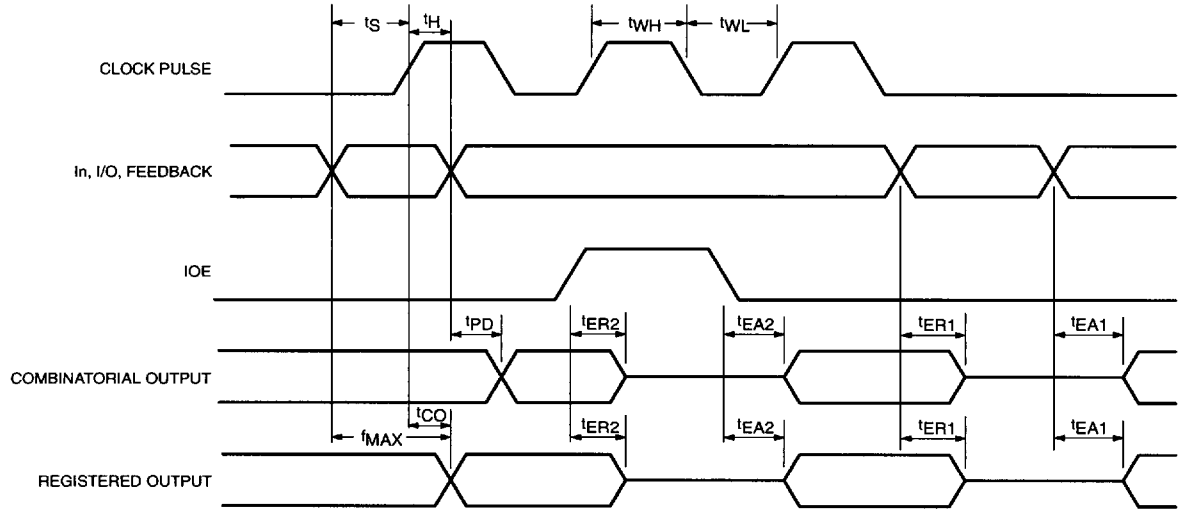
SYMBOL	PARAMETER	TEST CONDITIONS		LVT16V8-6			LVT16V8-7			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
C_{IN}	Input Capacitance (Pin 1)	V_{IN} = 2.0V	V_{CC} = 3.3V, T_{amb} = 25°C, f = 1MHz		10			10		pF
	Input Capacitance (Others)	V_{IN} = 2.0V			6			6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8			8		pF

Ground Bounce			MIN	TYP	MAX	UNIT
V_{OLP}	Maximum dynamic V_{OL}	V_{CC} = 3.3V, T_{amb} = +25°C, C_L = 50pF		0.7	1.1	V

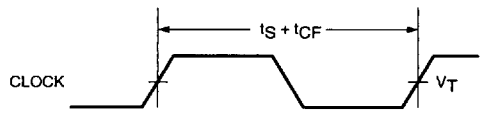
NOTES:

1. Calculated from measured f_{MAX} internal.
2. This parameter is not 100% tested, but is calculated at initial characterization and at any time the design is modified where its value may be affected.
3. Reference diagrams on page 12.

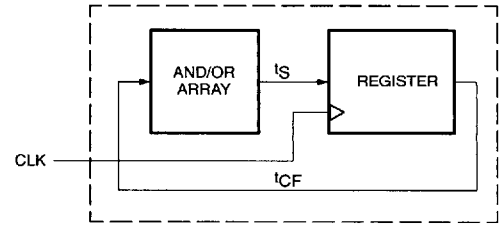
SWITCHING WAVEFORMS



AC Electrical Timing Characteristics



Clock to Feedback (f_{MAX} Internal) (See Path at Right)

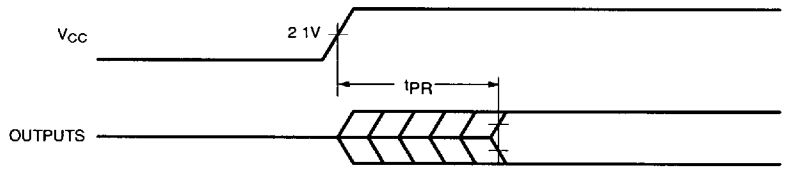


Clock to Feedback

SP00395C

NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 1.5ns max.

AC WAVEFORMS

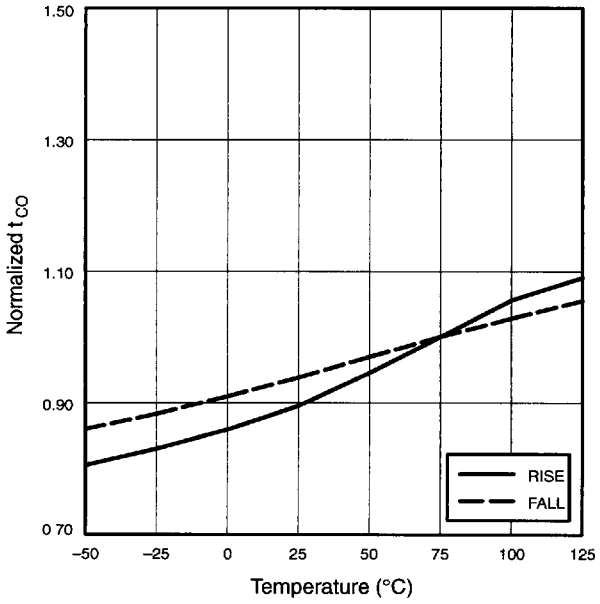


Power-Up Reset Waveform

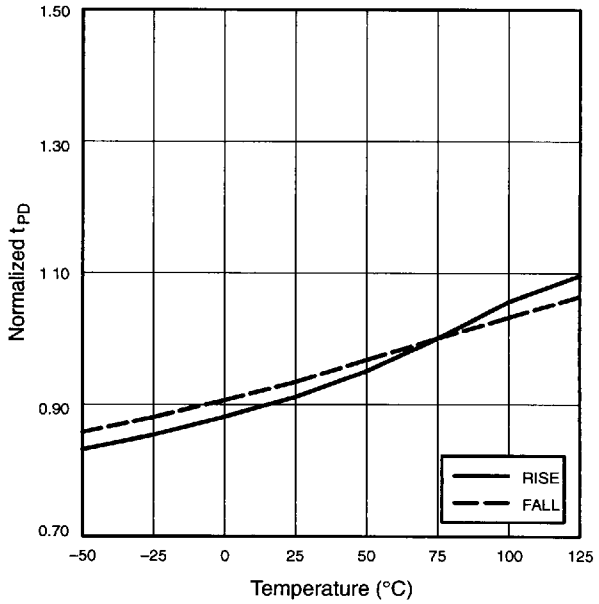
SP00396A

LVT16V8-6 TIMING CHARACTERIZATION

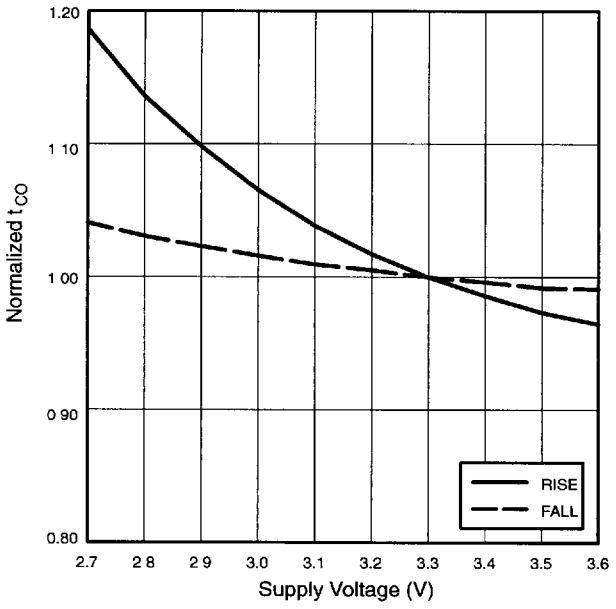
Normalized t_{CO} vs Temperature
(V_{CC} = 3.3V, output load = 50pF, 4outputs switching)



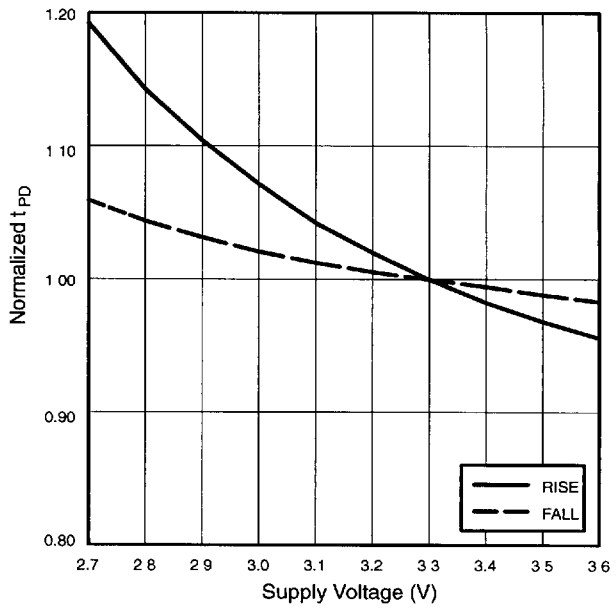
Normalized t_{PD} vs Temperature
(V_{CC} = 3.3V, output load = 50pF, 4 outputs switching)



Normalized t_{CO} vs V_{CC}
(temp = 25°C, output load = 50pF, 5 outputs switching)



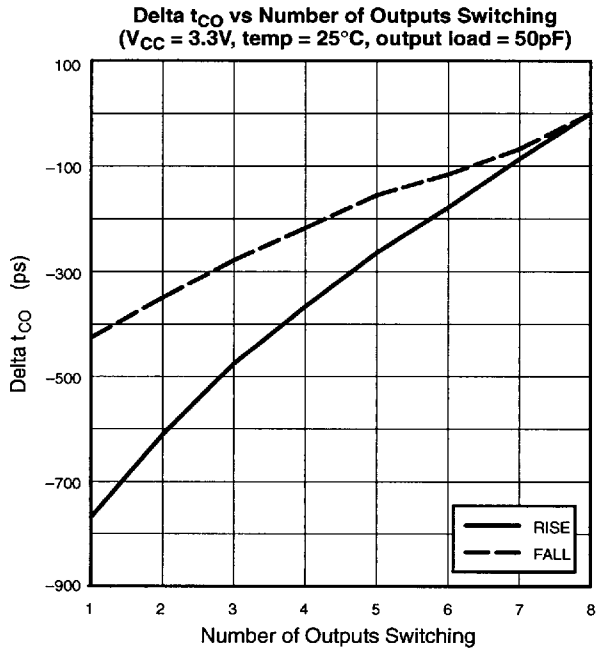
Normalized t_{PD} vs V_{CC}
(temp = 25°C, output load = 50pF, 5 outputs switching)

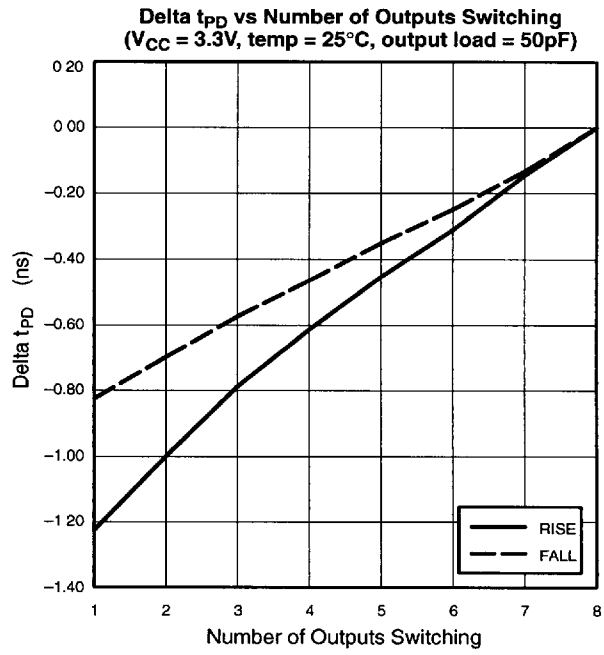


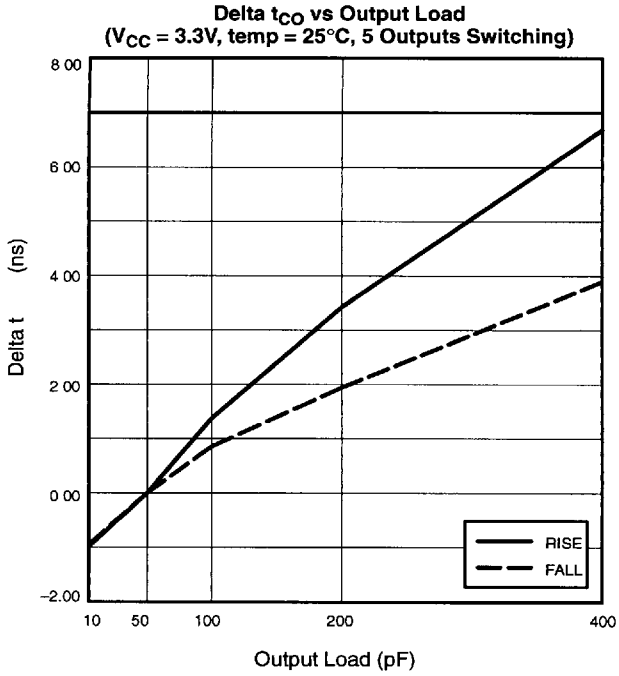
The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

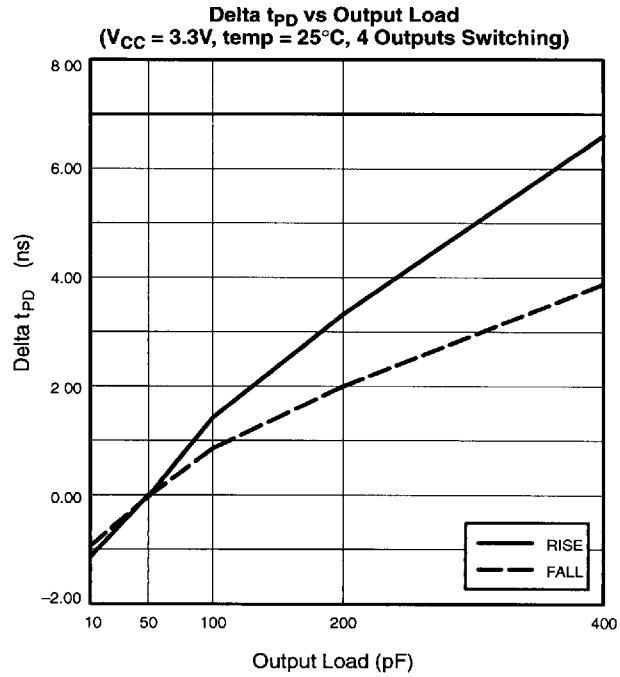
SP00401

LVT16V8-6 TIMING CHARACTERIZATION









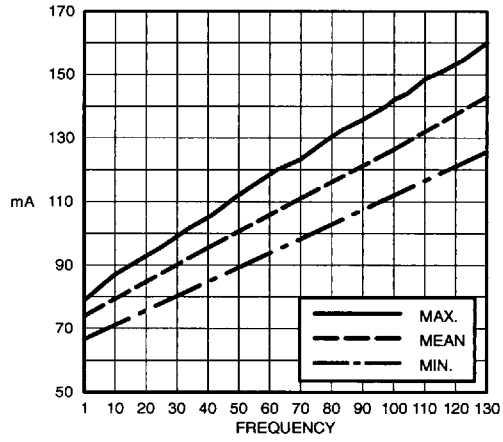
The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

SP00402

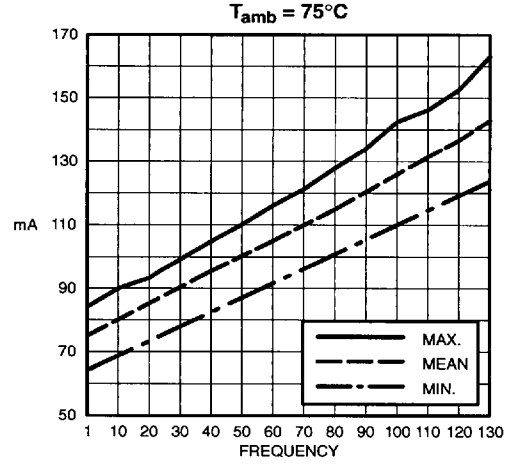
LVT16V8-6 I_{CC} vs. FREQUENCY

Output load = 50pF; No resistor load; 10-bit counter

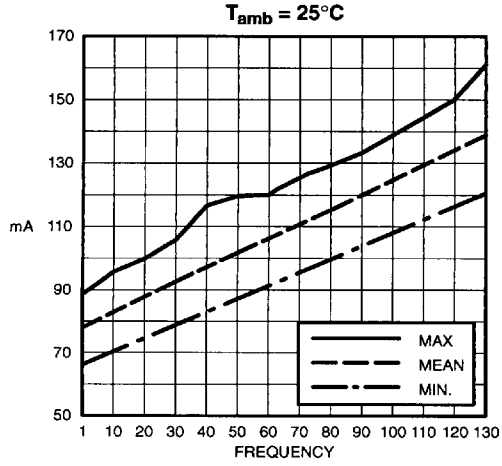
T_{amb} = 85°C



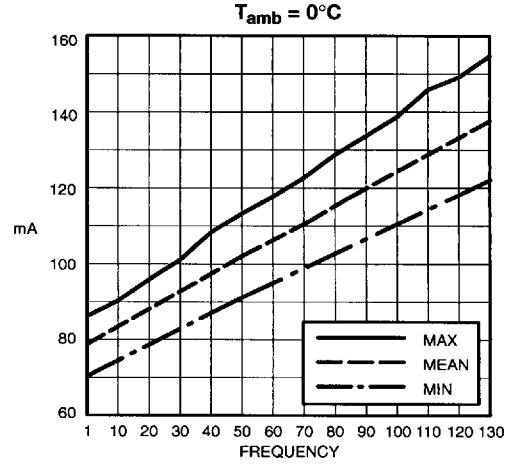
T_{amb} = 75°C



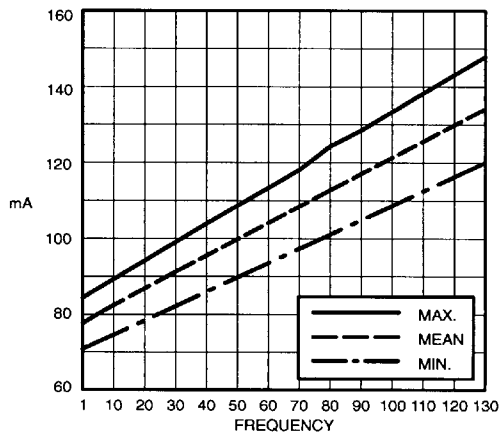
T_{amb} = 25°C



T_{amb} = 0°C

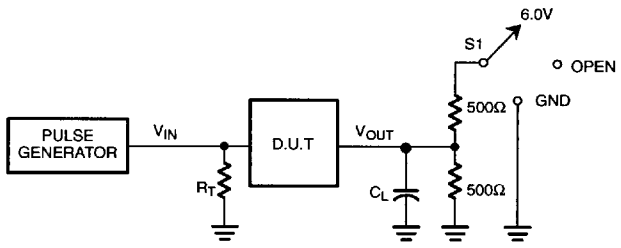


T_{amb} = –40°C



SP00403

TEST CIRCUIT



Test Circuit

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

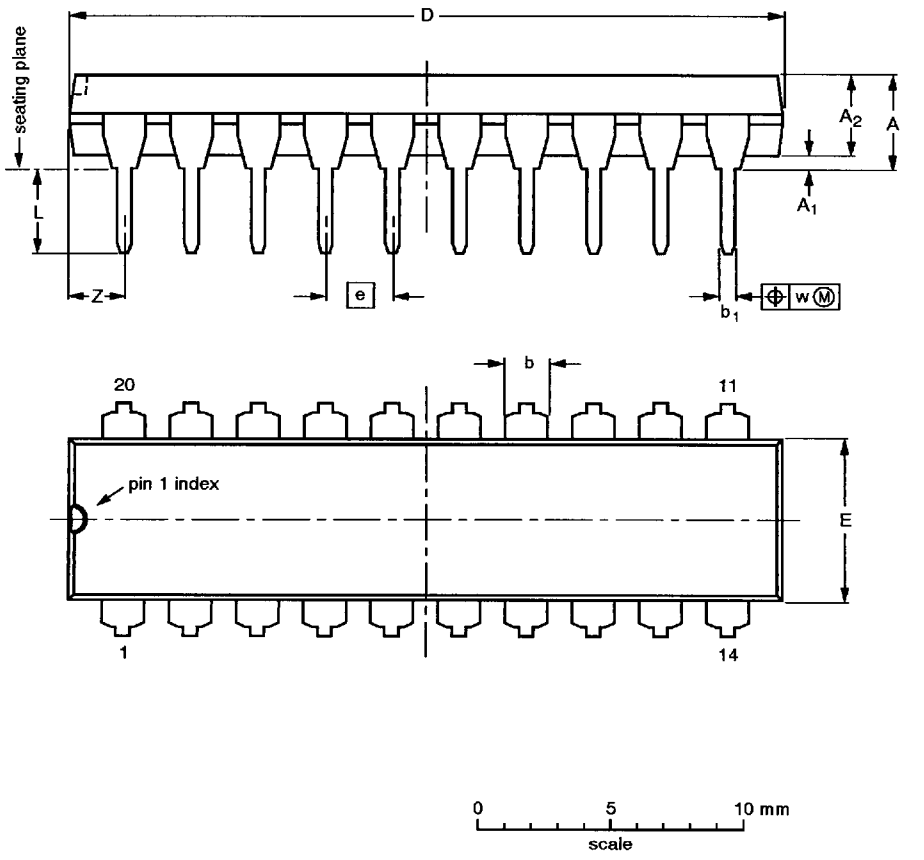
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SP00397B

Table 5. Thermal Impedances

PACKAGES	Θ_{JA}
20-pin plastic dual in-line package	68°C/W
20-pin plastic leaded chip carrier	72°C/W
20-pin small outline package	88°C/W

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS

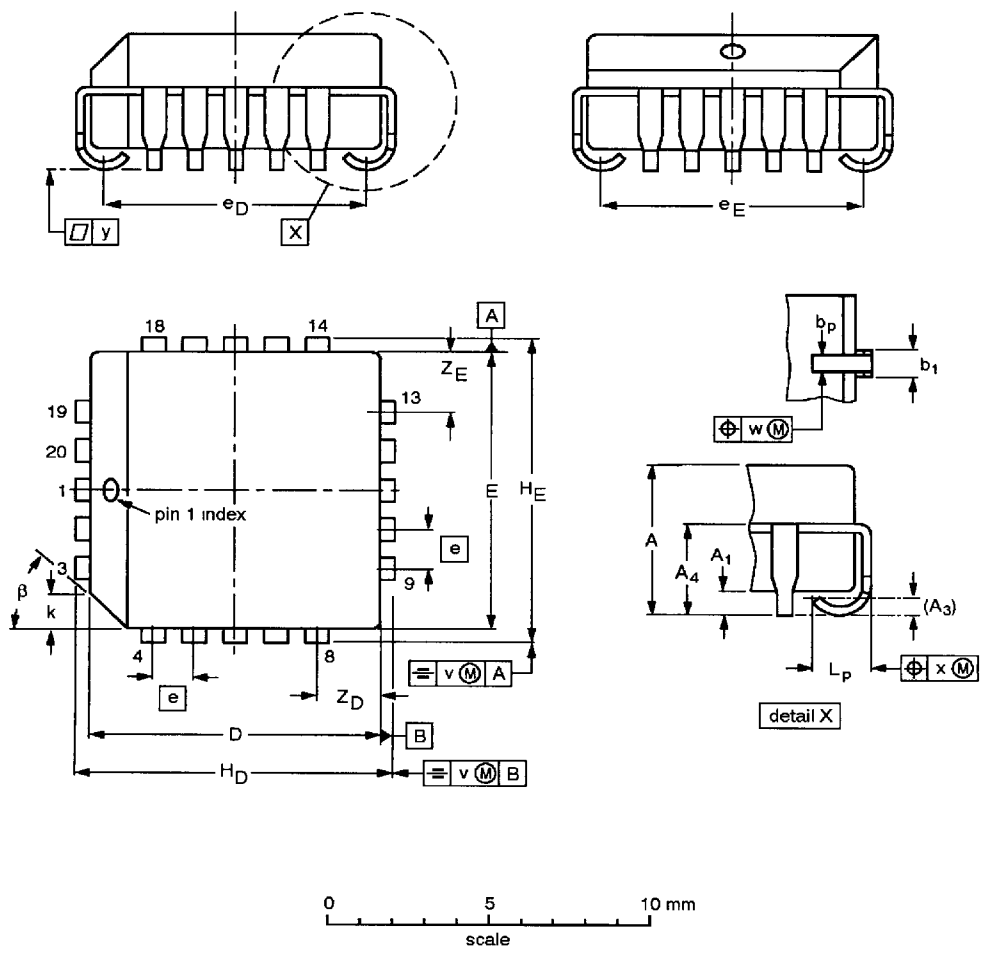
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-03-11

PLCC20: plastic leaded chip carrier; 20 leads **SOT380-1**



DIMENSIONS

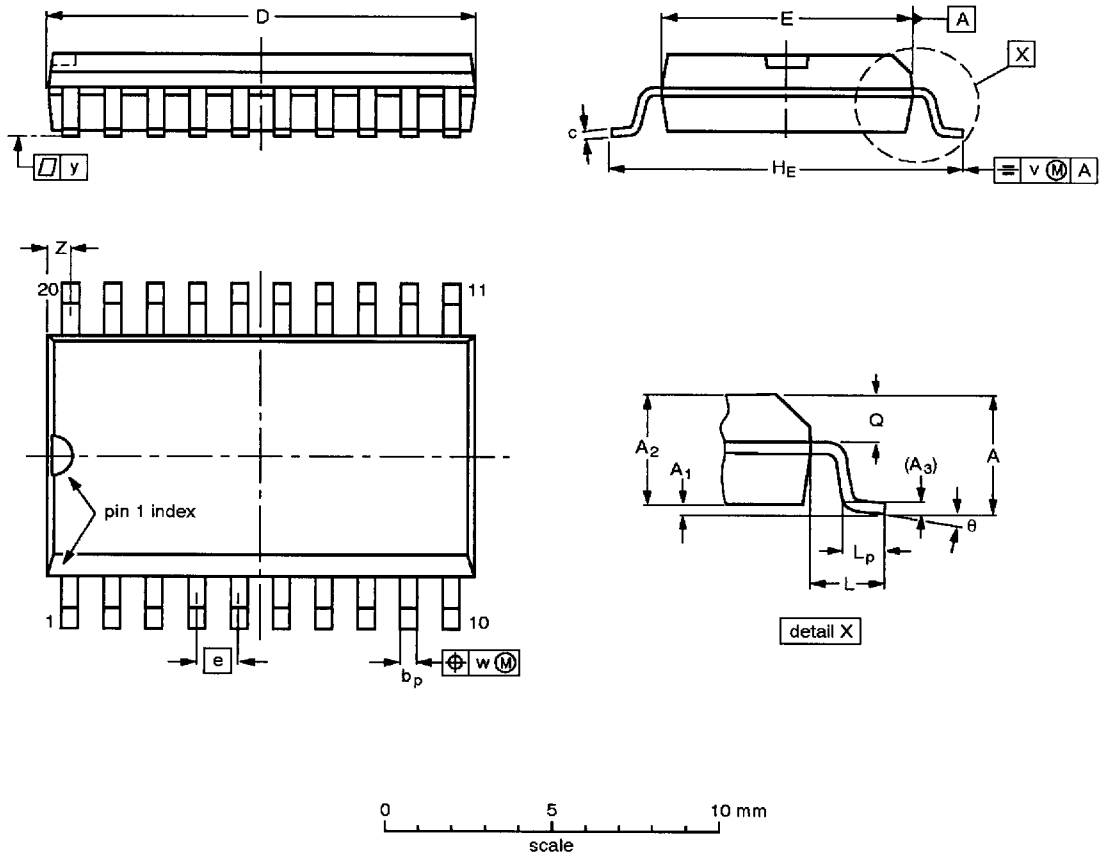
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~92-11-17~~ 95-02-25

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS

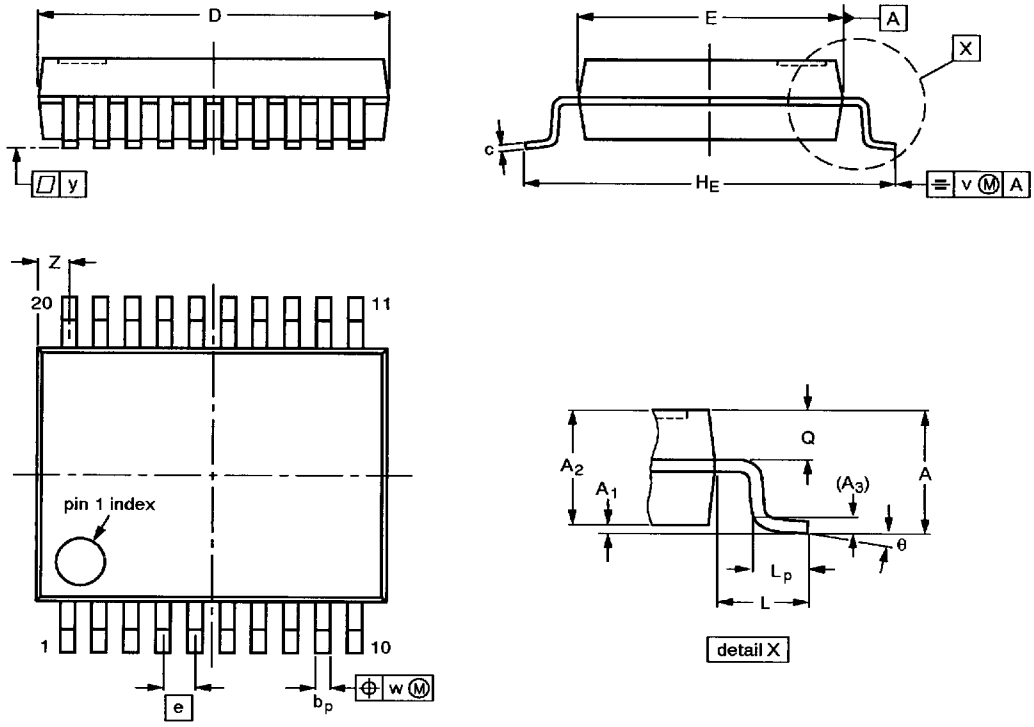
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°

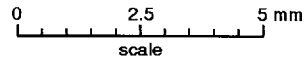
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04