Features

512Kx32 bit CMOS Static
Random Access Memory

- Access Times: 15, 17 and 20ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package

- 72 Pin ZIP, No. 173
- 72 lead SIMM, No. 174
- Common Data Inputs and Outputs

Single +3.3V (±10%) Supply Operation

512Kx32 Static RAM CMOS, High Speed Module

The EDI8G32512V is a high speed 16 megabit Static RAM module organized as 512K words by 32 bits. This module is constructed from four 512Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables ($\overline{E}$Ø-$\overline{E}$3) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8G32512V is offered in gold plated 72 pin ZIP and 72 lead SIMM packages, which enable 16 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 3.3V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD1- PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

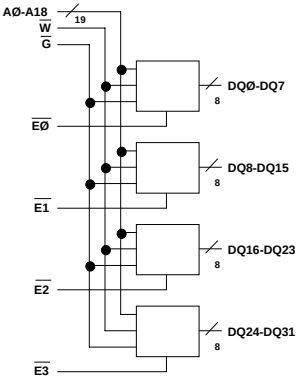
Pin Configurations and Block Diagram

NC	2	1	NC
PD4	4	3	PD3
PD1	6	5	VSS
DQØ	8	7	PD2
DQ1	10	9	DQ8
DQ2	12	11	DQ9
DQ3	14	13	DQ10
VCC	16	15	DQ11
A7	18	17	AØ
A8	20	19	A1
A9	22	21	A2
DQ4	24	23	DQ12
DQ5	26	25	DQ13
DQ6	28	27	DQ14
DQ7	30	29	DQ15
W	32	31	VSS
A14	34	33	A15
EØ	36	35	E1
E2	38	37	E3
A16	40	39	A17
VSS	42	41	G
DQ16	44	43	DQ24
DQ17	46	45	DQ25
DQ18	48	47	DQ26
DQ19	50	49	DQ27
A10	52	51	A3
A11	54	53	A4
A12	56	55	A5
A13	58	57	VCC
DQ20	60	59	A6
DQ21	62	61	DQ28
DQ22	64	63	DQ29
DQ23	66	65	DQ30
VSS	68	67	DQ31
NC	70	69	A18
NC	72	71	NC

PD1, PD2,PD4 = Open
PD3 = VSS

Pin Names

AØ-A18	Address Inputs
$\overline{E}$Ø-$\overline{E}$3	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ31	Common Data Input/Output
VCC	Power (+3.3V±10%)
VSS	Ground
NC	No Connection



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 4.6V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	Vcc +0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle			640	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$VIH, VIN$\leq$VIL or VIN $\geq$VIH			200	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq$VCC-0.2V			40	mA
CMOS		VIN$\geq$VCC-0.2V or VIN $\leq$ 0.2V				
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±20	µA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC2/ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	45	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	45	pF

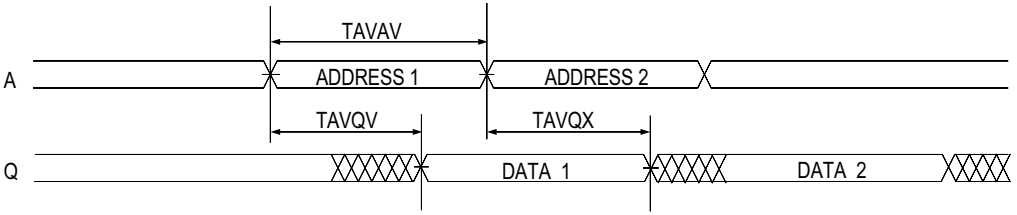
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

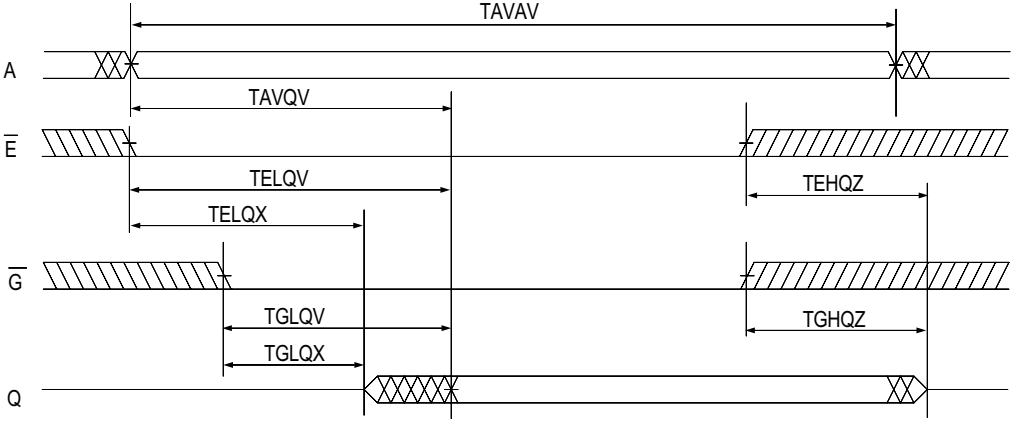
	Symbol		15ns		17ns		20ns	
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Read Cycle Time	TAVAV	TRC	15		17		20	
Address Access Time	TAVQV	TAA		15		17		20
Chip Enable Access	TELQV	TACS		15		17		20
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3	
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		7		7		10
Output Hold from Address Change	TAVQX	TOH	3		3		3	
Output Enable to Output Valid	TGLQV	TOE		7		7		8
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0	
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		7		7		8

Notes 1. Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

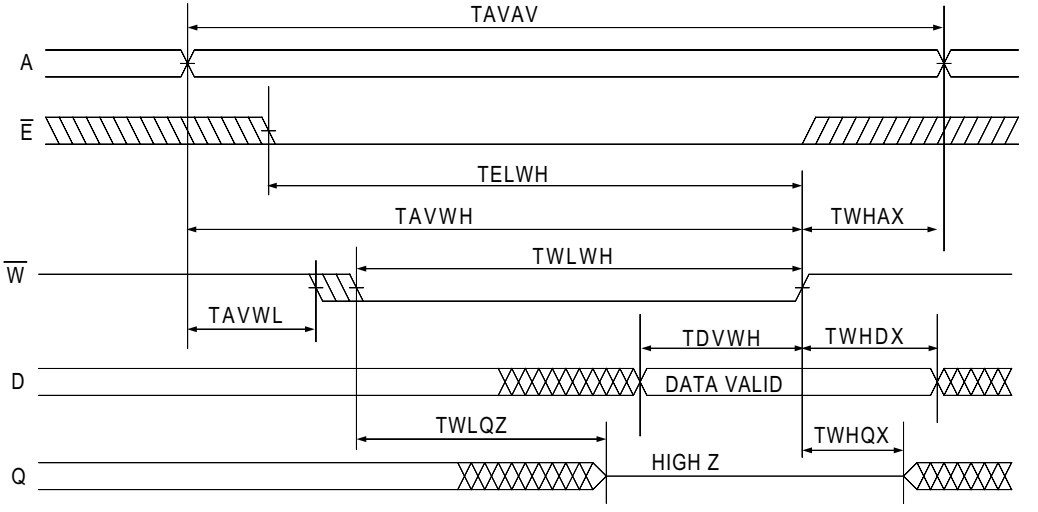


AC Characteristics Write Cycle

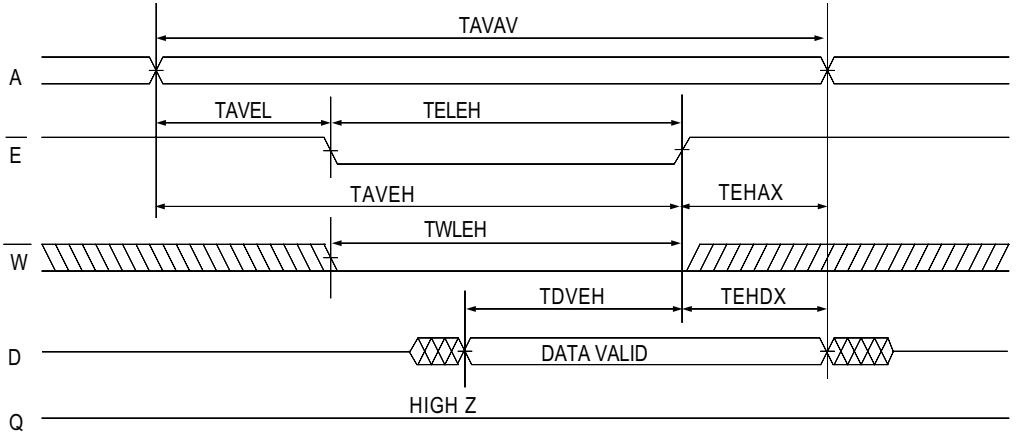
	Symbol		15ns		17ns		20ns	
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Cycle Time	TAVAV	TWC	15		17		20	
Chip Enable to End of Write	TELWH	TCW	10		12		15	
	TWLEH	TCW	10		12		15	
Address Setup Time	TAVWL	TAS	0		0		0	
	TAVEL	TAS	0		0		0	
Address Valid to End of Write	TAVWH	TAW	10		12		15	
	TAVEH	TAW	10		12		15	
Write Pulse Width	TWLWH	TWP	10		12		15	
	TELEH	TWP	10		12		15	
Write Recovery Time	TWHAX	TWR	0		0		0	
	TEHAX	TWR	0		0		0	
Data Hold Time	TWHDX	TDH	0		0		0	
	TEHDX	TDH	0		0		0	
Write to Output in High Z (1)	TWLQZ	TWHZ	0	7	0	8	0	8
Data to Write Time	TDVWH	TDW	7		8		9	
	TDVEH	TDW	7		8		9	
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		3	

Notes: 1. Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

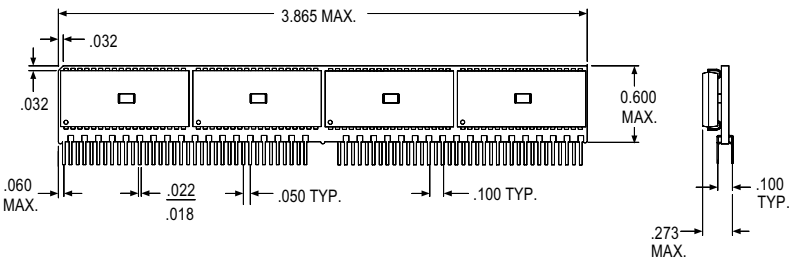
Part Number	Speed (ns)	Package No.
EDI8G32512V15MMC	15	174
EDI8G32512V17MMC	17	174
EDI8G32512V20MMC	20	174

Part Number	Speed (ns)	Package No.
EDI8G32512V15MZC	15	173
EDI8G32512V17MZC	17	173
EDI8G32512V20MZC	20	173

Package Description

Package No. 173
72 Pin ZIP

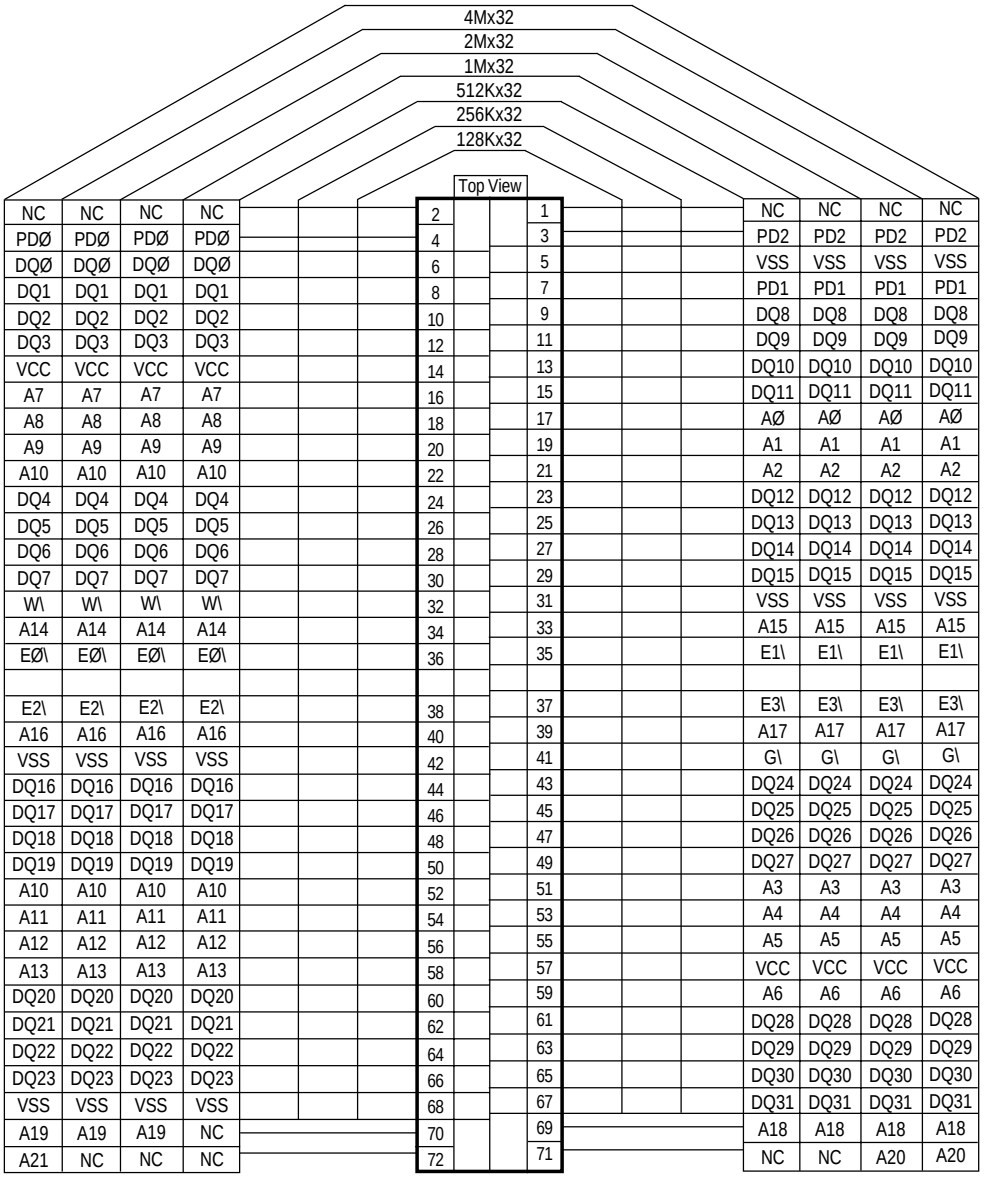
(Gold Plated Leads)



Package No. 174
72 lead SIMM

(Gold Plated Contacts)

X32 Pinout Map for 72 pin ZIP
Package Configurations



NC	NC	NC	NC	2			1	NC	NC	NC	NC
PDØ	PDØ	PDØ	PDØ	4			3	PD2	PD2	PD2	PD2
DQØ	DQØ	DQØ	DQØ	6			5	VSS	VSS	VSS	VSS
DQ1	DQ1	DQ1	DQ1	8			7	PD1	PD1	PD1	PD1
DQ2	DQ2	DQ2	DQ2	10			9	DQ8	DQ8	DQ8	DQ8
DQ3	DQ3	DQ3	DQ3	12			11	DQ9	DQ9	DQ9	DQ9
VCC	VCC	VCC	VCC	14			13	DQ10	DQ10	DQ10	DQ10
A7	A7	A7	A7	16			15	DQ11	DQ11	DQ11	DQ11
A8	A8	A8	A8	18			17	AØ	AØ	AØ	AØ
A9	A9	A9	A9	20			19	A1	A1	A1	A1
A10	A10	A10	A10	22			21	A2	A2	A2	A2
DQ4	DQ4	DQ4	DQ4	24			23	DQ12	DQ12	DQ12	DQ12
DQ5	DQ5	DQ5	DQ5	26			25	DQ13	DQ13	DQ13	DQ13
DQ6	DQ6	DQ6	DQ6	28			27	DQ14	DQ14	DQ14	DQ14
DQ7	DQ7	DQ7	DQ7	30			29	DQ15	DQ15	DQ15	DQ15
W\	W\	W\	W\	32			31	VSS	VSS	VSS	VSS
A14	A14	A14	A14	34			33	A15	A15	A15	A15
EØ\	EØ\	EØ\	EØ\	36			35	E1\	E1\	E1\	E1\
E2\	E2\	E2\	E2\	38			37	E3\	E3\	E3\	E3\
A16	A16	A16	A16	40			39	A17	A17	A17	A17
VSS	VSS	VSS	VSS	42			41	G\	G\	G\	G\
DQ16	DQ16	DQ16	DQ16	44			43	DQ24	DQ24	DQ24	DQ24
DQ17	DQ17	DQ17	DQ17	46			45	DQ25	DQ25	DQ25	DQ25
DQ18	DQ18	DQ18	DQ18	48			47	DQ26	DQ26	DQ26	DQ26
DQ19	DQ19	DQ19	DQ19	50			49	DQ27	DQ27	DQ27	DQ27
A10	A10	A10	A10	52			51	A3	A3	A3	A3
A11	A11	A11	A11	54			53	A4	A4	A4	A4
A12	A12	A12	A12	56			55	A5	A5	A5	A5
A13	A13	A13	A13	58			57	VCC	VCC	VCC	VCC
DQ20	DQ20	DQ20	DQ20	60			59	A6	A6	A6	A6
DQ21	DQ21	DQ21	DQ21	62			61	DQ28	DQ28	DQ28	DQ28
DQ22	DQ22	DQ22	DQ22	64			63	DQ29	DQ29	DQ29	DQ29
DQ23	DQ23	DQ23	DQ23	66			65	DQ30	DQ30	DQ30	DQ30
VSS	VSS	VSS	VSS	68			67	DQ31	DQ31	DQ31	DQ31
A19	A19	A19	NC	70			69	A18	A18	A18	A18
A21	NC	NC	NC	72			71	NC	NC	A20	A20