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BCM2085
PRODUCT Brief

65-nm CMOS DigRF EDGE CELLULAR TRANSCEIVER

FEATURES

- Quad-band CMOS EDGE/GPRS RF transceiver

- Supports multislot GPRS and EDGE operation up to Class 34

- Innovative polar transmit architecture

- GMSK and 8-PSK TX modulators and ramp DAC

- Four integrated receive LNAs

- Digital low-IF receive architecture including digital filter

- $\Sigma\Delta$ ADCs for conversion of baseband receive signal

- Fully integrated $\Sigma\Delta$ fractional-N synthesizer including VCOs and loop filters

- Integrated digitally-controlled crystal oscillator (DCXO)

- DigRF compatible (v1.12) baseband interface

- Autonomous, real-time radio calibration

- Compact 49-pin FBGA package (4 mm × 4 mm)

SUMMARY OF BENEFITS

- Advanced 65-nm standard digital CMOS design for lowest power consumption

- Highly integrated design enables lowest cost, smallest area DigRF EDGE solution

- Polar transmitter architecture for EDGE enables use of standard linear power amplifiers to simplify

- No SAW filters in the transmit path

- No baseband intervention required for radio calibration

APPLICATIONS

- Mobile handsets and smartphones

BCM2085 Block Diagram

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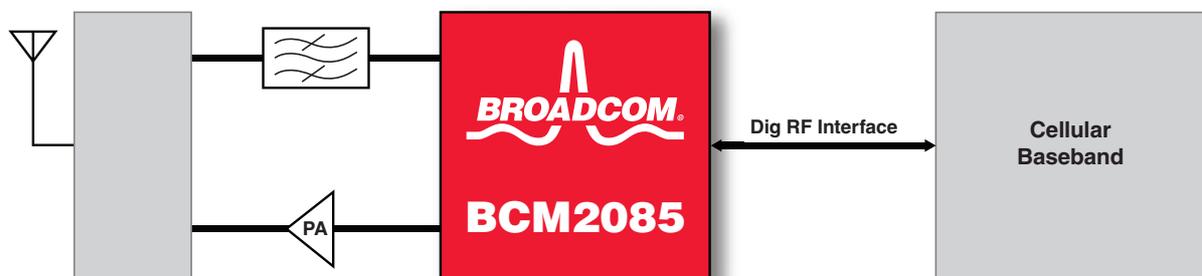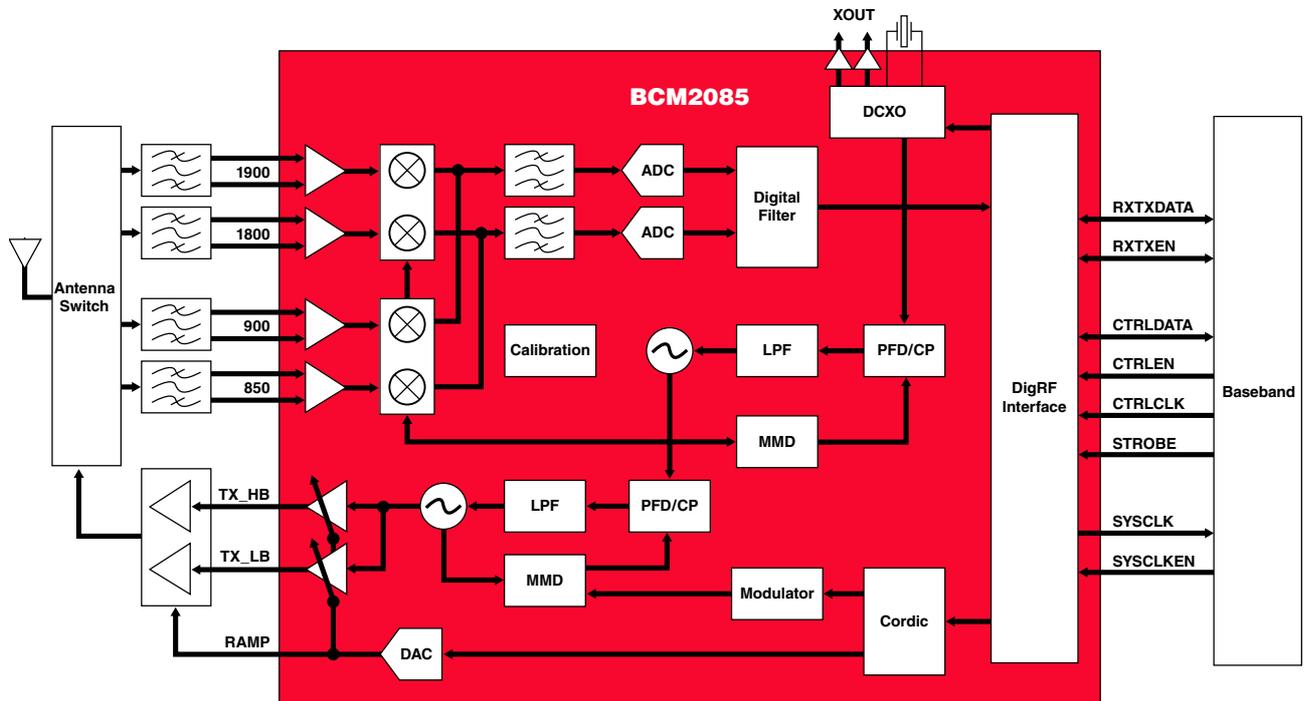
BCM2085 Reference Design

The BCM2085 is a 65-nm CMOS single chip quad-band GSM/GPRS/ EDGE RF transceiver for GSM850/EGSM900/DCS1800/PCS1900 voice and data applications. The monolithic die, designed on a 65-nm pure digital CMOS technology, integrates the transceiver core as well as the analog functionality to provide a digital interface compliant with the DigRF v1.12 standard. The BCM2085 offers a low power, highly-integrated and low cost EDGE RF solution in a 4 mm x 4 mm package. It is the industry's smallest DigRF-compliant EDGE transceiver.

The BCM2085 delivers outstanding RF performance while achieving low power consumption through innovative architecture and circuit design. The RF transceiver draws upon Broadcom's extensive experience in pure digital CMOS radio design. Proprietary, autonomous, real-time calibrations within the radio ensure the BCM2085 delivers critical radio performance while using pure digital CMOS. Integration of the voltage controlled oscillators, synthesizers, and loop filters minimizes the board area and external component count.

A novel polar transmit architecture ensures the low transmit power consumption and eliminates any SAW filters in the transmit path. The transmitter employs a $\Sigma\Delta$ modulator for GMSK and a polar modulator for 8PSK. The transmit modulators and ramp generator are also integrated. This architecture enables the use of standard linear power amplifiers to accelerate time to market through ease of design while ensuring a robust manufacturing solution.

The receiver is based on a proven low-IF architecture providing suppression of DC offsets avoiding the issues related to direct conversion receivers. Four integrated LNAs permit quad-band implementations. Digitization of the receive signal is performed with $\Sigma\Delta$ ADCs followed by internal digital channel filtering.

The BCM2085 features an integrated $\Sigma\Delta$ fractional-N synthesizer to achieve fast settling times supporting multi-slot GPRS/EDGE operation up to Class 34. The reference frequency for the synthesizer is supplied from the internal digitally-controlled crystal oscillator (DCXO) allowing the use of a low cost crystal. Two buffered reference frequency outputs are also provided to supply other devices in the system.

Compatible with all DigRF-compliant basebands, the BCM2085 is the ideal choice to easily lower the cost and size of EDGE handsets and smartphones.

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