



INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEELTM253

CMOS Programmable Electrically Erasable Logic Device

Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
 - 35mA + 1mA/MHz max
- **COMPATIBLE PERFORMANCE**
 - t_{PD} = 30ns max, t_{OE} = 30ns max
- **ARCHITECTURAL FLEXIBILITY**
 - 8 inputs and 10 I/Os
 - Programmable AND/OR arrays with 42 product terms/10 sum terms
- **EE REPROGRAMMABILITY**
 - Superior programming and functional yield
 - Low cost windowless package
 - Erases and programs in seconds
- **FPLA ARCHITECTURE**
- **SUPERSET REPLACEMENT FOR PLS153**
 - Ten additional product terms
 - Output-enable terms in OR array
 - Signature word
 - Foolproof design security
- **APPLICATION VERSATILITY**
 - Replace random SSI/MSI logic
 - Create customized comparators, multiplexers, encoders, converters, etc.
- **DEVELOPMENT SUPPORT**
 - Third-party software and programmers
 - ICT PEEL Development System and software.

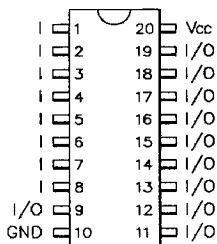
General Description

The ICT PEEL253 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL253 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogrammability of the PEEL253 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

The PEEL253 provides both a programmable AND array and a programmable OR array. It offers superset compatibility with the bipolar PLS153 with several architectural enhancements, including: output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL253 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL253 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

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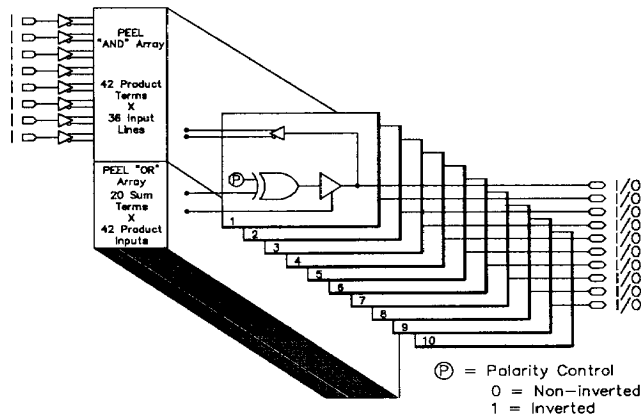
Pin Configuration



Pin Names

I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

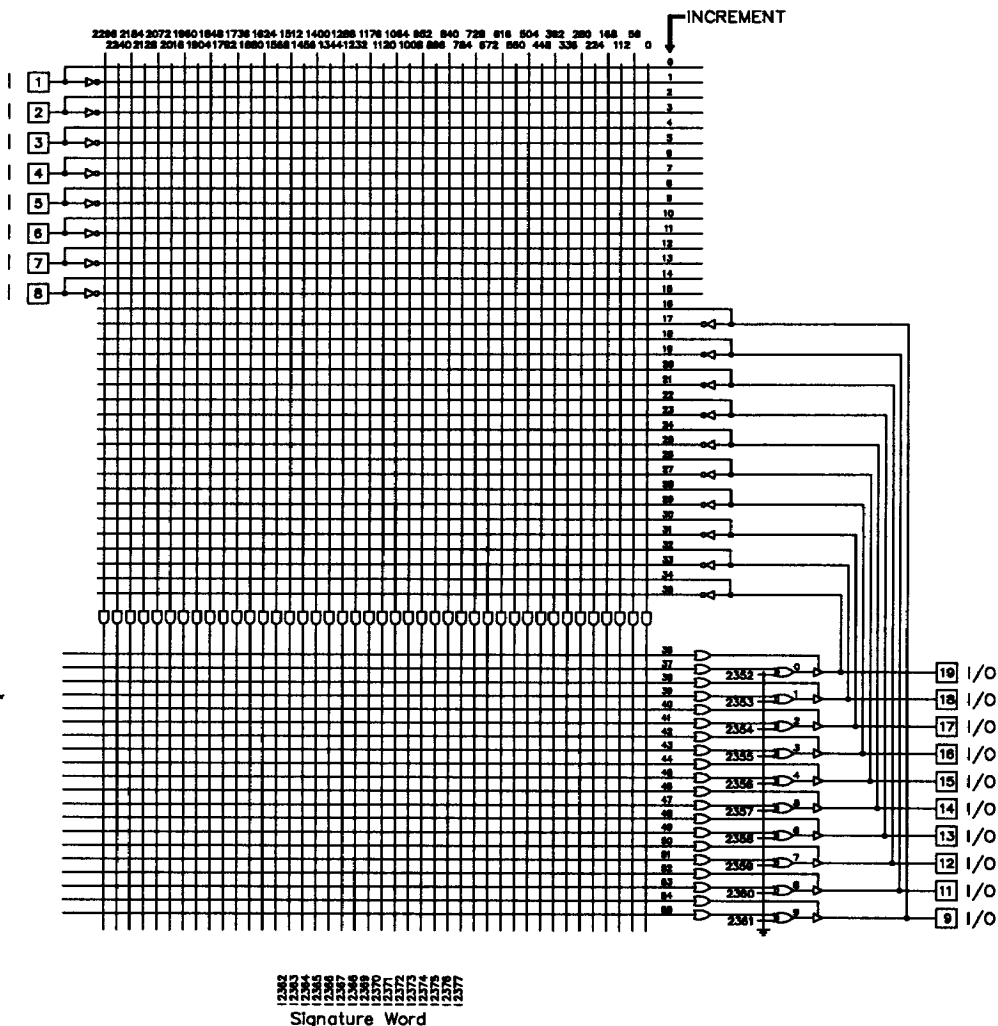
Block Diagram



Ⓟ = Polarity Control
0 = Non-inverted
1 = Inverted



JEDEC Programming Cell Number = Product Term Number + Increment



PEEL253 Logic Array Diagram



Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to GND	– 0.6 to +7.0	V
V _{IO}	Voltage Applied to Any Pin ⁸	Relative to GND ¹	– 0.6 to V _{CC} + 0.6	V
T _A	Ambient Temp, Power Applied		– 10 to + 85	°C
T _{ST}	Storage Temperature		– 65 to + 150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
T _A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		– 0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = – 3.2mA	2.4		V
V _{OHC}	Output HIGH Voltage CMOS	V _{CC} = Min, I _{OH} = – 10μA	V _{CC} – 0.1		V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 8mA ⁴		0.5	V
V _{OLC}	Output LOW Voltage CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
I _L	Input Leakage Current	V _{CC} = Max, GND ≤ V _I ≤ V _{CC}		10	μA
I _{OS}	Output Short Circuit Current ²	V _{CC} = Max, V _O =GND	– 30	– 90	mA
I _{OZ}	Output Leakage Current	I/O = High Impedance V _{CC} = Max, GND ≤ V _O ≤ V _{CC}		± 10	μA
I _{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V _{CC} ³		35	mA
I _{CCAC}	Power Supply Current, Active, CMOS Interface	V _{IN} = V _{IL} or V _{IH} . All inputs, feedback, and I/Os switching ³		I _{CCSC} + 1mA/MHz	mA
I _{CCST}	Power Supply Current Standby, TTL Interface	V _{IN} = V _{IL} or V _{IH} ³		45	mA
I _{CCAT}	Power Supply Current, Active, TTL Interface	V _{IN} = V _{IL} or V _{IH} . All inputs, feedback, and I/Os switching ³		I _{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested.

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C V _{CC} = 5.0V, f = 1kHz		6	pF
C _{OUT}	Output Capacitance			12	pF

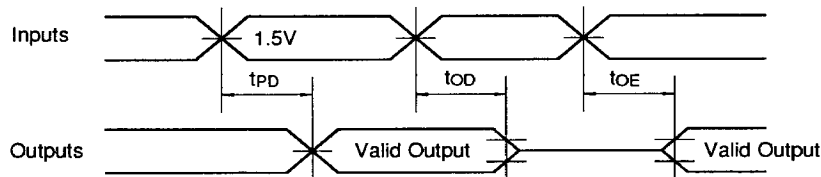


A.C. Electrical Characteristics

Over the Operating Range ^{5,9}

Symbol	Parameter	PEEL253-30		PEEL253-35		PEEL253-40		Unit
		Min	Max	Min	Max	Min	Max	
t _{PD}	Propagation Delay, Input to Output		30		35		40	ns
t _{OE}	Input to Output Enable ⁶		30		35		40	ns
t _{OD}	Input to Output Disable ^{6,7}		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is $-0.5V$, however, inputs may undershoot to $-2.0V$ for periods less than 30ns.
2. Test one output at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. $V_{OL} = 0.5V$ @ $I_{OL} = 15mA$ with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less from the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified); and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with $C_L = 5pF$.
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL253 program/verify specifications.
9. PEEL device test loads are specified at the end of this section..