

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89140 Series

MB89145/146 and MB89P147/PV140

DESCRIPTION

The MB89140 series is a line of single-chip microcontrollers that use the F²MC*-8L CPU core which can operate at low voltage but at high speed. The MB89140 series contains a variety of peripheral functions, such as timers, a serial interface, an A/D converter, and an external interrupt. The MB89140 series is applicable to a wide range of applications from welfare products to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

FEATURES

- Minimum execution time: 0.5 μs/8-MHz oscillation
- F²MC-8L family CPU core

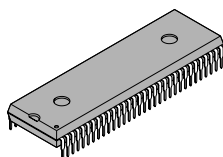
Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Test and branch instructions
- Bit manipulation instructions, etc.

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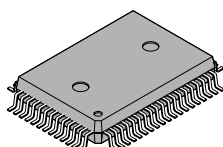
PACKAGE

64-pin Plastic SH-DIP



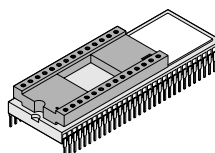
(DIP-64P-M01)

64-pin Plastic QFP



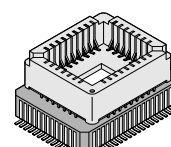
(FPT-64P-M06)

64-pin Ceramic MDIP



(MDP-64C-P02)

64-pin Ceramic MQFP



(MQP-64C-P01)

MB89140 Series

(Continued)

- Low-voltage operation (when an A/D converter is not used)
- Low current consumption (compatible with dual-clock system)
- High-voltage ports on chip
- Five types of timers
 - 8-bit PWM timer (also usable as a reload timer)
 - 12-bit MPG timer (also usable as a PPG output, PWM output, and reload timer)
 - 8/16-bit timer (also usable as two 8-bit timers)
 - 21-bit time-base timer
- One serial interface
 - Swichable transfer direction allows communication with various equipment.
- 10-bit A/D converter: 12 channels
 - Successive approximation type
- External interrupt: 2 channels
 - Two channels are independent and capable of wake-up from low-power consumption modes. (Rising edge, falling edge/both edges selectability)
 - 0.3 V to +7.0 V can be applied to INT1 (N-ch open-drain)
- Low-power consumption modes
 - Stop mode (Oscillation stops to minimize the current consumption.)
 - Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
 - Subclock mode
 - Watch mode
- Reset output and power-on reset selectability

MB89140 Series

■ PRODUCT LINEUP

Part number	MB89145	MB89146	MB89P147	MB89PV140
Parameter				
Classification	Mass production products (mask ROM products)		One-time PROM/ EPROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	16 K × 8 bits (internal mask ROM)	24 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM)	32 K × 8 bits (external ROM)
RAM size	512 × 8 bits	768 × 8 bits	1 K × 8 bits	
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.5 μs/8 MHz to 8.0 μs/8 MHz, 61 μs/32.768 kHz Interrupt processing time: 4.5 μs/8 MHz to 72.0 μs/8 MHz, 562.5 μs/32.768 kHz Note: The above times change according to the gear function.			
Ports	High-voltage output port (P-ch open-drain): 8 (P60 to P67, for heavy current) 16 (P40 to P47, P50 to P57 for low current) Buzzer output (P-ch open-drain, high-voltage): 1 (heavy current) Output ports (CMOS): 4 (P20 to P23) Input ports (CMOS): 2 (P70 and P71, function as X0A and X1A pins when dual-clock system is used.) I/O ports (CMOS): 23 (P00 to P07, P10 to P17, P30, and P32 to P37) I/O ports (N-ch open-drain): 1 (P31) Total: 55			
Clock timer	21 bits × 1 (in main clock mode), 15 bits × 1 (at 32.768 kHz)			
8-bit PWM timer (timer 1)	8-bit timer operation (toggled output capable, operating clock: 1, 2, 8, 16 system clock cycles) 8-bit resolution PWM operation (conversion cycle: 128 μs to 2.0 ms at 8.0-MHz oscillation, and highest gear speed)			
12-bit MPG (timer 4)	12-bit resolution PWM operation (maximum conversion cycle of 2048.4 μs to 16.4 ms at 8.0 MHz-oscillation, and highest gear speed) 12-bit resolution reload timer operation (toggled output capable) 12-bit resolution PPG operation (minimum resolution of 0.5 μs at 8.0-MHz oscillation, and highest gear speed)			
8/16-bit timer counter (timer 2, 3)	8/16-bit timer operation (operating clock, internal clock, external trigger) 8/16-bit event counter operation (Rising edge/falling edge/both edges selectability)			

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MB89140 Series

(Continued)

Part number	MB89145	MB89146	MB89P147	MB89PV140
Parameter				
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 4, 8, 16 system clock cycles)			
10-bit A/D converter	10-bit resolution × 12 channels A/D conversion mode (conversion time of 16.5 μs/8 MHz, and highest gear speed) Sense mode (conversion time of 9.0 μs/8 MHz, and highest gear speed) External activation capable			
External interrupt	2 independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge/both edges selectability Built-in analog noise canceller Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)			
Standby mode	Sleep mode, stop mode, watch mode, and subclock mode			
Process	CMOS			
Operating voltage*	2.7 V to 6.0 V			
EPROM for use				MBM27C256A-20TV MBM27C256A-20CZ

* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89145 MB89146 MB89P147	MB89PV140
DIP-64P-M01	○	×
DIP-64C-A06	×	×
FPT-64P-M06	○	×
MDP-64C-P02	×	○
MQP-64C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see section “■ Package Dimensions.”

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P147, the program area starts from address 8007_H but on the MB89PV140 starts from 8000_H.
(On the MB89P147, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV140, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P147.)
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV140, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.
However, the current consumption in sleep/stop modes is the same. (For more information, see section “■ Electrical Characteristics.”)

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product. Before using options check section “■ Mask Options.”

Take particular care on the following points:

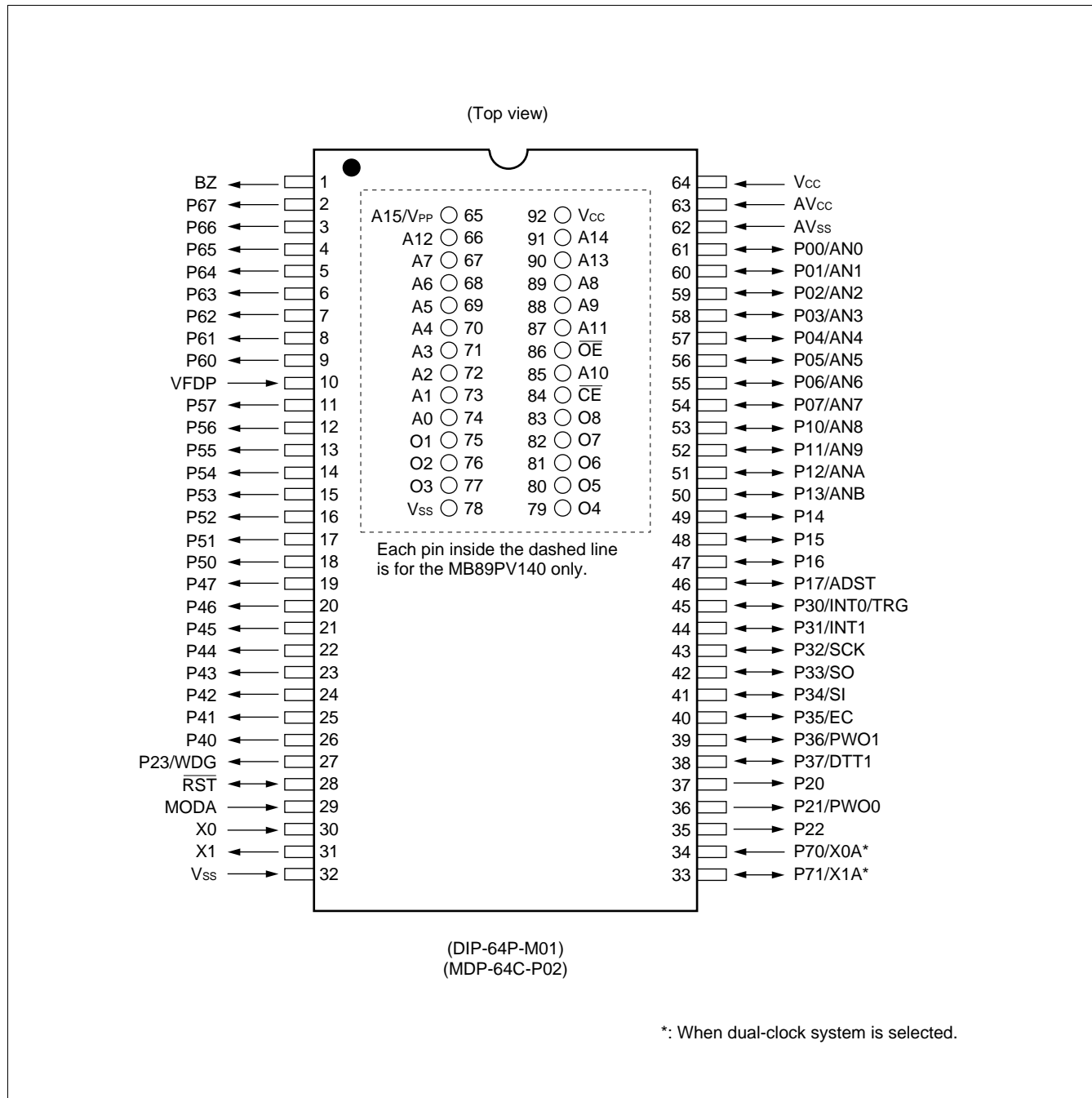
- Options are fixed on the MB89PV140.
- On the MB89P147, MB89145, and MB89146, the pull-down resistor option can either be selected for all affected pins, or for no pin; it is not possible to specify the pull-down resistor option for individual pins.

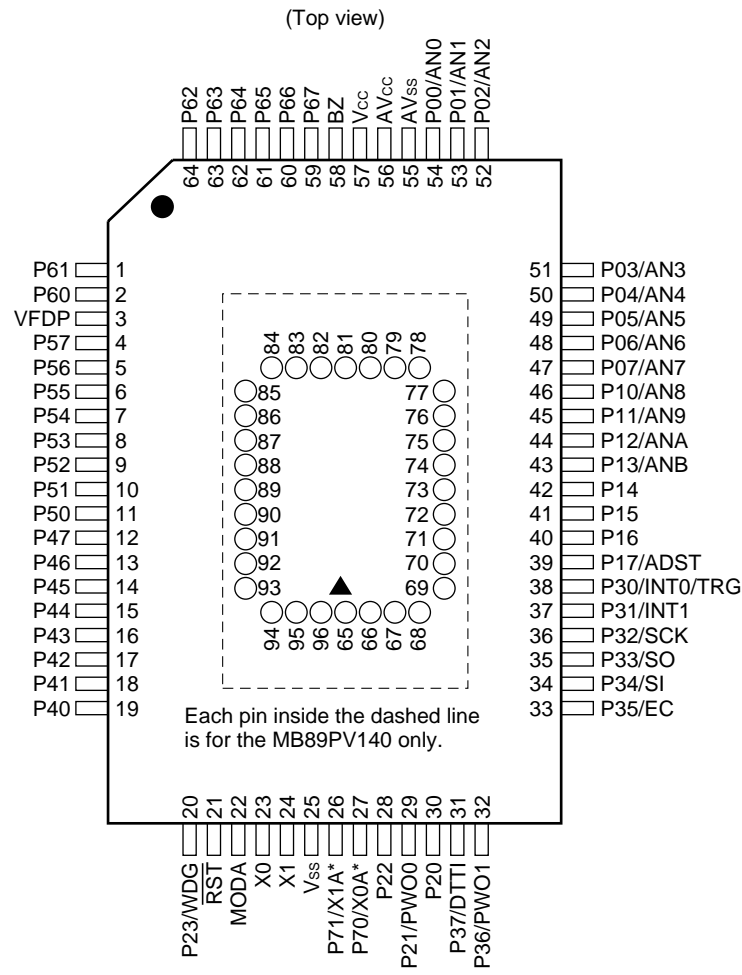
4. Subclock Oscillation Feedback Resistor

A built-in oscillation feedback resistor is provided for the subclock oscillator pin on the MB89PV140, but it is not provided for the MB89145, MB89146, MB89P147. Therefore these products should be connected to an external oscillation feedback resistor.

MB89140 Series

■ PIN ASSIGNMENT





(FPT-64P-M06)
(MQP-64C-P01)

*: When dual-clock system is selected.

• Pin assignment on package top (MB89PV140 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	\overline{OE}
66	A15/ V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	\overline{CE}	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

MB89140 Series

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SDIP ^{*1} MDIP ^{*2}	QFP ^{*3} MQFP ^{*4}			
30	23	X0	A	Main clock crystal oscillator pins
31	24	X1		
29	22	MODA	C	Operating mode selection pin Connect directly to V _{SS} in normal operation. This pin functions as the V _{PP} pin in EPROM products.
28	21	$\overline{\text{RST}}$	D	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source when the option is set. The internal circuit is initialized by the input of “L”. This pin is with a noise canceller.
54 to 61	47 to 54	P07/AN7 to P00/AN0	G	General-purpose I/O ports The input is a hysteresis input type and with a built-in noise canceller. Although these ports also serve as an analog input, analog input does not pass through the hysteresis input noise canceller.
46	39	P17/ADST	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as an A/D converter external activation.
47 to 49	40 to 42	P16 to P14	J	General-purpose I/O ports The input is a hysteresis input type and with a built-in noise canceller.
50 to 53	43 to 46	P13/ANB to P10/AN8	G	General-purpose I/O ports The input is a hysteresis input type and with a built-in noise canceller. Although these ports also serves as an analog input, analog input does not pass through the hysteresis input noise canceller.
34, 33	27, 26	P70/X0A, P71/X1A	B/K	General-purpose I/O ports with a built-in noise canceller (single-clock operation) Function as subclock crystal oscillator pins. (dual-clock operation)
35	28	P22	E	General-purpose output port
27	20	P23/WDG	E	General-purpose output port Also serves as a watchdog output.
36	29	P21/PW00	E	General-purpose output port Also serves as the PWM output for the 8-bit PWM timer.
37	30	P20	E	General-purpose output port

(Continued)

- *1: DIP-64P-M01
- *2: MDP-64C-P02
- *3: FPT-64P-M06
- *4: MQP-64C-P01

MB89140 Series

Pin no.		Pin name	Circuit type	Function
SDIP ^{*1} MDIP ^{*2}	QFP ^{*3} MQFP ^{*4}			
38	31	P37/DTTI	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. When overcurrent is detected, the 12-bit MPG output can be inactivated by the external edge input.
39	32	P36/PWO1	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as a 12-bit MPG output.
40	33	P35/EC	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as the external clock input for the 8/16-bit timer/counter.
41	34	P34/SI	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as the serial data input for the 8-bit serial interface.
42	35	P33/SO	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as the serial data output for the 8-bit serial interface.
43	36	P32/SCK	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serves as the serial transfer clock for the 8-bit serial interface.
44	37	P31/INT1	F	General-purpose I/O port The output is an N-ch open-drain type. The input is a hysteresis input type and with a built-in noise canceller. Also serves as an external interrupt. The interrupt input is also a hysteresis input type and with a built-in noise canceller.
45	38	P30/INT0/TRG	J	General-purpose I/O port The input is a hysteresis input type and with a built-in noise canceller. Also serve as an external interrupt or as an MPG trigger input. The interrupt input is also a hysteresis input type and with a built-in noise canceller.
1	58	BZ	I	Buzzer output-only pin P-ch high-voltage open-drain output port
19 to 26, 11 to 18	12 to 19, 4 to 11	P47 to P40, P57 to P50	H	Low-current P-ch high-voltage open-drain output ports Products with and without a built-in pull-down resistor between these pins and the VFDP pin are provided.

(Continued)

*1: DIP-64P-M01

*2: MDP-64C-P02

*3: FPT-64P-M06

*4: MQP-64C-P01

MB89140 Series

(Continued)

Pin no.		Pin name	Circuit type	Function
SDIP*1 MDIP*2	QFP*3 MQFP*4			
2 to 9	59 to 64 1, 2	P67 to P60	H	Heavy-current P-ch high-voltage open-drain output port Products with and without a built-in pull-down resistor between these pins and the VFDP pin are provided.
10	3	VFDP	—	Voltage supply pin for connection to a pull-down resistor for ports 4, 5, and 6. In products without a built-in pull-down resistor and in the MB89PV140, this pin should be left open.
64	57	V _{cc}	—	Power supply pin
32	25	V _{ss}	—	Power supply (GND) pin
63	56	AV _{cc}	—	A/D converter power supply pin Use this pin at the same voltage as V _{cc} .
62	55	AV _{ss}	—	A/D converter power supply (GND) pin Use this pin at the same voltage as V _{ss} .

*1: DIP-64P-M01

*2: MDP-64C-P02

*3: FPT-64P-M06

*4: MQP-64C-P01

MB89140 Series

• External EPROM pins (MB89PV140 only)

Pin no.		Pin name	I/O	Function
SDIP ^{*3} MDIP ^{*4}	QFP ^{*1} MQFP ^{*2}			
65	66	A15/V _{PP}	O	"H" level output pin
66	67	A12	O	Address output pins
67	68	A7		
68	69	A6		
69	70	A5		
70	71	A4		
71	72	A3		
72	73	A2		
73	74	A1		
74	75	A0		
75	77	O1	I	Data input pins
76	78	O2		
77	79	O3		
78	80	V _{SS}	O	Power supply (GND) pin
79	82	O4	I	Data input pins
80	83	O5		
81	84	O6		
82	85	O7		
83	86	O8		
84	87	\overline{CE}	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	\overline{OE}	O	ROM output enable pin Outputs "L" at all times.
87	91	A11	O	Address output pins
88	92	A9		
89	93	A8		
90	94	A13		
91	95	A14		
92	96	V _{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

*1: DIP-64P-M01

*2: MDP-64C-P02

*3: FPT-64P-M06

*4: MQP-64C-P01

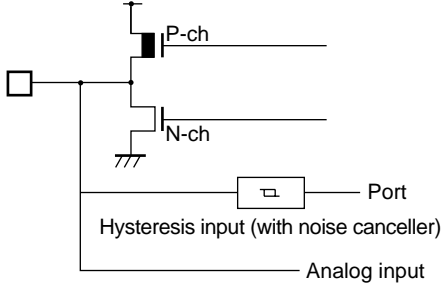
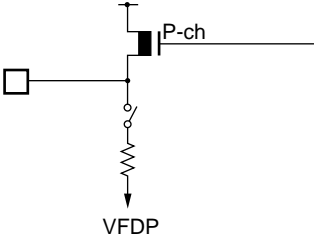
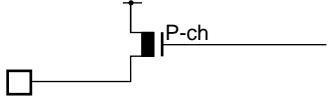
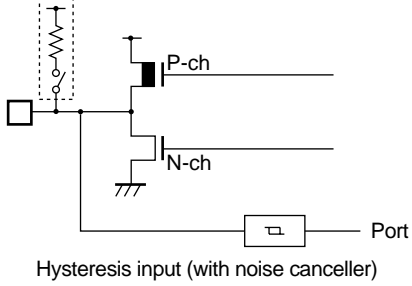
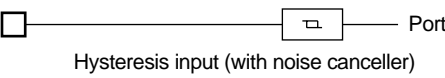
MB89140 Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>Standby control signal</p>	<ul style="list-style-type: none"> • Crystal or ceramic oscillation type (main clock) • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B	<p>Standby control signal</p>	<ul style="list-style-type: none"> • Crystal or ceramic oscillation type (subclock) • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V (The built-in feedback resistor is not provided except on the MB89PV140-102.)
C		
D	<p>Hysteresis input (with noise canceller)</p>	<ul style="list-style-type: none"> • At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • CMOS hysteresis input (with noise canceller)
E		<ul style="list-style-type: none"> • CMOS output
F	<p>Hysteresis input (with noise canceller)</p>	<ul style="list-style-type: none"> • N-ch open-drain output • CMOS hysteresis input (with noise canceller)

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Type	Circuit	Remarks
G		<ul style="list-style-type: none"> • CMOS output • CMOS hysteresis input (with noise canceller, except analog input)
H		<ul style="list-style-type: none"> • P-ch high-voltage open-drain output • Products with and without a built-in pull-down resistor are provided (except the MB89PV140).
I		<ul style="list-style-type: none"> • P-ch high-voltage open-drain output
J		<ul style="list-style-type: none"> • CMOS output • CMOS hysteresis input (with noise canceller) • Pull-up resistor optional
K		<ul style="list-style-type: none"> • CMOS hysteresis input (with noise canceller)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS} . (However, up to 7.0 V can be applied to P31/INT pin, regardless of V_{CC})

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P147

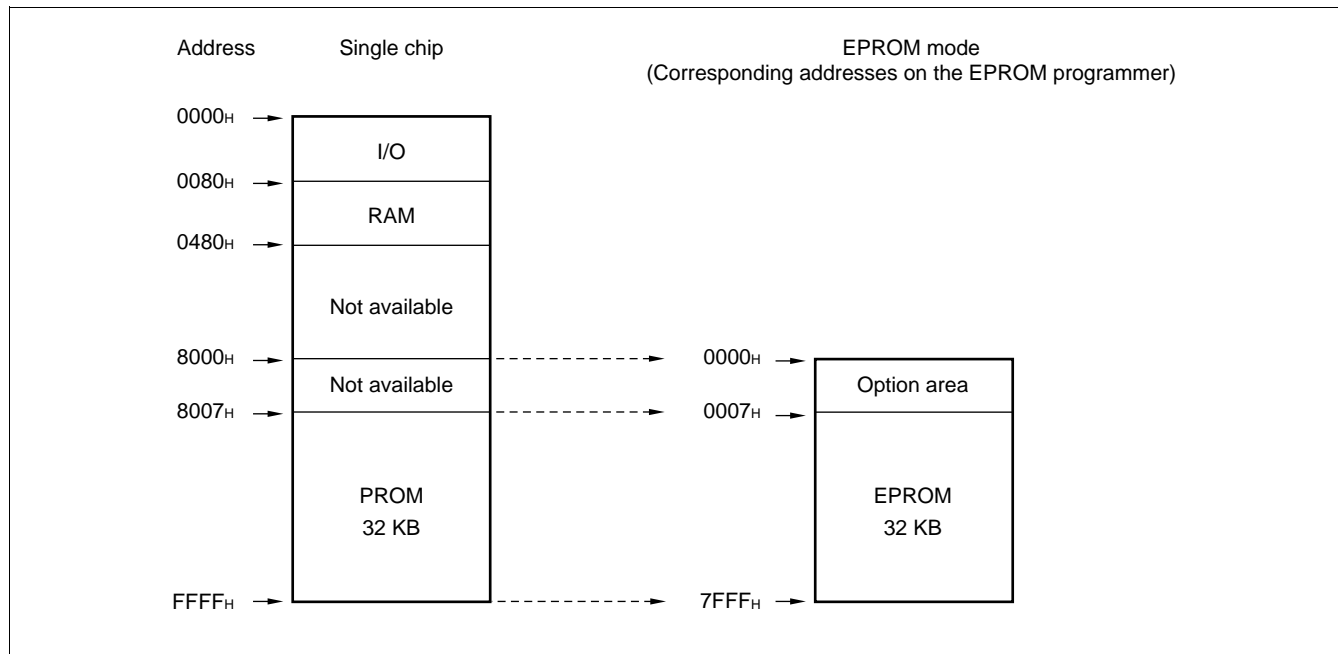
The MB89P147 is an OTPROM version of the MB89140 series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 32-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P147 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 32 Kbytes (8007_H to FFFF_H) the PROM can be programmed as follows:

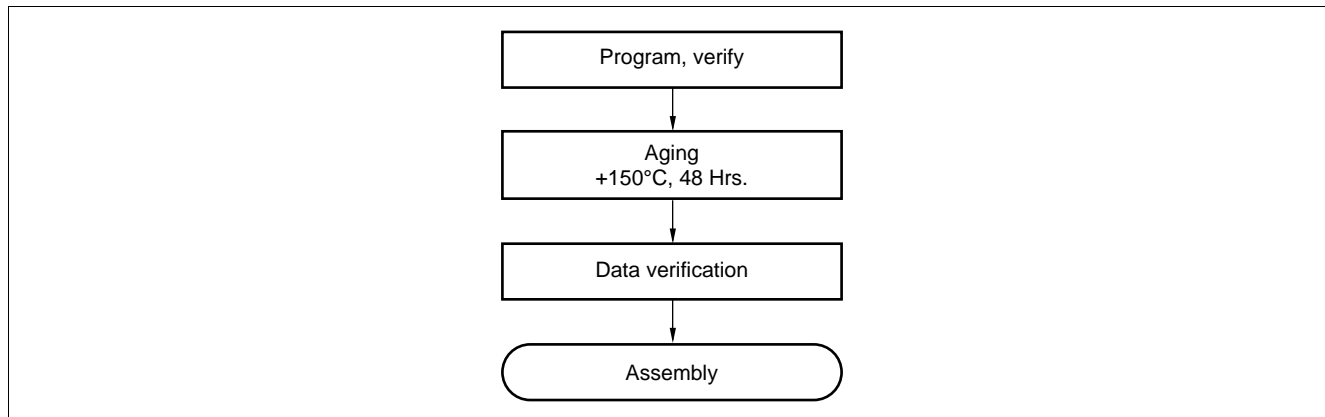
• Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007_H to 7FFF_H (note that addresses 8007_H to FFFF_H while operating as a single chip assign to 0007_H to 7FFF_H in EPROM mode). Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see “5. Setting OTPROM Options.” in section “■ Programming to the EPROM with Piggyback/evaluation Device”)
- (3) Program to 0000_H to 7FFF_H with the EPROM programmer.

MB89140 Series

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
DIP-64P-M01	ROM-64SD-28DP-8L4
FPT-64P-M06	ROM-64QF-28DP-8L4

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV, MBM27C256A-20CZ

2. Programming Socket Adapter

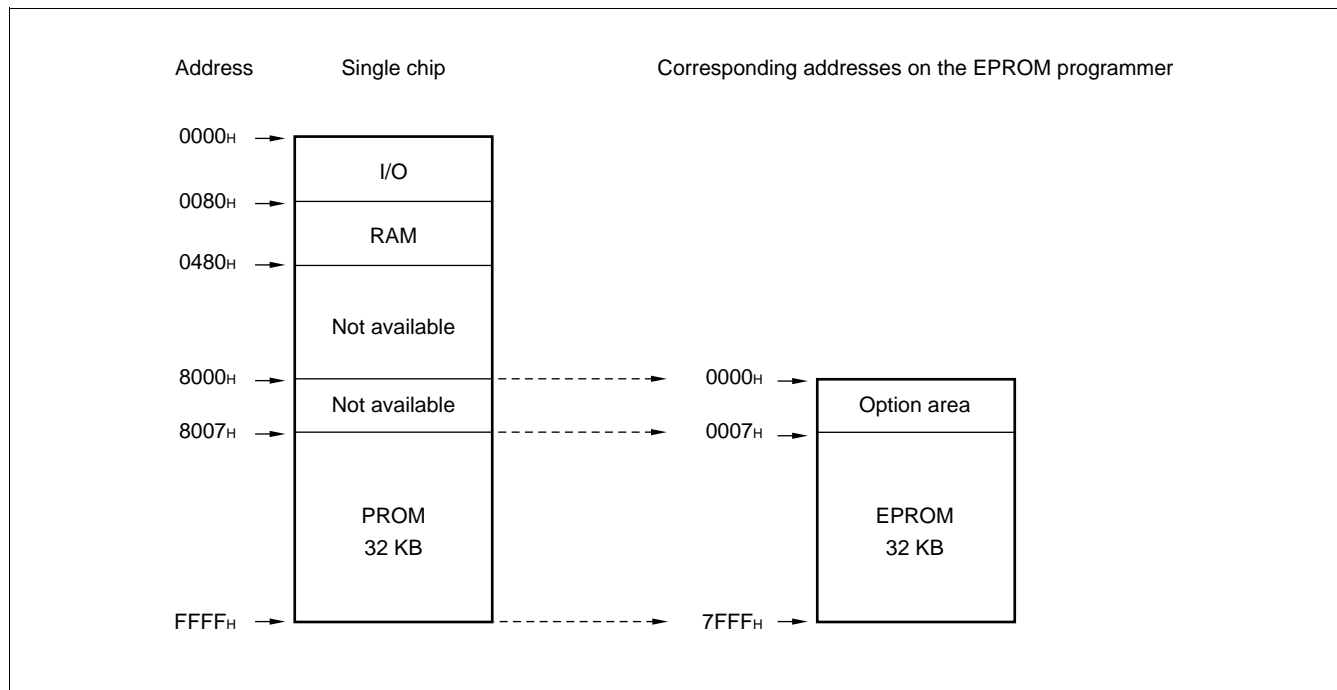
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG
LCC-32 (Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007H to 7FFFH.
- (3) Program to 0000H to 7FFFH with the EPROM programmer.

MB89140 Series

5. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8000 _H (0000 _H)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Single/dual-clock system 1: Dual clock 0: Single clock	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Reserved (Write 1 bit to this bit.)	Reserved (Write 1 bit to this bit.)
8001 _H (0001 _H)	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
8002 _H (0002 _H)	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	Vacancy Readable and writable	Vacancy Readable and writable
8003 _H (0003 _H)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
8004 _H (0004 _H)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
8005 _H (0005 _H)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
8006 _H (0006 _H)	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

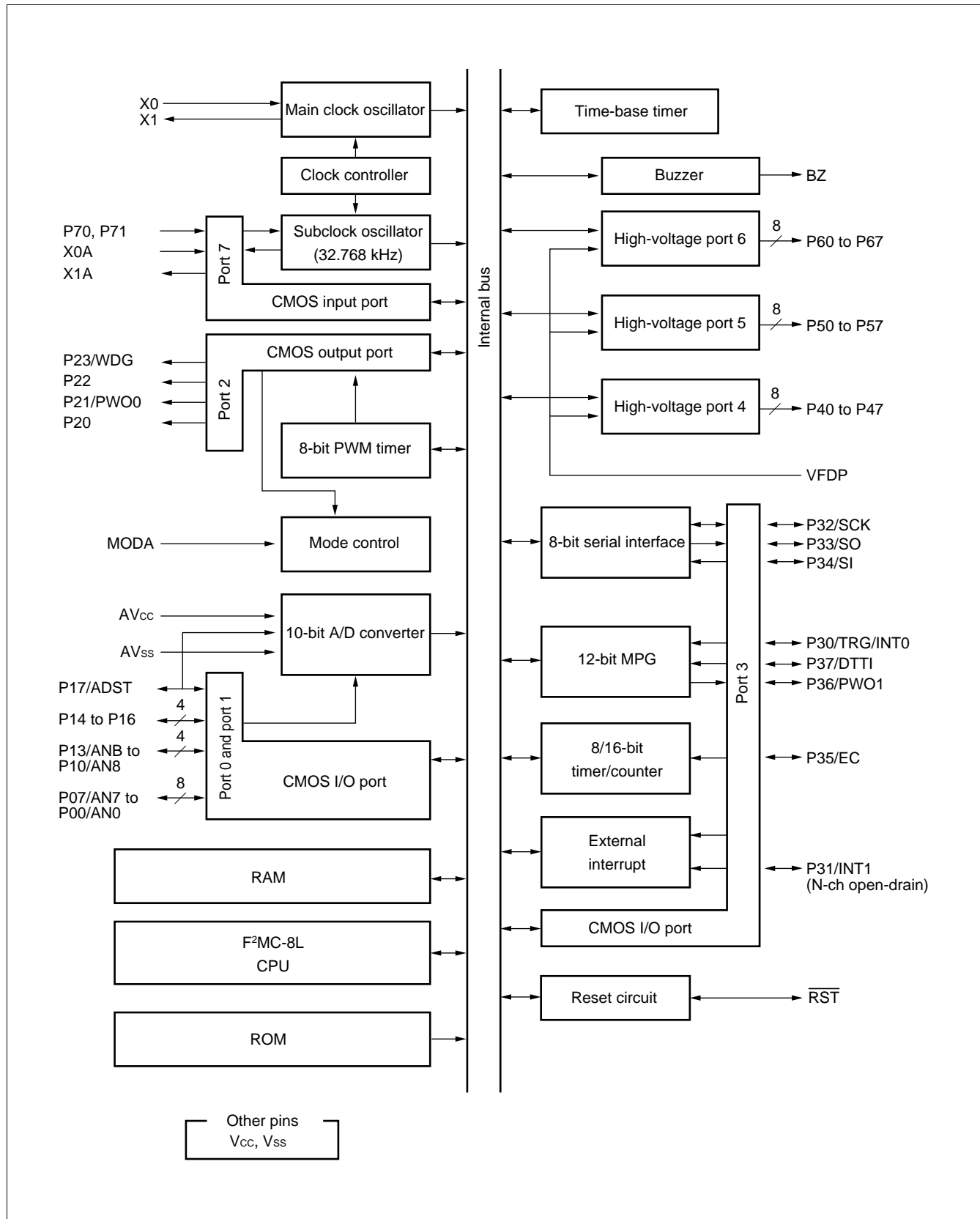
Notes: • Set each bit to 1 to erase.

- Do not write 0 to the vacant bit.

The read value of the vacant bit is 1, unless 0 is written to it.

- The parenthesized addresses are the corresponding addresses on the EPROM programmer.

■ BLOCK DIAGRAM

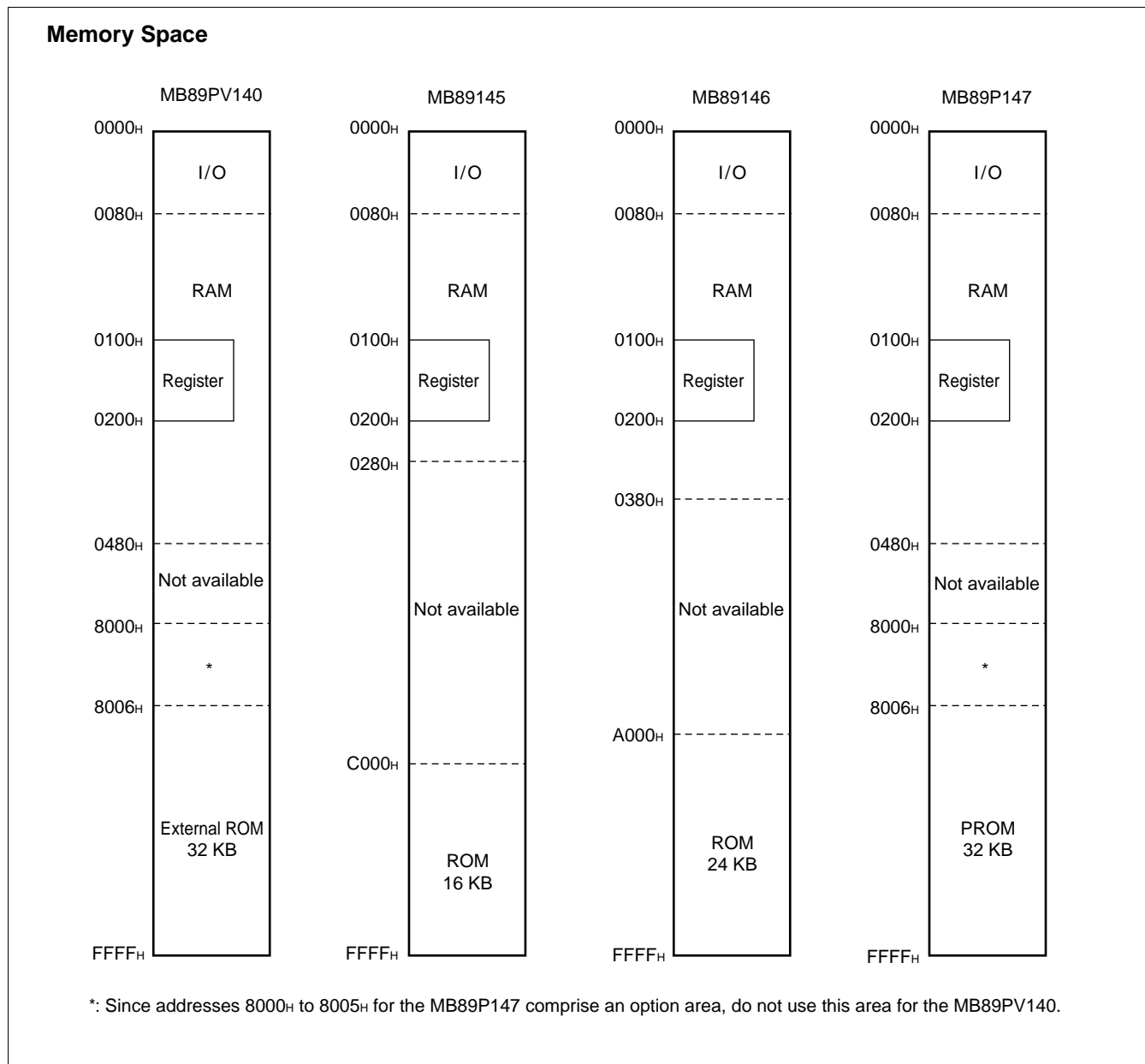


MB89140 Series

■ CPU CORE

1. Memory Space

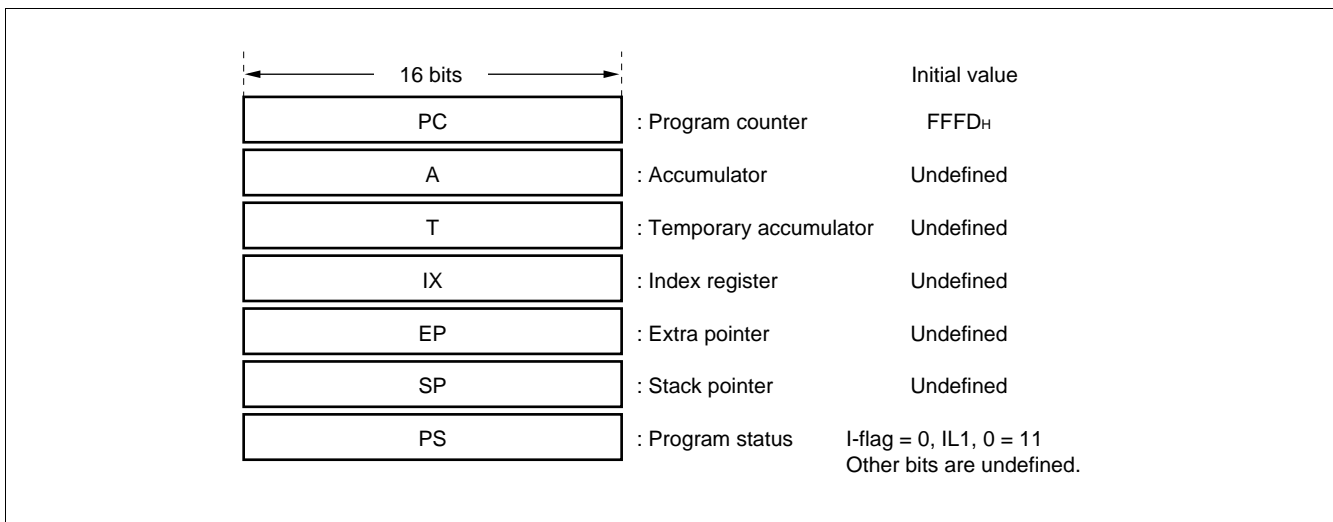
The microcontrollers of the MB89140 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89140 series is structured as illustrated below.



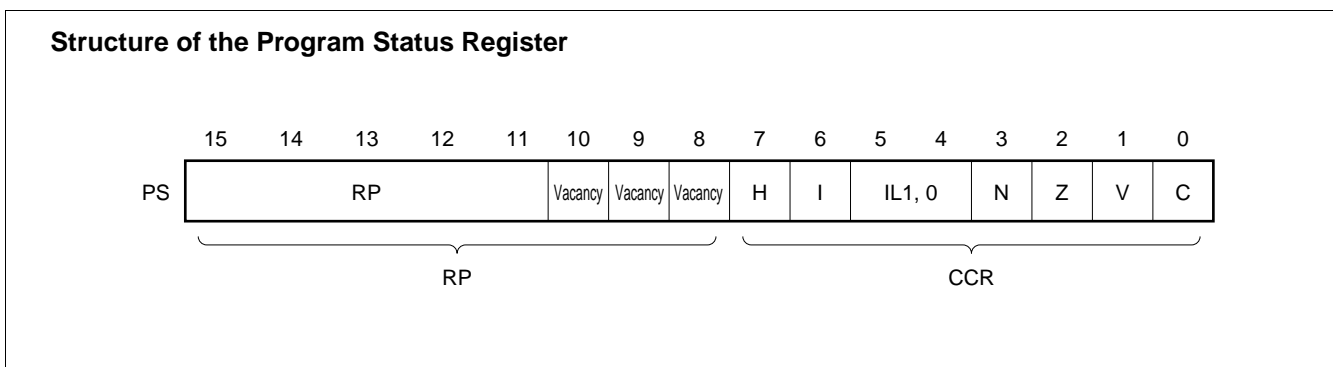
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification
- Extra pointer (EP): A 16-bit pointer for indicating a memory address
- Stack pointer (SP): A 16-bit register for indicating a stack area
- Program status (PS): A 16-bit register for storing a register pointer, a condition code



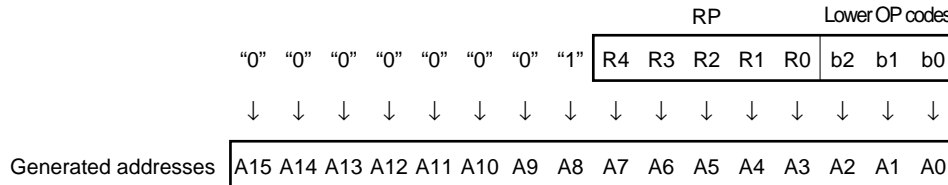
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



MB89140 Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

- H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.
- I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.
- IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	ILO	Interrupt level	High-low
0	0	1	High
0	1		↑
1	0	2	↓
1	1	3	Low = no interrupt

- N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.
- Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.
- V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.
- C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

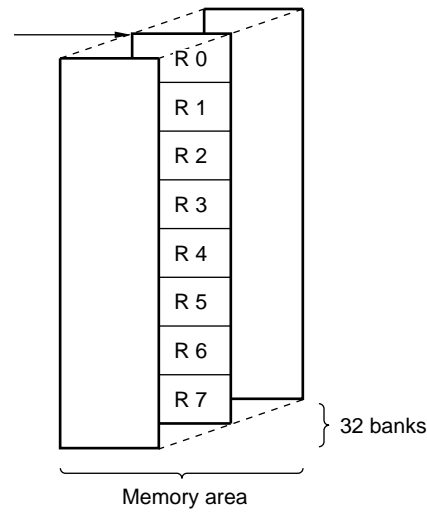
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used in the MB89140 series. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration

This address = $0100\text{H} + 8 \times (\text{RP})$



MB89140 Series

■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	BUZR	Buzzer register
0FH	(R/W)	EIC	External interrupt control register
10H	(R/W)	PDR4	Port 4 data register
11H	(R/W)	PDR5	Port 5 data register
12H	(R/W)	PDR6	Port 6 data register
13H	(R)	PDR7	Port 7 data register
14H			Vacancy
15H			Vacancy
16H	(W)	COMR	8-bit PWM timer compare register
17H	(R/W)	CNTR	8-bit PWM timer control register
18H	(R/W)	T3CR	Timer 3 control register
19H	(R/W)	T2CR	Timer 2 control register
1AH	(R/W)	T3DR	Timer 3 data register
1BH	(R/W)	T2DR	Timer 2 data register
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH	(R/W)	ADC1	A/D converter control register 1
1FH	(R/W)	ADC2	A/D converter control register 2

(Continued)

MB89140 Series

(Continued)

Address	Read/write	Register name	Register description
20 _H	(R/W)	ADDH	A/D converter data register (H)
21 _H	(R/W)	ADDL	A/D converter data register (L)
22 _H	(W)	PCR0	Port input control register 0
23 _H	(W)	PCR1	Port input control register 1
24 _H	(R/W)	MCNT	MPG control register
25 _H	(R/W)	INTSTR	MPG interrupt status register
26 _H	(W)	CMCLBR (H)	MPG compare clear buffer register H
27 _H	(W)	CMCLBR (L)	MPG compare clear buffer register L
28 _H	(W)	OUTCBR (H)	MPG output buffer register H
29 _H	(W)	OUTCBR (L)	MPG output buffer register L
2A _H			Vacancy
2B _H			Vacancy
2C _H			Vacancy
2D _H			Vacancy
2E _H			Vacancy
2F _H			Vacancy
30 _H to 77 _H			Vacancy
78 _H			Vacancy
79 _H			Vacancy
7A _H			Vacancy
7B _H			Vacancy
7C _H	(W)	ILR1	Interrupt level setting register 1
7D _H	(W)	ILR2	Interrupt level setting register 2
7E _H	(W)	ILR3	Interrupt level setting register 3
7F _H			Vacancy

Note: Do not use vacancies.

MB89140 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC}	V _{SS} - 0.3	V _{SS} + 7.0	V	
	AV _{CC}	V _{SS} - 0.3	V _{SS} + 7.0	V	*2
I/O voltage	V _{IO1}	V _{SS} - 0.3	V _{CC} + 0.3	V	Except P31
	V _{IO2}	V _{SS} - 0.3	7	V	P31
"H" level total average output current	ΣI _{OH}	—	-120	mA	Average value (operating current × operating rate)
"H" level maximum output current	I _{OH}	—	-12	mA	P00 to P07, P10 to P17, P20 to P23, P30, P32 to P37
		—	-20	mA	P40 to P47, P50 to P57
		—	-36	mA	P60 to P67, BZ
"H" level average output current	I _{OHAV}	—	-6	mA	P00 to P07, P10 to P17, P20 to P23, P30, P32 to P37 Average value (operating current × operating rate) ^{*1}
		—	-10	mA	P40 to P47, P50 to P57 Average value (operating current × operating rate) ^{*1}
		—	-18	mA	P60 to P67, BZ Average value (operating current × operating rate) ^{*1}
"L" level total average output current	ΣI _{OLAV}	—	150	mA	Average value (operating current × operating rate) ^{*1}
"L" level maximum output current	I _{OL}	—	12	mA	P00 to P07, P10 to P17, P20 to P23, P30 to P37
"L" level average output current	I _{OLAV}	—	6	mA	P00 to P07, P10 to P17, P20 to P23, P30 to P37 Average value (operating current × operating rate) ^{*1}
Power consumption	P _D	—	500	mW	
Operating temperature	T _A	-40	+85	°C	
Storage temperature	T _{stg}	-55	+150	°C	

*1: The total average output current is defined as the average current that flows through all of the relevant pins in a 100 ms period. The output peak current is defined as the peak value of any one of the relevant pins. The average output current is defined as the average current that flows through any one of the relevant pins in a 100 ms period.

*2: Use AV_{CC} and V_{CC} set at the same voltage.

Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

Precautions: Permanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC} AV _{CC}	2.7*	6.0*	V	Normal operation assurance range*
		2.2	6.0	V	In watch mode or subclock operation (Only for the MB89P147, the minimum value is 2.7 V.)
		1.5	6.0	V	Retains the RAM state in stop mode
	VFDP	V _{CC} - 40	V _{CC} + 0.3	V	
Operating temperature	T _A	-40	+85	°C	

* : These values vary with the operating frequency and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

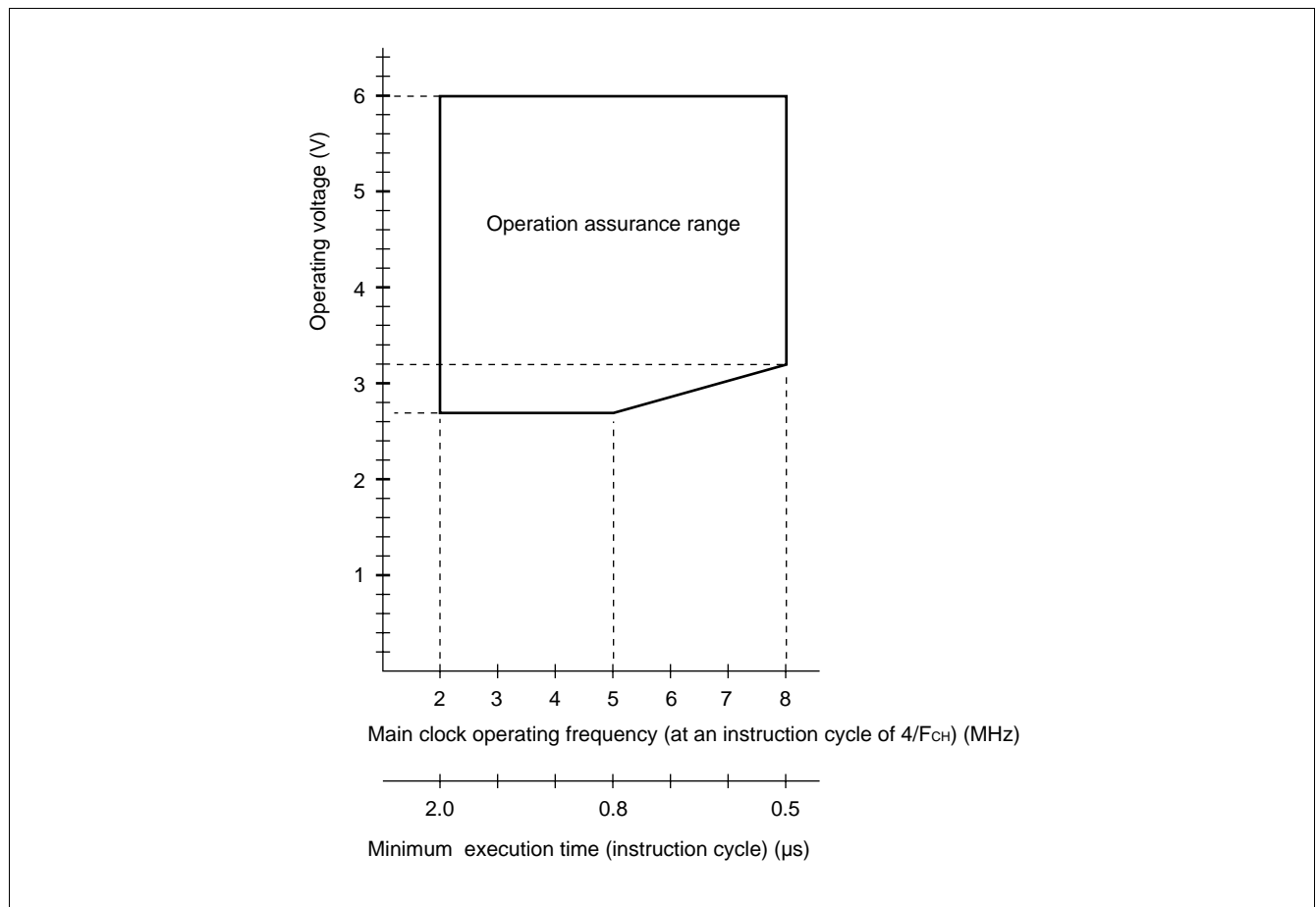


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$. Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

MB89140 Series

3. DC Characteristics

($V_{CC} = V_{CC} = 5.0\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IHS}	P00 to P07, P10 to P17, P30 to P37, P70, P71, X0, X1, \overline{RST} , MODA	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	V_{ILS}	P00 to P07, P10 to P17, P30 to P37, P70, P71, X0, X1, \overline{RST} , MODA	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17, P20 to P23, P30, P32 to P37	$I_{OH} = -2.0\text{ mA}$	2.4	—	—	V	
	V_{OH2}	P40 to P47, P50 to P57	$I_{OH} = -10\text{ mA}$	3.0	—	—	V	
	V_{OH3}	P60 to P67, BZ	$I_{OH} = -18\text{ mA}$	3.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P23, P30, P32 to P37	$I_{OL} = 1.8\text{ mA}$	—	—	0.4	V	
	V_{OL2}	\overline{RST}	$I_{OL} = 4.0\text{ mA}$	—	—	0.6	V	
Input leakage current	I_{LI1}	P00 to P07, P10 to P17, P30 to P37, P70, P71, MODA	$0.45\text{ V} < V_i < V_{CC}$	—	—	± 5	μA	Without pull-up resistor for P14 to P17 and P32 to P37
	I_{LI2}	P14 to P17, P32 to P37	$V_i = 0.0\text{ V}$	-200	-100	-50	μA	With pull-up resistor
Output leakage current	I_{LO1}	P40 to P47, P50 to P57	$V_i = VFDP = V_{CC} - 40\text{ V}$	—	—	-10	μA	
	I_{LO2}	P60 to P67, BZ	$V_i = VFDP = V_{CC} - 40\text{ V}$	—	—	-20	μA	
Pull-up resistance	R_{PULU}	\overline{RST} P14 to P17, P32 to P37	$V_i = 0.0\text{ V}$	25	50	100	k Ω	With pull-up resistor
Pull-down resistance	R_{PULD}	P40 to P47, P50 to P57, P60 to P67	$V_{OH} = 5.0\text{ V}$	50	100	150	k Ω	With pull-down resistor optional

(Continued)

MB89140 Series

(Continued)

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks	
				Min.	Typ.	Max.			
Power supply current*1	I _{CC1}	V _{CC}	F _{CH} = 8 MHz V _{CC} = 5.0 V t _{inst} *2 = 0.5 μs Output open	—	9	15	mA		
	I _{CC2}		F _{CH} = 8 MHz V _{CC} = 3.2 V t _{inst} *2 = 8.0 μs Output open	—	1.5	2	mA		
			—	2.5	5.0	mA	MB89P147		
	I _{CCS1}		Sleep mode	F _{CH} = 8 MHz V _{CC} = 5.0 V t _{inst} *2 = 0.5 μs	—	3	7	mA	
				F _{CH} = 8 MHz V _{CC} = 3.2 V t _{inst} *2 = 8.0 μs	—	1	1.5	mA	
	I _{CCS2}		Subclock mode	F _{CL} = 32.768 kHz V _{CC} = 3.0 V	—	50	150	μA	
					—	1	3	mA	MB89P147
	I _{CCCL}		Subclock sleep mode	F _{CL} = 32.768 kHz V _{CC} = 3.0 V	—	25	50	μA	
	I _{CCCT}		Watch mode	F _{CL} = 32.768 kHz V _{CC} = 3.0 V	—	3	15	μA	
	I _{CCCH}		Stop mode	T _A = +25°C	—	—	10	μA	
I _A	I _{AH}	AV _{CC}	F _{CH} = 8 MHz, when A/D conversion is activated	—	1.5	4	mA		
			T _A = +25°C, when A/D conversion is stopped	—	1	5	μA		
Input capacitance	C _{IN}	Other than AV _{CC} , AV _{SS} , V _{CC} , and V _{SS}	f = 1 MHz	—	10	—	pF		

*1: The power supply current is measured at the external clock.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

Note: F_{CH} indicates the main clock oscillation frequency. When F_{CH} = 8 MHz, the 4/F_{CH} execution time is 0.5 μs, and the 64/F_{CH} execution time is 8 μs.

MB89140 Series

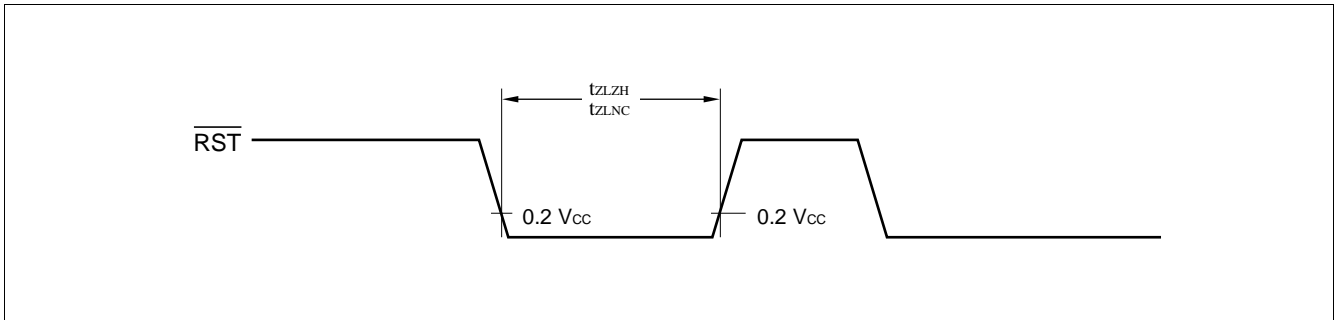
4. AC Characteristics

(1) Reset Timing

($A_{V_{CC}} = V_{CC} = 5.0\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
$\overline{\text{RST}}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}	—	—	ns	
$\overline{\text{RST}}$ noise limit width	t_{ZLNC}		30	50	80	ns	

Note: t_{XCYL} is the oscillation cycle ($1/F_{\text{CH}}$) to input to the X0 pin.



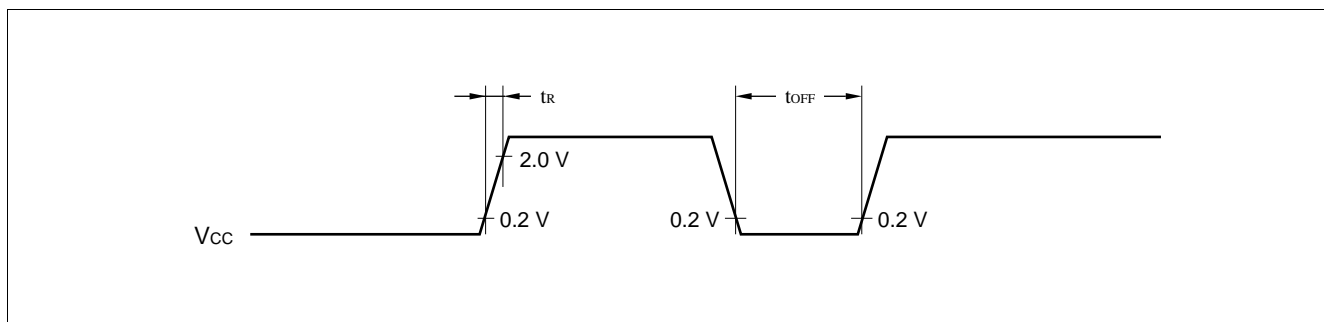
(2) Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_{R}	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

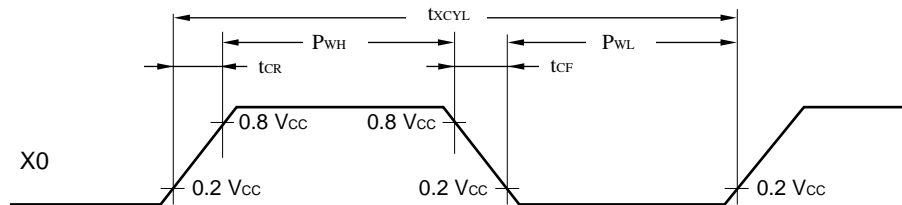


(3) Clock Timing

($V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

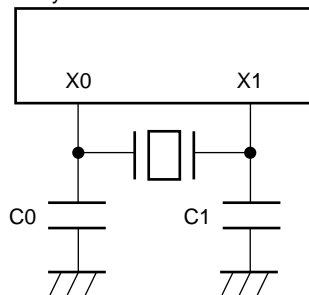
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	2	—	8	MHz	
	F_{CL}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{XCYL}	X0, X1	—	125	—	500	ns	
	t_{LXCYL}	X0A, X1A		—	30.5	—	μs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	30	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A		—	15.2	—	μs	
Input clock rising/falling time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	External clock	

X0 and X1 Timing and Conditions

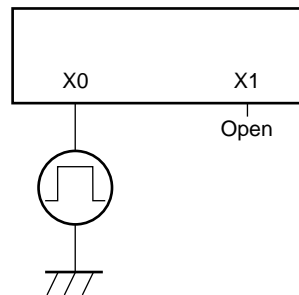


Main Clock Conditions

When a crystal or ceramic resonator is used

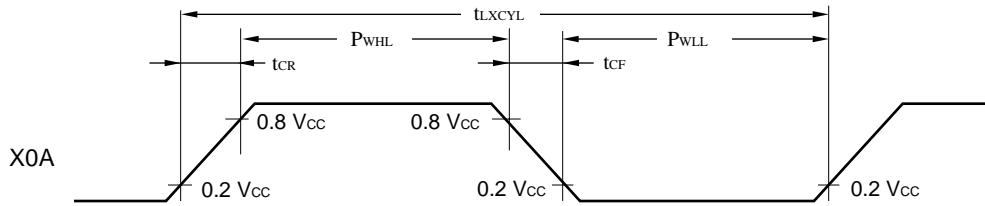


When an external clock is used



MB89140 Series

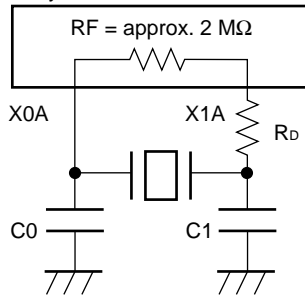
X0A and X1A Timing and Conditions



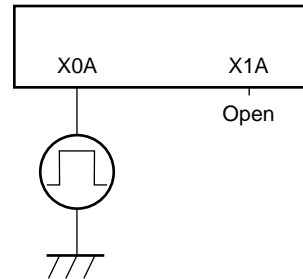
Subclock Conditions

MB89PV140

When a crystal or ceramic resonator is used

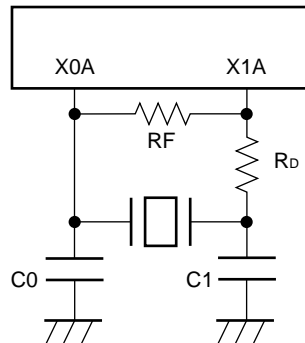


When an external clock is used

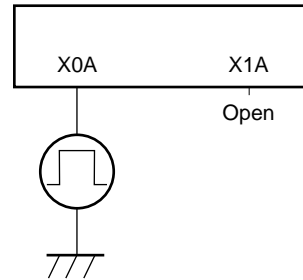


Mask ROM products and MB89P147

When a crystal or ceramic resonator is used



When an external clock is used



Note: The subclock oscillator feedback resistor is connected externally in dual-clock mask ROM products and in the MB89P147. (The subclock oscillator feedback resistor is connected internally in the MB89PV140-102.)

(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	μs	$(4/F_{CH}) t_{inst} = 0.5 \mu s$ when operating at $F_{CH} = 8 \text{ MHz}$
		$2/F_{CL}$	μs	$t_{inst} = 61.036 \mu s$ when operating at $F_{CL} = 32.768 \text{ kHz}$

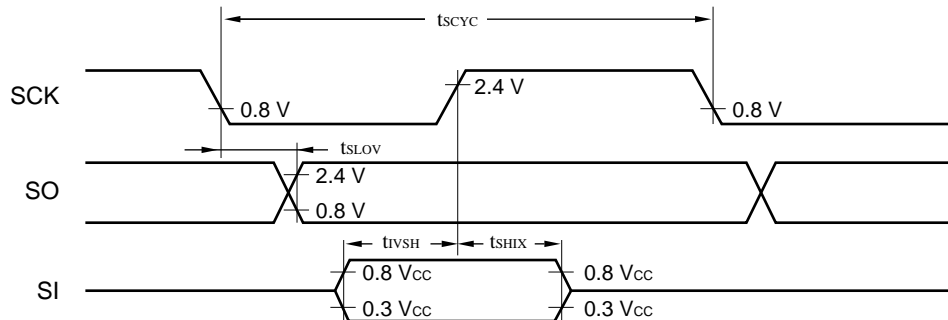
(5) Serial I/O Timing

($AV_{CC} = V_{CC} = 5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

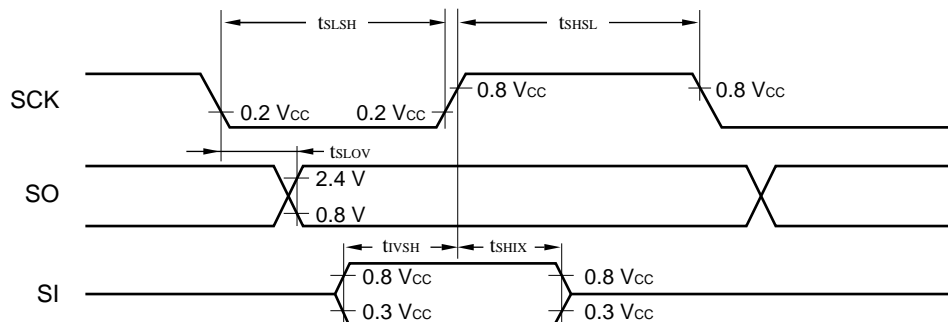
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	$2 t_{inst}^*$	—	μs	
SCK $\downarrow \rightarrow$ SO time	t_{SLOV}	SCK, SO		-200	200	ns	
Valid SI \rightarrow SCK \uparrow	t_{VSH}	SI, SCK		$1/2 t_{inst}^*$	—	μs	
SCK $\uparrow \rightarrow$ valid SI hold time	t_{SHIX}	SCK, SI		$1/2 t_{inst}^*$	—	μs	
Serial clock "H" pulse width	t_{SHSL}	SCK	External shift clock mode	$1 t_{inst}^*$	—	μs	
Serial clock "L" pulse width	t_{SLSH}	SCK		$1 t_{inst}^*$	—	μs	
SCK $\downarrow \rightarrow$ SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI \rightarrow SCK \uparrow	t_{VSH}	SI, SCK		$1/2 t_{inst}^*$	—	μs	
SCK $\uparrow \rightarrow$ valid SI hold time	t_{SHIX}	SCK, SI	$1/2 t_{inst}^*$	—	μs		

* : For information on t_{inst} , see "(4) Instruction Cycle."

Internal Shift Clock Mode



External Shift Clock Mode



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(6) Peripheral Input Timing

($AV_{CC} = V_{CC} = 5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

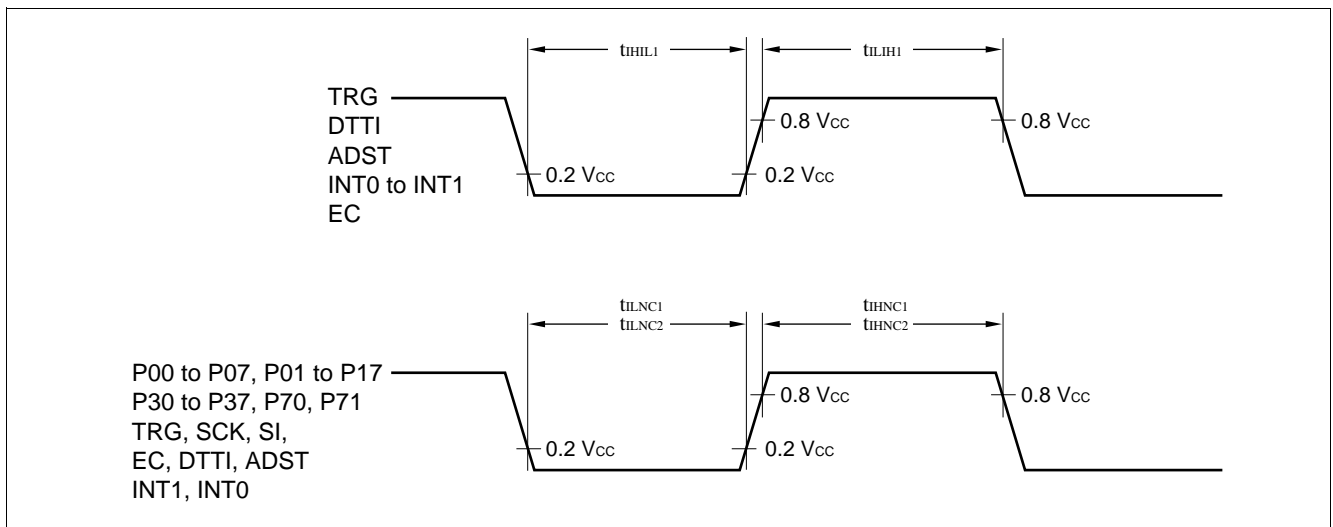
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input "H" pulse width 1	t_{LIH1}	TRG, DTTI ADST, EC INT0 to INT1	—	$2 t_{inst}^*$	—	μs	
Peripheral input "L" pulse width 1	t_{LIL1}	TRG, DTTI ADST, EC INT0 to INT1	—	$2 t_{inst}^*$	—	μs	

* : For information on t_{inst} , see "(4) Instruction Cycle."

(7) Peripheral Input Noise Limit Width

($AV_{CC} = V_{CC} = 5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40^\circ C$ to $+85^\circ C$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input "H" level noise limit width 1	t_{IHNC1}	All inputs except INT1 and INT0	7	15	30	ns	MB89P147/PV140
			15	30	60	ns	Except MB89P147/PV140
Peripheral input "L" level noise limit width 1	t_{ILNC1}	All inputs except INT1 and INT0	7	15	30	ns	MB89P147/PV140
			15	30	60	ns	Except MB89P147/PV140
Interrupt "H" level noise limit width 2	t_{IHNC2}	INT1, INT0	30	50	100	ns	MB89P147/PV140
			50	100	250	ns	Except MB89P147/PV140
Interrupt "L" level noise limit width 2	t_{ILNC2}	INT1, INT0	30	50	100	ns	MB89P147/PV140
			50	100	250	ns	Except MB89P147/PV140



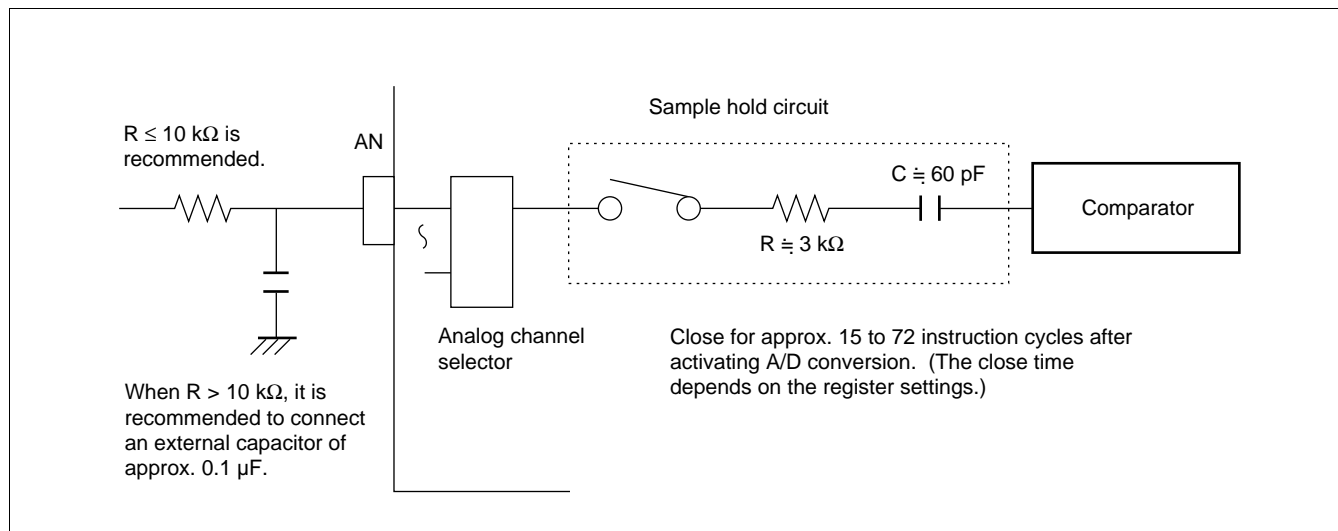
5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $F_{CH} = 8\text{ MHz}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	10	bit	
Total error				—	—	± 3.0	LSB	
Linearity error				—	—	± 2.0	LSB	
Differential linearity error				—	—	± 1.5	LSB	
Zero transition voltage	V_{OT}	AN0 to ANB	—	$AV_{SS} - 1.5\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 2.5\text{ LSB}$	mV	
Full-scale transition voltage	V_{FST}	AN0 to ANB	—	$AV_{CC} - 3.5\text{ LSB}$	$AV_{CC} - 1.5\text{ LSB}$	$AV_{CC} + 0.5\text{ LSB}$	mV	
Interchannel disparity	—	—	—	—	—	4	LSB	
A/D mode conversion time			At 8-MHz oscillation	33	—	—	t_{inst}^*	
Analog port input current	I_{AIN}	AN0 to ANB	$AV_{CC} = V_{CC} = 5.0\text{ V}$	—	—	10	μA	
Analog input voltage	—	AN0 to ANB	—	0.0	—	AV_{CC}	V	

* : For information on t_{inst} , see “(4) Instruction Cycle” in “4. AC Characteristics.”

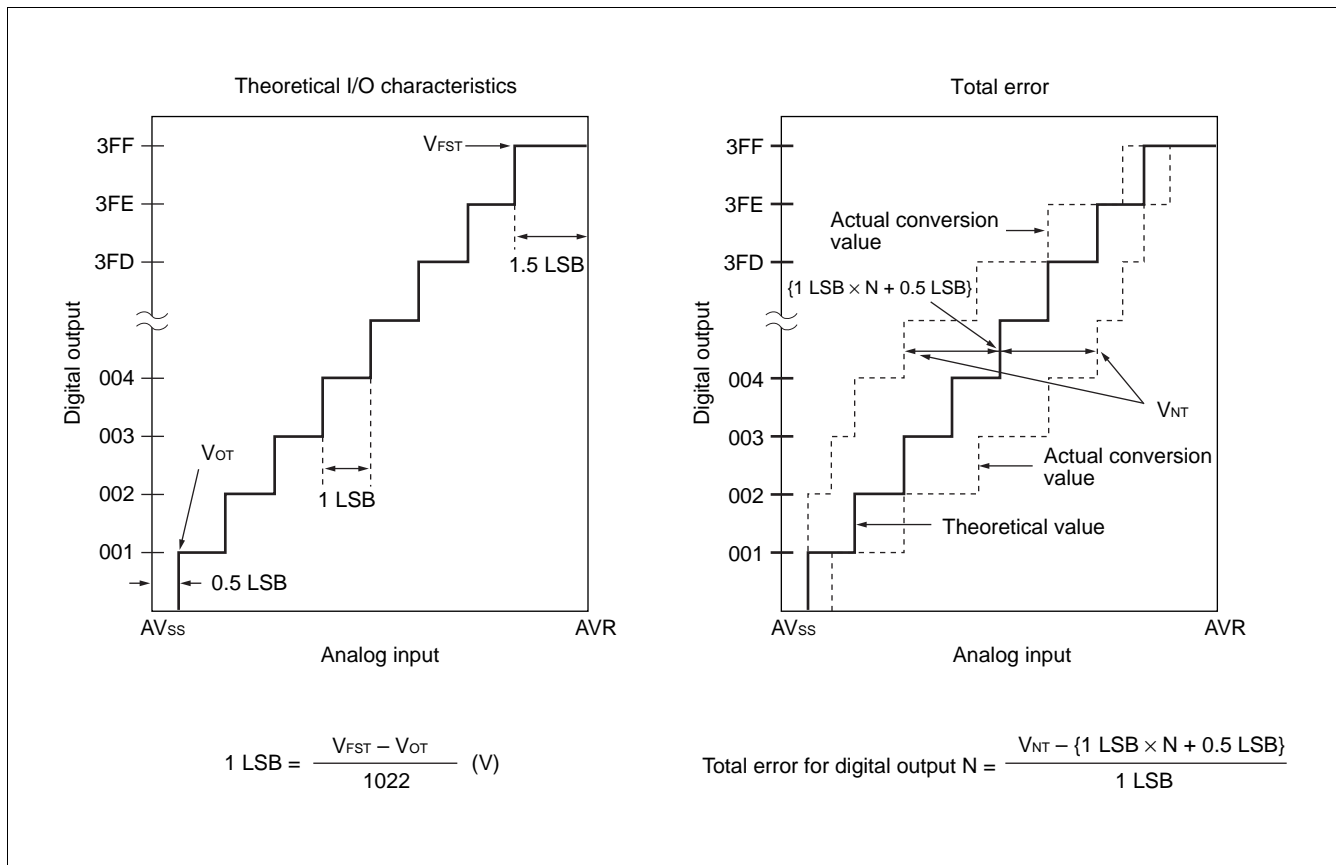
- Notes:
- The smaller AV_{CC} , the greater the error would become relatively.
 - The output impedance of the external circuit connected to an analog input block should be no more than several $k\Omega$. If the output impedance is too high, the analog voltage sampling time might be insufficient.



MB89140 Series

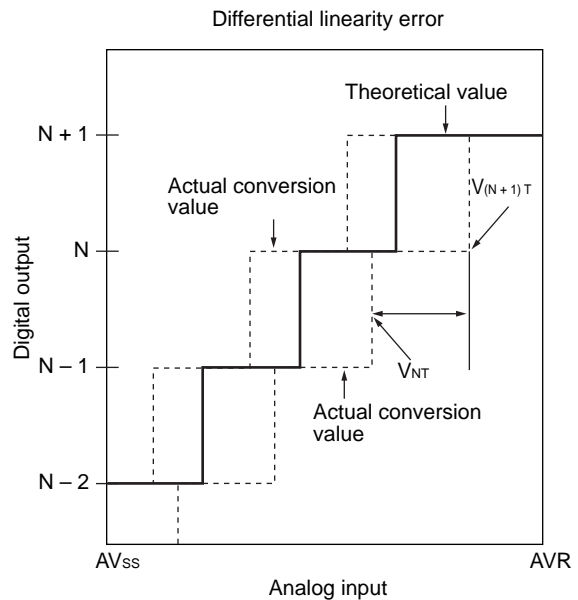
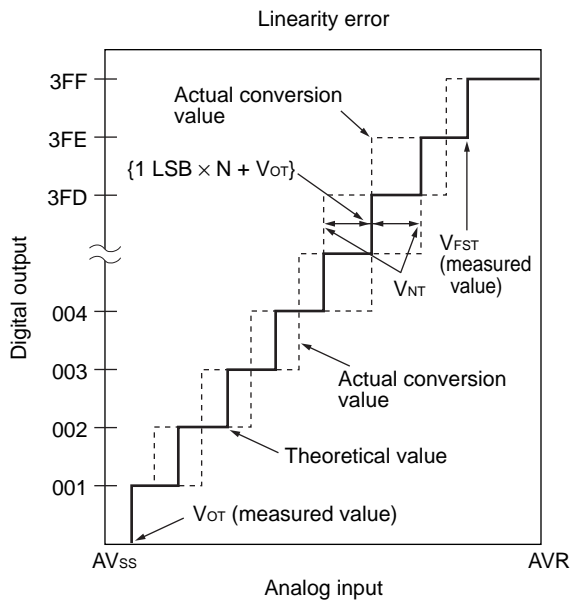
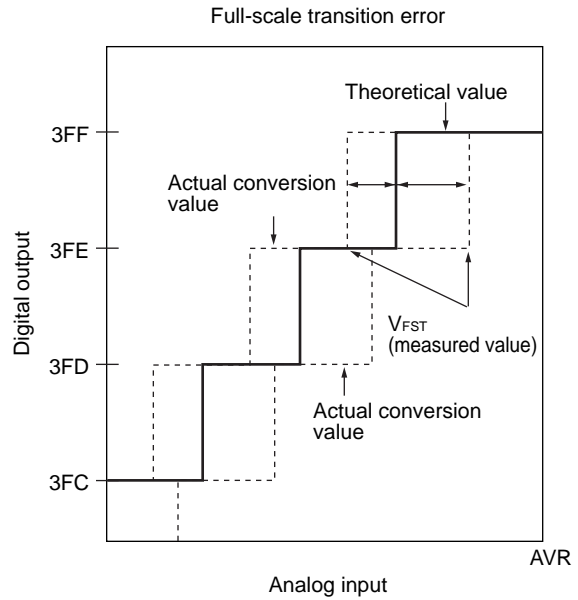
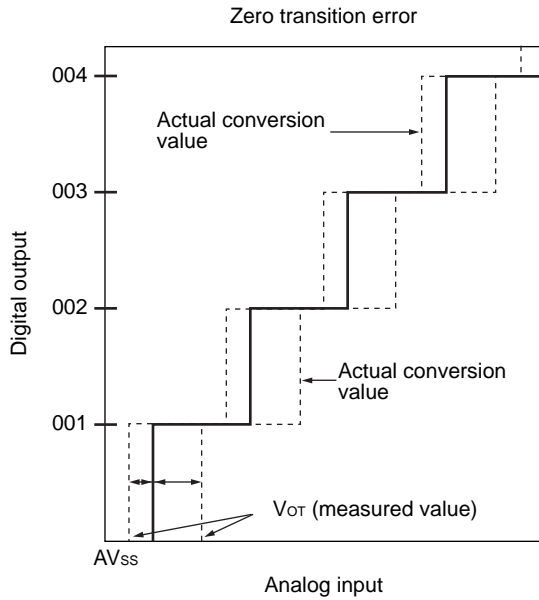
(1) A/D Glossary

- Resolution
Analog changes that are identifiable with the A/D converter
- Linearity error
The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
The difference between theoretical and actual values
This error is caused by the zero transition error, full-scale transition error, linearity error, quantization error and noise.



(Continued)

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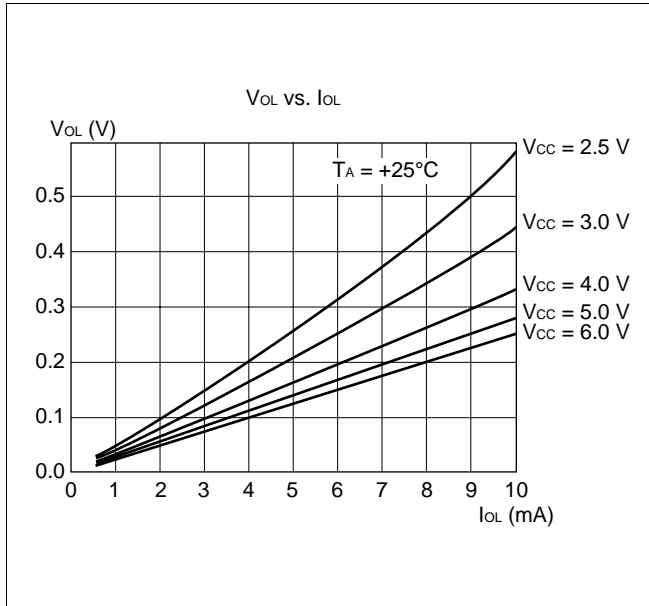
$$\text{Linearity error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linearity error for digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

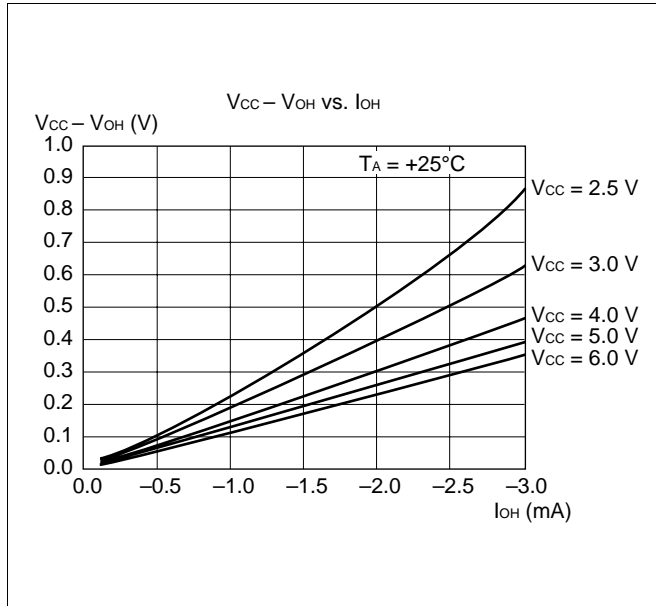
MB89140 Series

EXAMPLE CHARACTERISTICS

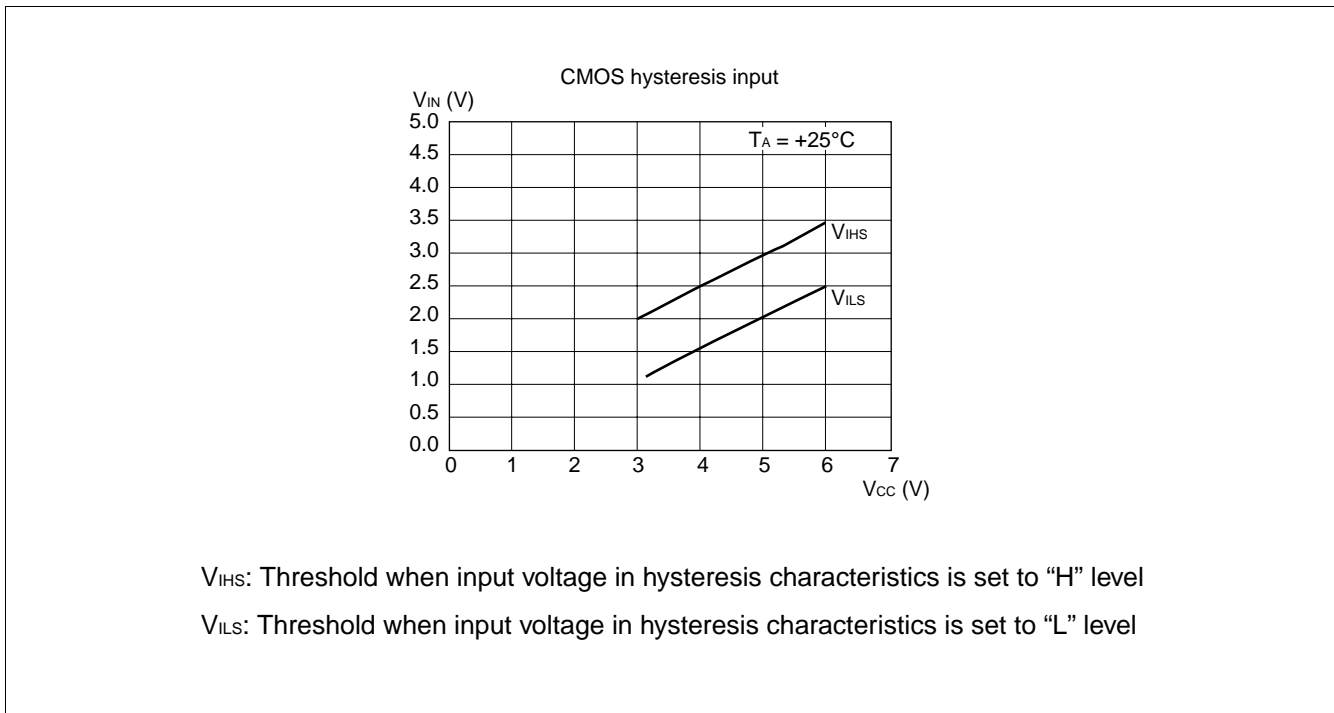
(1) "L" Level Output Voltage



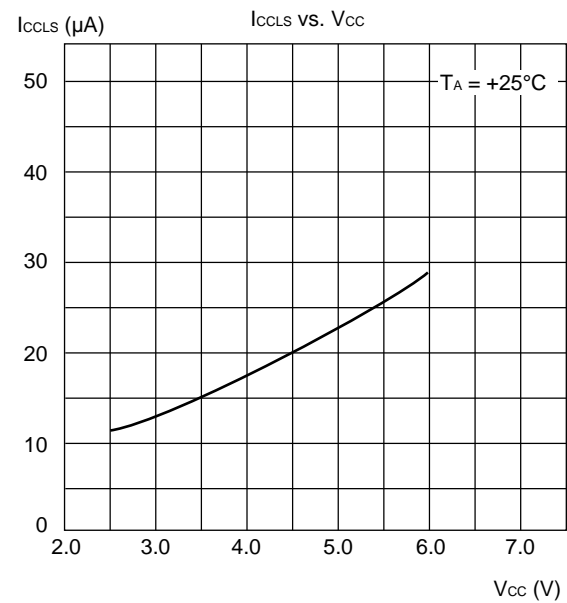
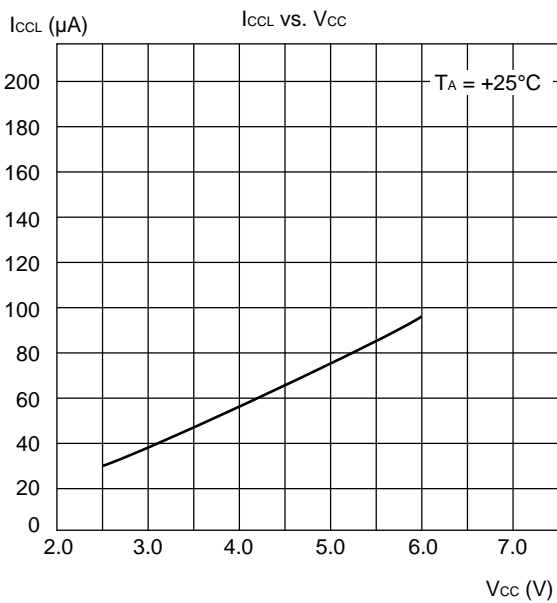
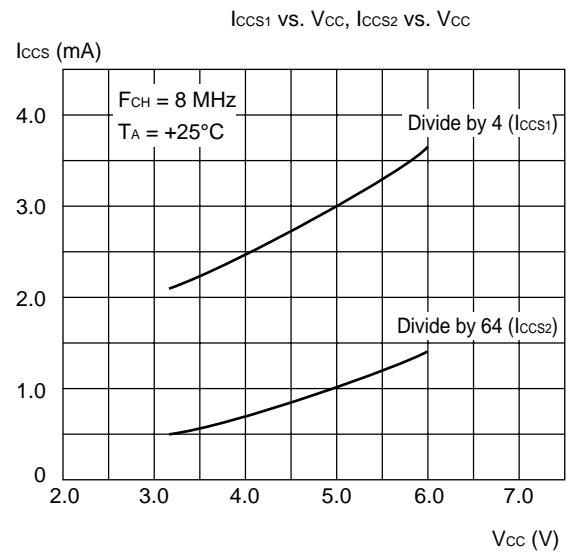
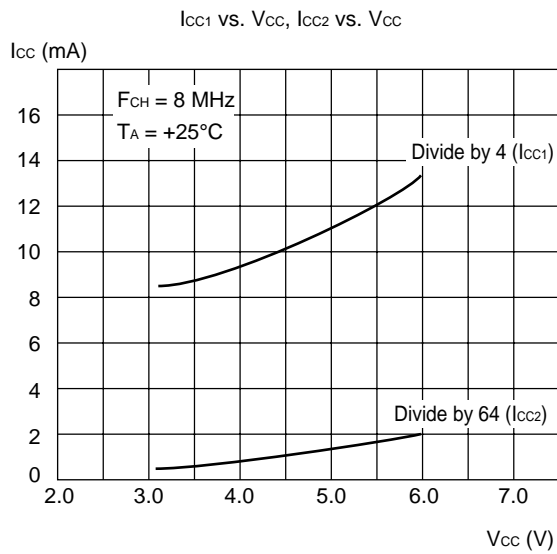
(2) "H" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



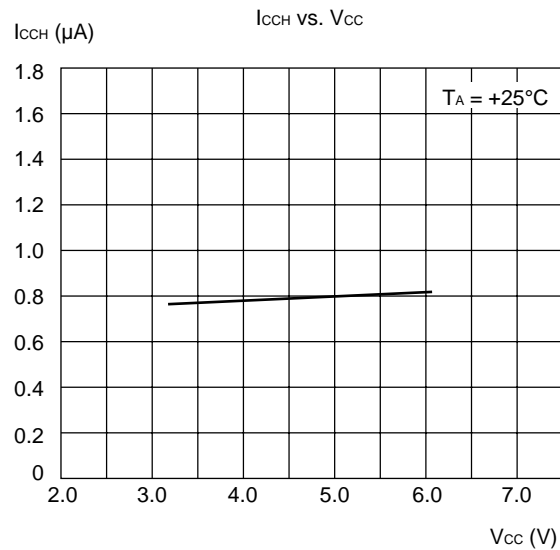
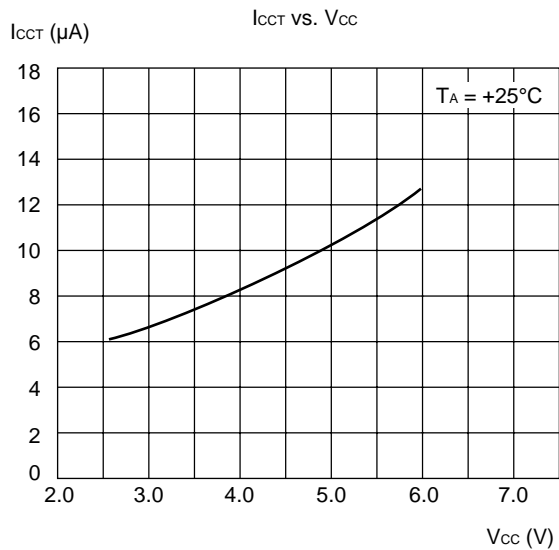
(4) Power Supply Current (External Clock)



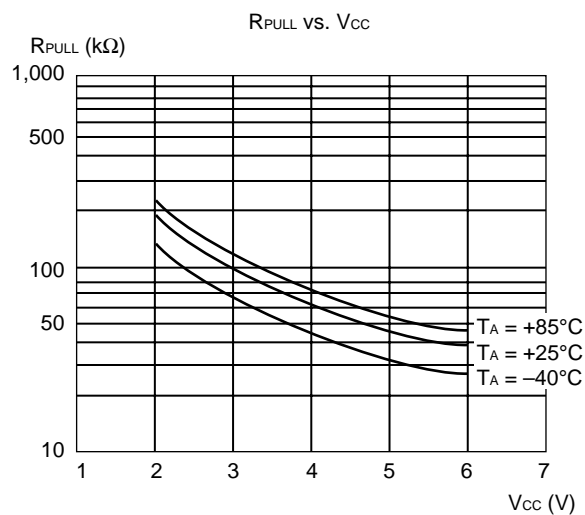
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MB89140 Series

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(5) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “–” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
MOV dir,A	3	2	(dir) ← (A)	-	-	-	----	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	-	-	-	----	46
MOV ext,A	4	3	(ext) ← (A)	-	-	-	----	61
MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	----	47
MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	----	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	-	-	++--	04
MOV A,dir	3	2	(A) ← (dir)	AL	-	-	++--	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	-	-	++--	06
MOV A,ext	4	3	(A) ← (ext)	AL	-	-	++--	60
MOV A,@A	3	1	(A) ← ((A))	AL	-	-	++--	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	++--	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	++--	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	-	-	-	----	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	-	-	-	----	86
MOV @EP,#d8	4	2	((EP)) ← d8	-	-	-	----	87
MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	----	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	-	-	-	----	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	-	-	-	----	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	-	-	-	----	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	-	-	-	----	D7
MOVW EP,A	2	1	(EP) ← (A)	-	-	-	----	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	++--	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	++--	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	++--	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	++--	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A) + 1)	AL	AH	dH	++--	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	++--	C7
MOVW A,EP	2	1	(A) ← (EP)	-	-	dH	----	F3
MOVW EP,#d16	3	3	(EP) ← d16	-	-	-	----	E7
MOVW IX,A	2	1	(IX) ← (A)	-	-	-	----	E2
MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	----	F2
MOVW SP,A	2	1	(SP) ← (A)	-	-	-	----	E1
MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	----	F1
MOV @A,T	3	1	((A)) ← (T)	-	-	-	----	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	-	-	-	----	83
MOVW IX,#d16	3	3	(IX) ← d16	-	-	-	----	E6
MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	----	70
MOVW PS,A	2	1	(PS) ← (A)	-	-	-	++++	71
MOVW SP,#d16	3	3	(SP) ← d16	-	-	-	----	E5
SWAP	2	1	(AH) ↔ (AL)	-	-	AL	----	10
SETB dir: b	4	2	(dir): b ← 1	-	-	-	----	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	-	-	-	----	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	-	-	----	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	----	43
XCHW A,EP	3	1	(A) ↔ (EP)	-	-	dH	----	F7
XCHW A,IX	3	1	(A) ↔ (IX)	-	-	dH	----	F6
XCHW A,SP	3	1	(A) ↔ (SP)	-	-	dH	----	F5
MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	----	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.

- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

MB89140 Series

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
ADDC A,Ri	3	1	$(A) \leftarrow (A) + (Ri) + C$	-	-	-	++++	28 to 2F
ADDC A,#d8	2	2	$(A) \leftarrow (A) + d8 + C$	-	-	-	++++	24
ADDC A,dir	3	2	$(A) \leftarrow (A) + (dir) + C$	-	-	-	++++	25
ADDC A,@IX +off	4	2	$(A) \leftarrow (A) + ((IX) + off) + C$	-	-	-	++++	26
ADDC A,@EP	3	1	$(A) \leftarrow (A) + ((EP)) + C$	-	-	-	++++	27
ADDCW A	3	1	$(A) \leftarrow (A) + (T) + C$	-	-	dH	++++	23
ADDC A	2	1	$(AL) \leftarrow (AL) + (TL) + C$	-	-	-	++++	22
SUBC A,Ri	3	1	$(A) \leftarrow (A) - (Ri) - C$	-	-	-	++++	38 to 3F
SUBC A,#d8	2	2	$(A) \leftarrow (A) - d8 - C$	-	-	-	++++	34
SUBC A,dir	3	2	$(A) \leftarrow (A) - (dir) - C$	-	-	-	++++	35
SUBC A,@IX +off	4	2	$(A) \leftarrow (A) - ((IX) + off) - C$	-	-	-	++++	36
SUBC A,@EP	3	1	$(A) \leftarrow (A) - ((EP)) - C$	-	-	-	++++	37
SUBCW A	3	1	$(A) \leftarrow (T) - (A) - C$	-	-	dH	++++	33
SUBC A	2	1	$(AL) \leftarrow (TL) - (AL) - C$	-	-	-	++++	32
INC Ri	4	1	$(Ri) \leftarrow (Ri) + 1$	-	-	-	+++-	C8 to CF
INCW EP	3	1	$(EP) \leftarrow (EP) + 1$	-	-	-	----	C3
INCW IX	3	1	$(IX) \leftarrow (IX) + 1$	-	-	-	----	C2
INCW A	3	1	$(A) \leftarrow (A) + 1$	-	-	dH	++--	C0
DEC Ri	4	1	$(Ri) \leftarrow (Ri) - 1$	-	-	-	+++-	D8 to DF
DECW EP	3	1	$(EP) \leftarrow (EP) - 1$	-	-	-	----	D3
DECW IX	3	1	$(IX) \leftarrow (IX) - 1$	-	-	-	----	D2
DECW A	3	1	$(A) \leftarrow (A) - 1$	-	-	dH	++--	D0
MULU A	19	1	$(A) \leftarrow (AL) \times (TL)$	-	-	dH	----	01
DIVU A	21	1	$(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$	dL	00	00	----	11
ANDW A	3	1	$(A) \leftarrow (A) \wedge (T)$	-	-	dH	++R-	63
ORW A	3	1	$(A) \leftarrow (A) \vee (T)$	-	-	dH	++R-	73
XORW A	3	1	$(A) \leftarrow (A) \nabla (T)$	-	-	dH	++R-	53
CMP A	2	1	$(TL) - (AL)$	-	-	-	++++	12
CMPW A	3	1	$(T) - (A)$	-	-	-	++++	13
RORC A	2	1	$\rightarrow C \rightarrow A \leftarrow$	-	-	-	++-+	03
ROLC A	2	1	$\leftarrow C \leftarrow A \leftarrow$	-	-	-	++-+	02
CMP A,#d8	2	2	$(A) - d8$	-	-	-	++++	14
CMP A,dir	3	2	$(A) - (dir)$	-	-	-	++++	15
CMP A,@EP	3	1	$(A) - ((EP))$	-	-	-	++++	17
CMP A,@IX +off	4	2	$(A) - ((IX) + off)$	-	-	-	++++	16
CMP A,Ri	3	1	$(A) - (Ri)$	-	-	-	++++	18 to 1F
DAA	2	1	Decimal adjust for addition	-	-	-	++++	84
DAS	2	1	Decimal adjust for subtraction	-	-	-	++++	94
XOR A	2	1	$(A) \leftarrow (AL) \nabla (TL)$	-	-	-	++R-	52
XOR A,#d8	2	2	$(A) \leftarrow (AL) \nabla d8$	-	-	-	++R-	54
XOR A,dir	3	2	$(A) \leftarrow (AL) \nabla (dir)$	-	-	-	++R-	55
XOR A,@EP	3	1	$(A) \leftarrow (AL) \nabla ((EP))$	-	-	-	++R-	57
XOR A,@IX +off	4	2	$(A) \leftarrow (AL) \nabla ((IX) + off)$	-	-	-	++R-	56
XOR A,Ri	3	1	$(A) \leftarrow (AL) \nabla (Ri)$	-	-	-	++R-	58 to 5F
AND A	2	1	$(A) \leftarrow (AL) \wedge (TL)$	-	-	-	++R-	62
AND A,#d8	2	2	$(A) \leftarrow (AL) \wedge d8$	-	-	-	++R-	64
AND A,dir	3	2	$(A) \leftarrow (AL) \wedge (dir)$	-	-	-	++R-	65

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
AND A,@EP	3	1	$(A) \leftarrow (AL) \wedge ((EP))$	-	-	-	++R-	67
AND A,@IX +off	4	2	$(A) \leftarrow (AL) \wedge ((IX) +off)$	-	-	-	++R-	66
AND A,Ri	3	1	$(A) \leftarrow (AL) \wedge (Ri)$	-	-	-	++R-	68 to 6F
OR A	2	1	$(A) \leftarrow (AL) \vee (TL)$	-	-	-	++R-	72
OR A,#d8	2	2	$(A) \leftarrow (AL) \vee d8$	-	-	-	++R-	74
OR A,dir	3	2	$(A) \leftarrow (AL) \vee (dir)$	-	-	-	++R-	75
OR A,@EP	3	1	$(A) \leftarrow (AL) \vee ((EP))$	-	-	-	++R-	77
OR A,@IX +off	4	2	$(A) \leftarrow (AL) \vee ((IX) +off)$	-	-	-	++R-	76
OR A,Ri	3	1	$(A) \leftarrow (AL) \vee (Ri)$	-	-	-	++R-	78 to 7F
CMP dir,#d8	5	3	$(dir) - d8$	-	-	-	++++	95
CMP @EP,#d8	4	2	$((EP)) - d8$	-	-	-	++++	97
CMP @IX +off,#d8	5	3	$((IX) +off) - d8$	-	-	-	++++	96
CMP Ri,#d8	4	2	$(Ri) - d8$	-	-	-	++++	98 to 9F
INCW SP	3	1	$(SP) \leftarrow (SP) + 1$	-	-	-	----	C1
DECW SP	3	1	$(SP) \leftarrow (SP) - 1$	-	-	-	----	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
BZ/BEQ rel	3	2	If $Z = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FD
BNZ/BNE rel	3	2	If $Z = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FC
BC/BLO rel	3	2	If $C = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	F9
BNC/BHS rel	3	2	If $C = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	F8
BN rel	3	2	If $N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FB
BP rel	3	2	If $N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FA
BLT rel	3	2	If $V \vee N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FF
BGE rel	3	2	If $V \vee N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FE
BBC dir: b,rel	5	3	If $(dir: b) = 0$ then $PC \leftarrow PC + rel$	-	-	-	-+--	B0 to B7
BBS dir: b,rel	5	3	If $(dir: b) = 1$ then $PC \leftarrow PC + rel$	-	-	-	-+--	B8 to BF
JMP @A	2	1	$(PC) \leftarrow (A)$	-	-	-	----	E0
JMP ext	3	3	$(PC) \leftarrow ext$	-	-	-	----	21
CALLV #vct	6	1	Vector call	-	-	-	----	E8 to EF
CALL ext	6	3	Subroutine call	-	-	-	----	31
XCHW A,PC	3	1	$(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$	-	-	dH	----	F4
RET	4	1	Return from subroutine	-	-	-	----	20
RETI	6	1	Return form interrupt	-	-	-	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
PUSHW A	4	1		-	-	-	----	40
POPW A	4	1		-	-	dH	----	50
PUSHW IX	4	1		-	-	-	----	41
POPW IX	4	1		-	-	-	----	51
NOP	1	1		-	-	-	----	00
CLRC	1	1		-	-	-	----R	81
SETC	1	1		-	-	-	----S	91
CLRI	1	1		-	-	-	----	80
SETI	1	1		-	-	-	----	90

MB89140 Series

INSTRUCTION MAP

L	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext A	MOVW A,PS A	CLR A	SETI	CLR dir: 0	BBC dir: 0,rel	IN A	DE A	JMP @A	MOVW A,PC	
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLR dir: 1	SETC	CLR dir: 1,rel	BBC dir: 1,rel	IN SP	DE SP	MOVW SPA	MOVW A,SP	
2	ROL A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	CLR dir: 2	MOV @A,T	MOV A,@A	BBC dir: 2,rel	IN IX	DE IX	MOVW IX,A	MOVW A,IX	
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	CLR dir: 3	MOVW @A,T	MOVW A,@A	BBC dir: 3,rel	IN EP	DE EP	MOVW EPA	MOVW A,EP	
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8	XOR A,#d8	AND A,#d8	OR A,#d8	OR A,#d8	CLR dir: 4	DAA	DAS	BBC dir: 4,rel	MOVW A,ext A	MOVW ext,A	MOVW A,#d16	XCHW A,PC	
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	XOR A,dir	AND A,dir	OR A,dir	OR A,dir	CLR dir: 5	MOV dir,#d8	CMP dir,#d8	BBC dir: 5,rel	MOVW A,dir A	MOVW dir,A	MOVW SP,#d16	XCHW A,SP	
6	MOV A,@IX+ d	CMP A,@IX+ d	ADDC A,@IX+ d	SUBC A,@IX+ d	XOR A,@IX+ d	AND A,@IX+ d	OR A,@IX+ d	OR A,@IX+ d	CLR dir: 6	MOV @IX+ d,#d8	CMP @IX+ d,#d8	BBC dir: 6,rel	MOVW A,@IX+ d	MOVW @IX+ d,A	MOVW IX,#d16	XCHW A,IX	
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	XOR A,@EP	AND A,@EP	OR A,@EP	OR A,@EP	CLR dir: 7	MOV @EP,#d8	CMP @EP,#d8	BBC dir: 7,rel	MOVW A,@EP A	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP	
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	XOR A,R0	AND A,R0	OR A,R0	OR A,R0	SETB dir: 0	MOV R0,#d8	CMP R0,#d8	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel	
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	XOR A,R1	AND A,R1	OR A,R1	OR A,R1	SETB dir: 1	MOV R1,#d8	CMP R1,#d8	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel	
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	XOR A,R2	AND A,R2	OR A,R2	OR A,R2	SETB dir: 2	MOV R2,#d8	CMP R2,#d8	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel	
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	XOR A,R3	AND A,R3	OR A,R3	OR A,R3	SETB dir: 3	MOV R3,#d8	CMP R3,#d8	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel	
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	XOR A,R4	AND A,R4	OR A,R4	OR A,R4	SETB dir: 4	MOV R4,#d8	CMP R4,#d8	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel	
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	XOR A,R5	AND A,R5	OR A,R5	OR A,R5	SETB dir: 5	MOV R5,#d8	CMP R5,#d8	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel	
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	XOR A,R6	AND A,R6	OR A,R6	OR A,R6	SETB dir: 6	MOV R6,#d8	CMP R6,#d8	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel	
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	XOR A,R7	AND A,R7	OR A,R7	OR A,R7	SETB dir: 7	MOV R7,#d8	CMP R7,#d8	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel	

MB89140 Series

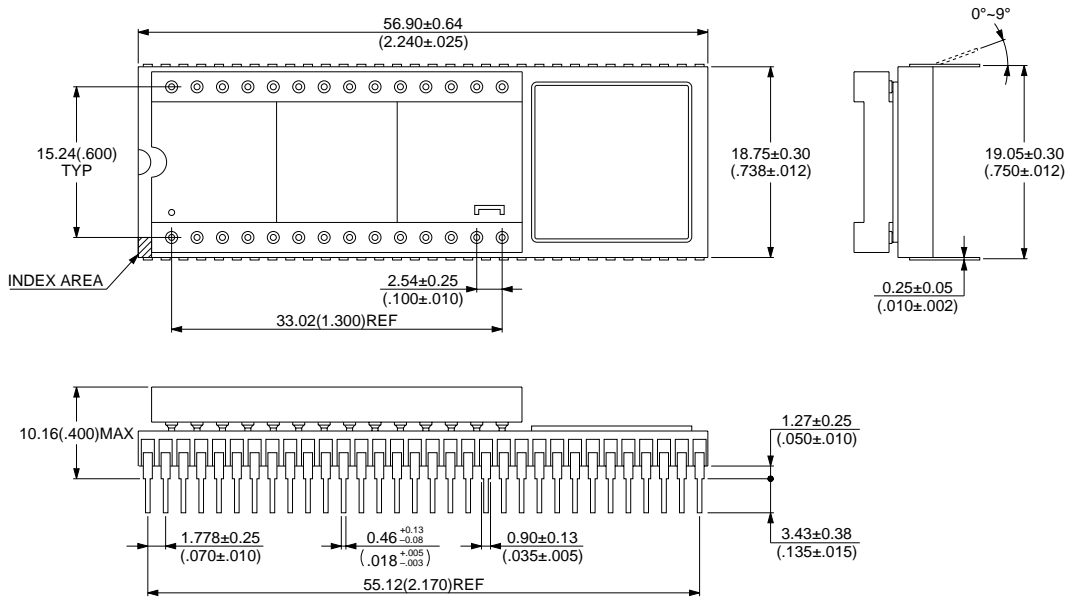
■ MASK OPTIONS

No.	Part number Parameter	MB89PV140	MB89PV140	MB89145V1	MB89145V2	MB89P147V1	MB89P147V2
		-101	-102	MB89146V1	MB89146V2		
1	Power-on reset <ul style="list-style-type: none"> └ With power-on reset └ Without power-on reset 	Fixed to with power-on reset		Specify when ordering masking		Set with EPROM programmer	
2	Reset pin output <ul style="list-style-type: none"> └ With reset output └ Without reset output 	Fixed to with power-on reset		Specify when ordering masking		Set with EPROM programmer	
3	Clock mode selection <ul style="list-style-type: none"> └ Single-clock mode └ Dual-clock mode 	Single clock	Dual clock	Specify when ordering masking		Set with EPROM programmer	
4	Pull-up resistors <ul style="list-style-type: none"> └ P14 to P17 └ P32 to P37 	Fixed to without pull-up resistor		Specify when ordering masking (specify by pin)		Set with EPROM programmer (specify by pin)	
5	Pull-down resistors <ul style="list-style-type: none"> └ P47 to P40 └ P57 to P50 └ P67 to P60 	Fixed to without pull-up resistor		Without pull-down resistor	All pins with pull-down resistor	Without pull-down resistor	All pins with pull-down resistor

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89145V1P-SH MB89145V2P-SH MB89146V1P-SH MB89146V2P-SH MB89P147V1P-SH MB89P147V2P-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89145V1PF MB89145V2PF MB89146V1PF MB89146V2PF MB89P147V1PF MB89P147V2PF	64-pin Plastic QFP (FPT-64P-M06)	
MB89PV140C-101-ES-SH MB89PV140C-102-ES-SH	64-pin Ceramic MDIP (MDP-64C-P02)	
MB89PV140CF-101-ES MB89PV140CF-102-ES	64-pin Ceramic MQFP (MQP-64C-P01)	

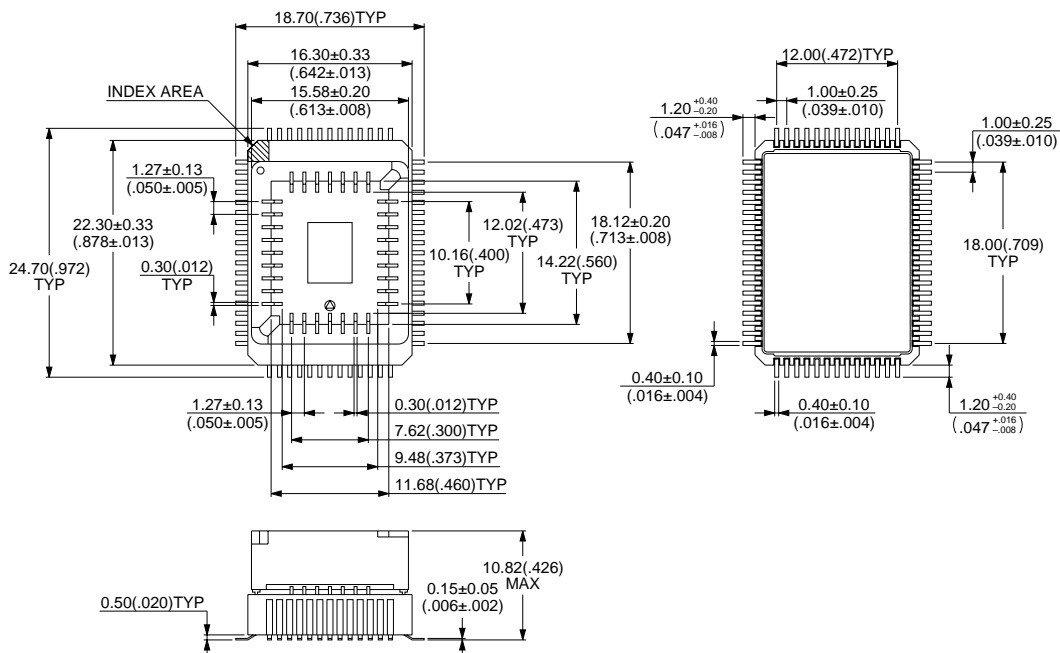
64-pin Ceramic MDIP (MDP-64C-P02)



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Dimensions in mm (inches)

64-pin Ceramic MQFP (MQP-64C-P01)



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Dimensions in mm (inches)

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