CS8321

Micropower 5.0 V, 150 mA Low Dropout Linear Regulator

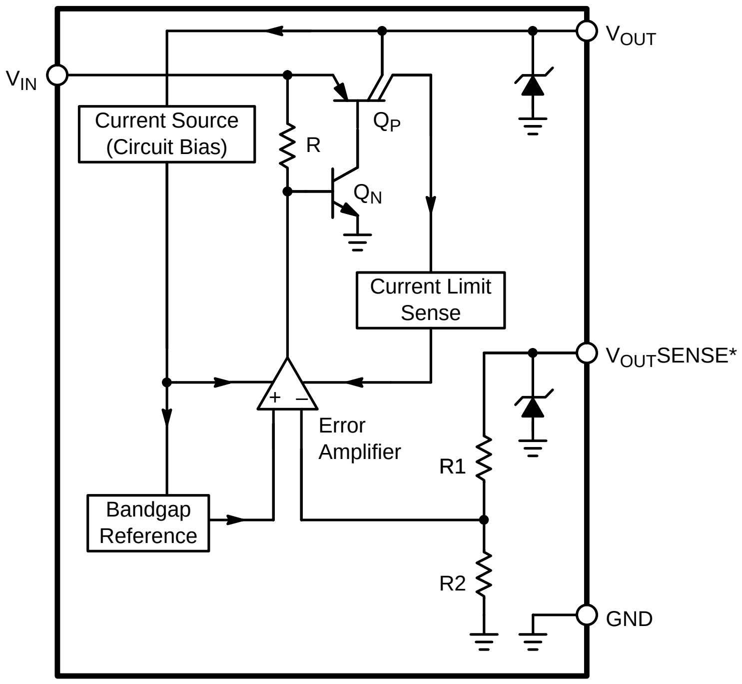
The CS8321 is a precision 5.0 V micropower voltage regulator with very low quiescent current (140 μA typ at 1.0 mA load). The 5.0 V output is accurate within ±2% and supplies 150 mA of load current with a typical dropout voltage of only 300 mV.

This combination of low quiescent current and outstanding regulator performance makes the CS8321 ideal for any battery operated equipment.

The regulator is protected against reverse battery and short circuit conditions. The device can withstand 45 V load dump transients making it suitable for use in automotive environments.

Features

- 5.0 V ± 2% Output
- Low 140 μA (typ) Quiescent Current
- 150 mA Output Current Capability
- Fault Protection
  - –15 V Reverse Voltage Output Current Limit
- Low Reverse Current (Output to Input)



*Lead Shorted to V_{OUT} in 3–Pin Applications

Figure 1. Block Diagram

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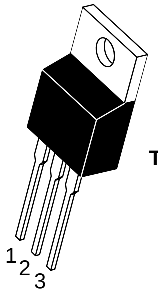
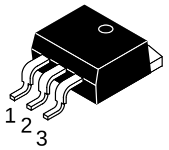


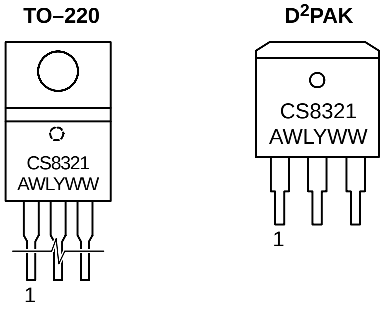
TO–220
THREE LEAD
T SUFFIX
CASE 221A

Pin 1. V_{IN}
2. GND
3. V_{OUT}



D^{2}PAK
3–PIN
DP SUFFIX
CASE 418E

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

Device	Package	Shipping
CS8321YT3	TO–220 THREE LEAD	50 Units/Rail
CS8321YDP3	D^{2}PAK, 3–PIN	50 Units/Rail
CS8321YDPR3	D^{2}PAK, 3–PIN	750 Tape & Reel

*Contact your local sales representative for SO–16, DIP–16, SO–8, and DIP–8 package options.

February, 2002 – Rev. 4

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
Transient Input Voltage		–15, 45	V
Output Current		Internally Limited	–
ESD Susceptibility (Human Body Model)		2.0	kV
Junction Temperature		–40 to 150	°C
Storage Temperature		–65 to 150	°C
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	°C °C

1. 10 seconds max.
2. 60 seconds max above 183°C

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS

(6.0 V < V_{IN} < 26 V, I_{OUT} = 1.0 mA, –40°C ≤ T_A ≤ 125°C, –40°C ≤ T_J ≤ 150°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage, V_{OUT}	9.0 V < V_{IN} 16 V, 100 mA ≤ I_{OUT} ≤ 150 mA	4.9	5.0	5.1	V
Dropout Voltage (V_{IN} – V_{OUT})	I_{OUT} = 150 mA, –40°C ≤ T_A ≤ 85°C I_{OUT} = 150 mA, T_A = 125°C	– –	0.3 –	0.5 0.6	V V
Quiescent Current, (I_Q)	I_{OUT} = 1.0 mA @ V_{IN} = 13 V I_{OUT} < 50 mA @ V_{IN} = 13 V I_{OUT} < 150 mA @ V_{IN} = 13 V	– – –	– 4.0 15	200 6.0 25	μA mA mA
Load Regulation	V_{IN} = 14 V, 100 μA < I_{OUT} < 150 mA	–	5.0	50	mV
Line Regulation	6.0 V ≤ V ≤ 26 V, I_{OUT} = 1.0 mA	–	5.0	50	mV
Ripple Rejection	7.0 ≤ V_{IN} ≤ 17 V, I_{OUT} = 150 mA, f = 120 Hz	60	75	–	dB
Current Limit	–	175	250	–	mA
Short Circuit Output Current	V_{OUT} = 0 V	60	200	–	mA
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	–	140	200	μA

PACKAGE PIN DESCRIPTION

PACKAGE PIN #			
TO–220	D^2PAK	PIN SYMBOL	FUNCTION
1	1	V_{IN}	Input voltage.
2	2	GND	Ground. All GND leads must be connected to ground.
3	3	V_{OUT}	5.0 V, ±2%, 150 mA Output.

CIRCUIT DESCRIPTION AND APPLICATION NOTES

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

The CS8321 is a series pass voltage regulator. It consists of an error amplifier, bandgap voltage reference, PNP pass transistor with antisaturation control, and current limit.

As the voltage at the input, V_{IN}, is increased (Figure 1), Q_N is forward biased via R. Q_N provides base drive for Q_P. As Q_P becomes forward biased, the output voltage, V_{OUT}, begins to rise as Q_P's output current charges the output capacitor. Once V_{OUT} rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to Q_P. The error amplifier monitors the scaled output voltage via an internal voltage divider, R1 and R2, and compares it to the bandgap voltage reference. The error amplifier's output is a current which is equal to the error amplifier's differential input voltage times its transconductance. Therefore, the error amplifier varies the base drive current to Q_N, which provides bias to Q_P, based on the difference between the reference voltage and the scaled output voltage, V_{OUT}.

Antisaturation Protection

An antisaturation control circuit has also been added to prevent the pass transistor from going into deep saturation, which would cause excessive power dissipation due to large bias currents lost to the substrate via a parasitic PNP transistor, as shown in Figure 2.

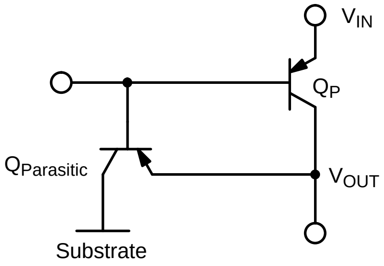


Figure 2. The Parasitic PNP Transistor Which Is Part of the Pass Transistor (Q_P) Structure

Current Limit Limit

The output stage is protected against short circuit conditions. As shown in Figure 3, the output current will fold back when the faulted load is continually increased. This technique has been incorporated to limit the total power dissipation across the device during a short circuit condition, since the device does not contain overtemperature shutdown.

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

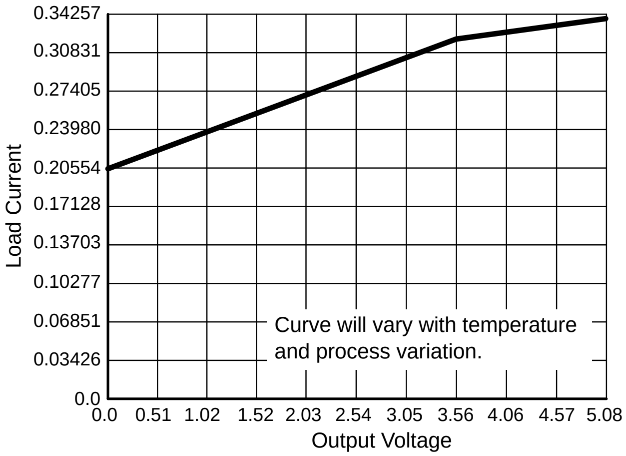
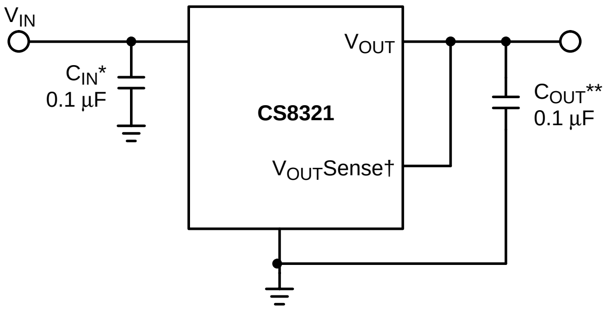


Figure 3. Typical Current Limit and Fold Back Waveform

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 4 should work for most applications, however it is not necessarily the best solution.



*C_{IN} required if regulator is located far from the power supply filter.

**C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

†Pin internally shorted to V_{OUT} in 3–pin applications.

Figure 4. Test and Application Circuit Showing Output Compensation

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 5) is:

$$P_{D(max)} = (V_{IN(max)} - V_{OUT(min)})I_{OUT(max)} + V_{IN(max)}I_Q \qquad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application, and
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^{\circ}C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

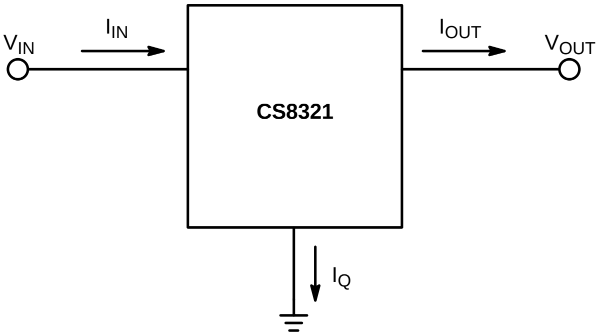


Figure 5. Single Output Regulator with Key Performance Parameters Labeled

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

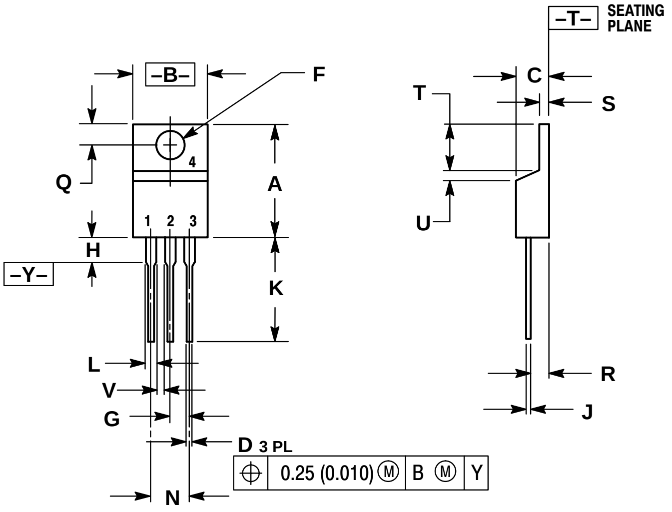
where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

PACKAGE DIMENSIONS

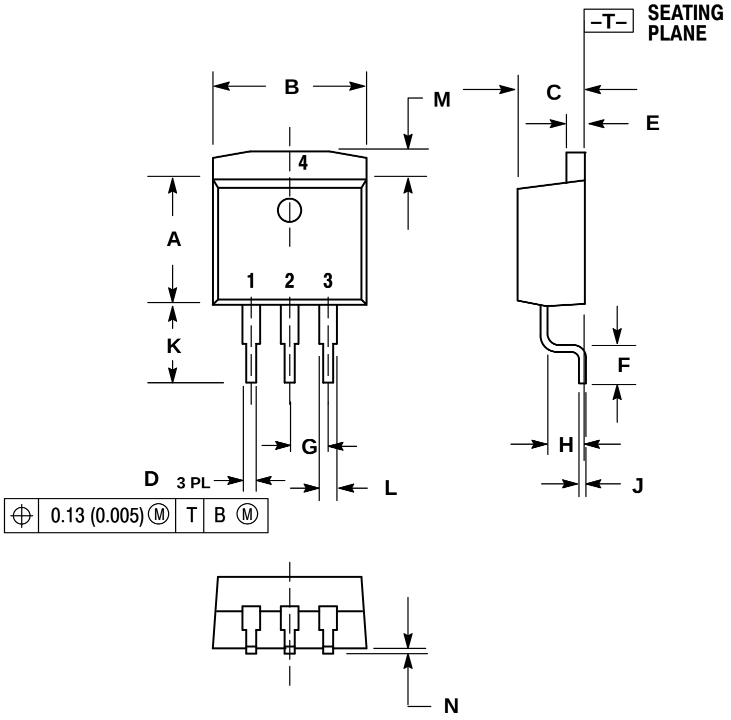
TO–220
THREE LEAD
T SUFFIX
CASE 221A–08
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.025	0.035	0.64	0.89
F	0.139	0.155	3.53	3.93
G	0.100 BSC		2.54 BSC	
H	---	0.280	---	7.11
J	0.012	0.045	0.31	1.14
K	0.500	0.580	12.70	14.73
L	0.045	0.060	1.15	1.52
N	0.200 BSC		5.08 BSC	
Q	0.100	0.135	2.54	3.42
R	0.080	0.115	2.04	2.92
S	0.020	0.055	0.51	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---

D^{2}PAK
3–PIN
DP SUFFIX
CASE 418E–01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.100 BSC		2.54 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
L	0.045	0.055	1.14	1.40
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

PACKAGE THERMAL DATA

PACKAGE THERMAL DATA

Parameter		TO–220	D^2PAK	Unit
$R_{\Theta JC}$	Typical	3.5	1.0*	°C/W
$R_{\Theta JA}$	Typical	50	10–50†	°C/W

*Depending on die area.

†Depending on thermal properties of substrate. $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$.

Notes

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