Features

- **Wide Power Supply Range, 3.0 V to 5.5 V**
- **Fast Read Access Time - 120 ns**
- **Compatible with JEDEC Standard AT27C1024**
- **Low Power 3.3-Volt CMOS Operation**
    - 20 µA max. Standby
    - 36 mW max. Active at 5 MHz for V_{CC} = 3.6 V
    - 165 mW max. Active at 5 MHz for V_{CC} = 5.5 V
- **Wide Selection of JEDEC Standard Packages**
    - 40-Lead 600-mil PDIP and Cerdip
    - 44-Pad PLCC and LCC
    - 40-Lead TSOP
- **High Reliability CMOS Technology**
    - 2000 V ESD Protection
    - 200 mA Latchup Immunity
- **Rapid Programming - 100 µs/byte (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

Description

The AT27LV1024 chip is a low power, low voltage 1,048,576 bit ultraviolet erasable and electrically programmable read only memory (EPROM) organized as 64K x 16 bits. It requires only one supply in the range of 3.0 to 5.5 V in normal read mode operation, making it ideal for portable systems.

With a typical power draw of only 15 mW at 1 MHz and V_{CC} at 3.3 V, the AT27LV1024 draws less than one-fifth the power of a standard 5-V EPROM. Standby mode supply current is typically less than 1 µA at 3.3 V.
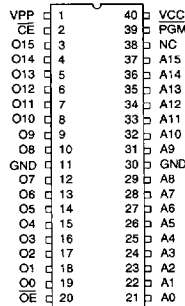
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1 Megabit (64K x 16) Low Voltage UV Erasable CMOS EPROM

Pin Configurations

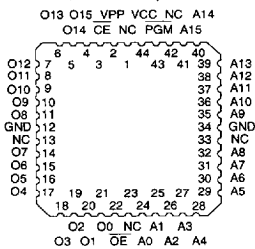| Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View

VPP	1	40	VCC
$\overline{CE}$	2	39	$\overline{PGM}$
O15	3	38	NC
O14	4	37	A15
O13	5	36	A14
O12	6	35	A13
O11	7	34	A12
O10	8	33	A11
O9	9	32	A10
O8	10	31	A9
GND	11	30	GND
O7	12	29	A8
O6	13	28	A7
O5	14	27	A6
O4	15	26	A5
O3	16	25	A4
O2	17	24	A3
O1	18	23	A2
O0	19	22	A1
$\overline{OE}$	20	21	A0

LCC, PLCC Top View

O13 O15 VPP VCC NC A14
O14 $\overline{CE}$ NC $\overline{PGM}$ A15

O12	7 6 5 4 3 2 1 44 43 42 41 40 39	A13
O11	8	38 A12
O10	9	37 A11
O9	10	36 A10
O8	11	35 A9
GND	12	34 GND
NC	13	33 NC
O7	14	32 A8
O6	15	31 A7
O5	16	30 A6
O4	17 18 19 20 21 22 23 24 25 26 27 28 29	A5

O2 O0 NC A1 A3
O3 O1 $\overline{OE}$ A0 A2 A4

Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1

A9	A10	1 2	40 39	A8 GND
A11	A12	3 4	38 37	A6 A7
A13	A14	5 6	36 35	A4 A5
A15	NC	7 8	34 33	A2 A3
$\overline{PGM}$	VCC	9 10	32 31	A0 A1
VPP	$\overline{CE}$	11 12	30 29	O0 $\overline{OE}$
O15	O14	13 14	28 27	O2 O1
O13	O12	15 16	26 25	O4 O3
O11	O10	17 18	24 23	O6 O5
O9	O8	19 20	22 21	GND O7
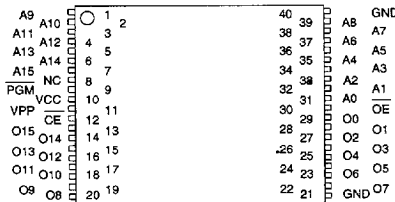
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Description (Continued)

The AT27LV1024 comes in a choice of industry standard JEDEC-approved packages, including: one-time programmable (OTP) plastic PDIP, PLCC, and TSOP, as well as windowed ceramic Cerdip and LCC. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV1024 operating with V_{CC} at 3.0 V produces TTL level outputs that are compatible with standard TTL logic devices operating at $V_{CC} = 5.0$ V.

Atmel's 27LV1024 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV1024 programs identically as an AT27C1024.
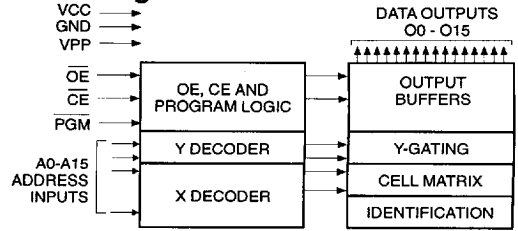
Erasure Characteristics

The entire memory array of the AT27LV1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature......................	-65°C to +125°C
Voltage on Any Pin with Respect to Ground........................	-2.0 V to +7.0 V$^{(1)}$
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V$^{(1)}$
V$_{PP}$ Supply Voltage with Respect to Ground.....................	-2.0 V to +14.0 V$^{(1)}$
Integrated UV Erase Dose..............	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V$_{PP}$	V$_{CC}$	Outputs
Read	V_{IL}	V_{IL}	$X^{(1)}$	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Rapid Program$^{(2)}$	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} $^{(2)}$	D_{IN}
PGM Verify$^{(2)}$	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} $^{(2)}$	D_{OUT}
PGM Inhibit$^{(2)}$	V_{IH}	X	X	X	V_{PP}	V_{CC} $^{(2)}$	High Z
Product Identification$^{(2),(4)}$	V_{IL}	V_{IL}	X	A9=V_H $^{(3)}$ A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC} $^{(2)}$	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require $V_{CC} \geq 4.5$ V.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

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D.C. and A.C. Operating Conditions for Read Operation

		AT27LV1024			
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V

▨ = Advance Information

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D.C. and Operating Characteristics for Read Operation
(V_{CC} = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}				±1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}				±5	μA
I_{PP1} [2]	V_{PP} [1] Read/Standby Current	V_{PP} = V_{CC}				10	μA
I_{SB}	V_{CC} [1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3 V		V_{CC} = 3.6 V		20	μA
				V_{CC} = 5.5 V		100	μA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5 V		V_{CC} = 3.6 V		100	μA
				V_{CC} = 5.5 V		1	mA
I_{CC}	V_{CC} Active Current	I_{CC1}	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6 V	Com.		10	mA
				Ind.		12	mA
		I_{CC2}	f = 5 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		30	mA
				Ind.		40	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA				.4	V
		I_{OL} = 100 μA				.2	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA			2.4		V
		I_{OH} = -100 μA			V_{CC}-0.2		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

## A.C. Characteristics for Read Operation (V_{CC} = 3.0V to 5.5V)

Symbol	Parameter	Condition		-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{ACC} [3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		120		150		200		250	ns
			Ind.		120		150		200		250	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			120		150		200		250	ns
t_{OE} [2,3]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			50		60		70		100	ns
t_{DF} [4,5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float				40		50		50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first				0		0		0		0	ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

▨ = Advance Information

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## A.C. Waveforms for Read Operation [1]
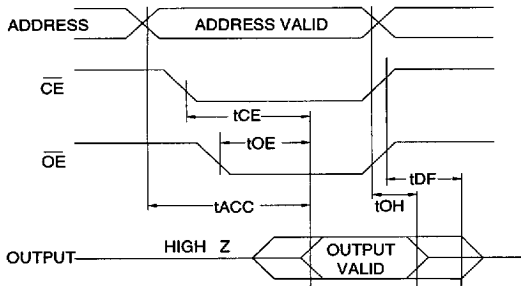
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
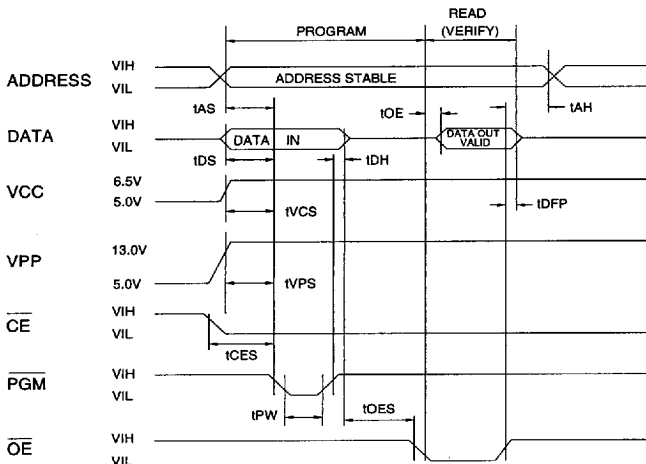
Input Test Waveforms and Measurement Levels

t_R, t_F < 20 ns (10% to 90%)

Output Test Load

Note: $C_L = 100$ pF including jig capacitance.
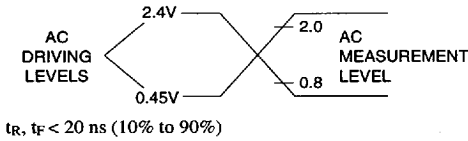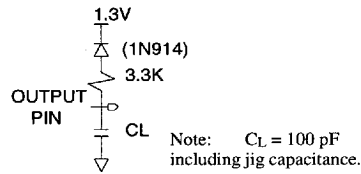
Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]

Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

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D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Sym-bol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL}, V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			50	mA
I_{PP2}	Vpp Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Sym-bol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) . . . . 20 ns
Input Pulse Levels . . . . 0.45 V to 2.4 V
Input Timing Reference Level . . . . 0.8 V to 2.0 V
Output Timing Reference Level . . . . 0.8 V to 2.0 V

Notes:
1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27LV1024 Integrated Product Identification Code[1]

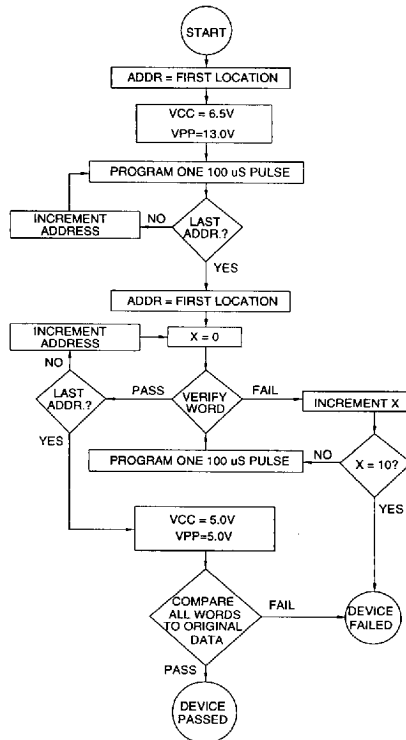| Codes	Pins										Hex Data
	A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Note: 1. The AT27LV1024 has the same Product Identification Code as the AT27C1024. Both are programming compatible.

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Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.5 V and Vpp is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0 V and Vcc to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.

Ordering Information

tACC (ns)	Icc (mA) Vcc = 3.6 V		Ordering Code	Package	Operation Range
	Active	Standby			
120	10	0.02	AT27LV1024-12DC AT27LV1024-12JC AT27LV1024-12LC AT27LV1024-12PC AT27LV1024-12VC	40DW6 44J 44LW 40P6 40V	Commercial (0˚C to 70˚C)
120	12	0.02	AT27LV1024-12DI AT27LV1024-12JI AT27LV1024-12LI AT27LV1024-12PI AT27LV1024-12VI	40DW6 44J 44LW 40P6 40V	Industrial (-40˚C to 85˚C)
150	10	0.02	AT27LV1024-15DC AT27LV1024-15JC AT27LV1024-15LC AT27LV1024-15PC AT27LV1024-15VC	40DW6 44J 44LW 40P6 40V	Commercial (0˚C to 70˚C)
150	12	0.02	AT27LV1024-15DI AT27LV1024-15JI AT27LV1024-15LI AT27LV1024-15PI AT27LV1024-15VI	40DW6 44J 44LW 40P6 40V	Industrial (-40˚C to 85˚C)
200	10	0.02	AT27LV1024-20DC AT27LV1024-20JC AT27LV1024-20LC AT27LV1024-20PC AT27LV1024-20VC	40DW6 44J 44LW 40P6 40V	Commercial (0˚C to 70˚C)
200	12	0.02	AT27LV1024-20DI AT27LV1024-20JI AT27LV1024-20LI AT27LV1024-20PI AT27LV1024-20VI	40DW6 44J 44LW 40P6 40V	Industrial (-40˚C to 85˚C)
250	10	0.02	AT27LV1024-25DC AT27LV1024-25JC AT27LV1024-25LC AT27LV1024-25PC AT27LV1024-25VC	40DW6 44J 44LW 40P6 40V	Commercial (0˚C to 70˚C)
250	12	0.02	AT27LV1024-25DI AT27LV1024-25JI AT27LV1024-25LI AT27LV1024-25PI AT27LV1024-25VI	40DW6 44J 44LW 40P6 40V	Industrial (-40˚C to 85˚C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)
40V	40 Lead, Plastic Thin Small Outline Package OTP (TSOP) 10 x 14 mm

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